# Developments in serial powering and light flex PCB for future Higgs Factories

**FCC-ee vertex detector R&D workshop**
**Pisa, 30-31 October 2025**

Attilio Andreazza

Università di Milano and INFN

**On behalf of:**

- **DRD3 CCF Project Proposal** Birmingham, Bristol, Edinburgh, FBK, Heidelberg, Hochschule RheinMain, IHEP, KIT, Lancaster, Milano, Pisa, Torino, Trento
- **Oxford** (D. Bortoletto, R. Plackett, DMS Sultan)
- and with addition of stolen slides from DRD3 and DRD7 workshops...

INFN MILANO

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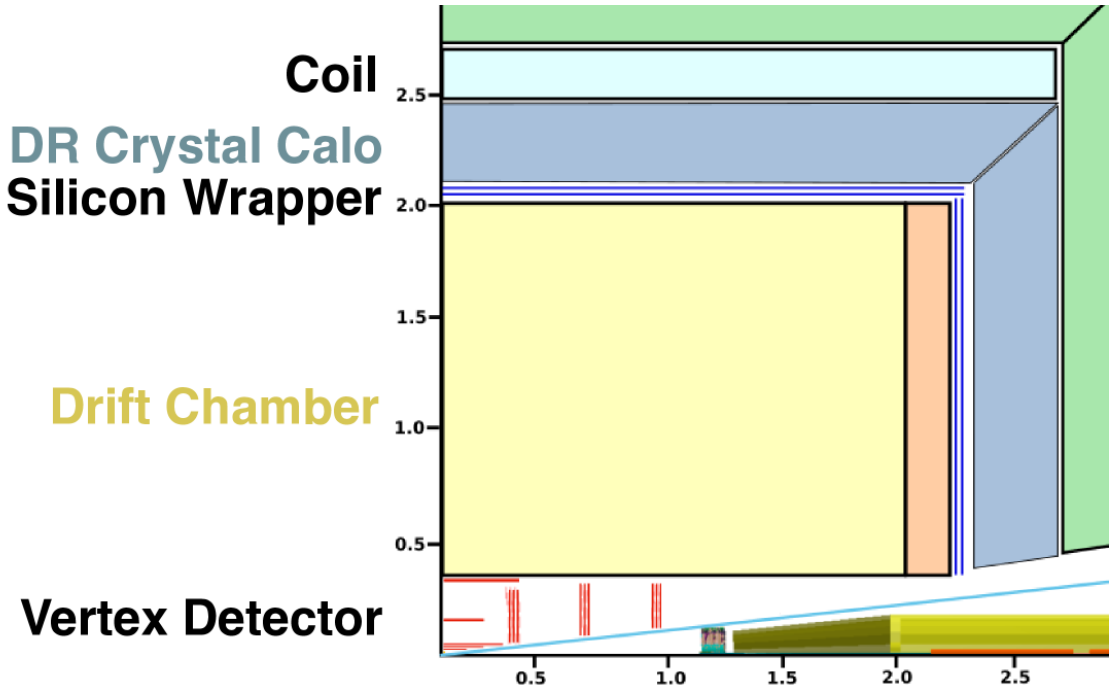
DIPARTIMENTO DI FISICA

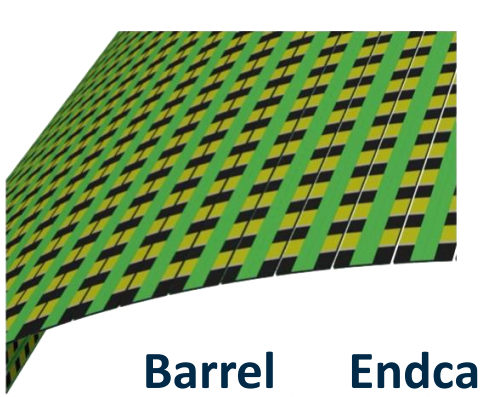
# Motivation: Higgs Factories



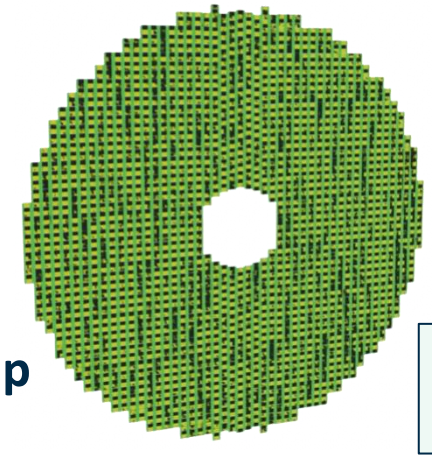

## Silicon tracking in different regions

**(IDEA concept shown here, but general considerations are valid for all layouts)**

- **inner vertex detector (R=1.4-3.3 cm)**
  - **3-5 μm resolution, O(200 MHz/cm²), very low material**
- **outer vertex detector (R=13-31 cm)**
  - **~7 μm resolution, 32 ns timestamp, O(40-100 kHz/cm²)**
  - **material is a concern**
- **silicon wrapper/TOF (R/z = 200 cm)**
  - **~7 μm resolution, 32 ns timestamp**
  - **100 m² (2 layers): ~2.5 10⁵ chips, ~100 kW power**

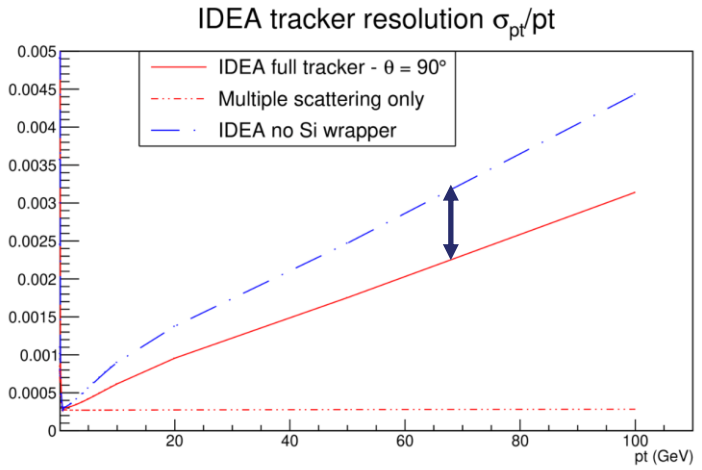


**Barrel**



**Endcap**

The IDEA detector concept for FCC-ee [arXiv:2502.21223](arXiv:2502.21223)



# Project motivation: service integration

**Distribution of power and data signals along the local supports**

- **serial powering** to reduce dissipation on the distribution lines
- **minimize** the number of connections

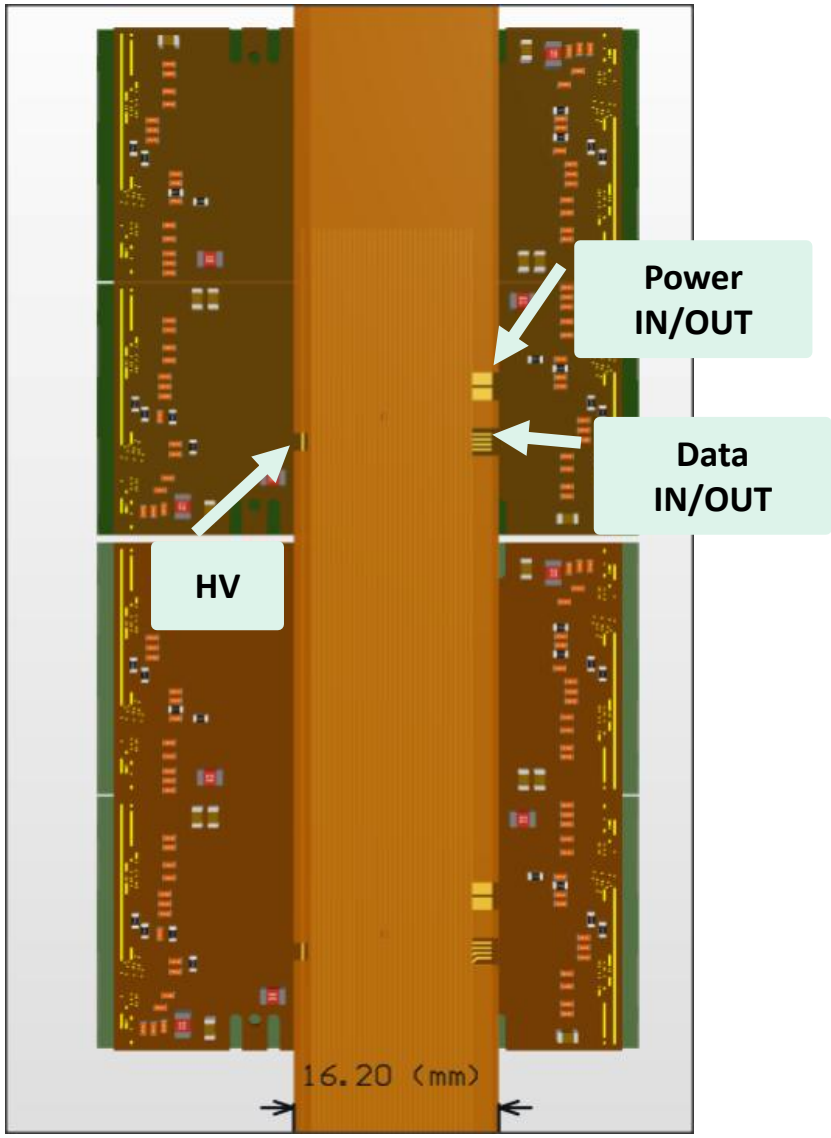
**Read-out units are:**

- **multi-chip modules** (example 2x2 quad modules)
- (or large stitched detectors)

**Minimal I/O connection on chip requires:**

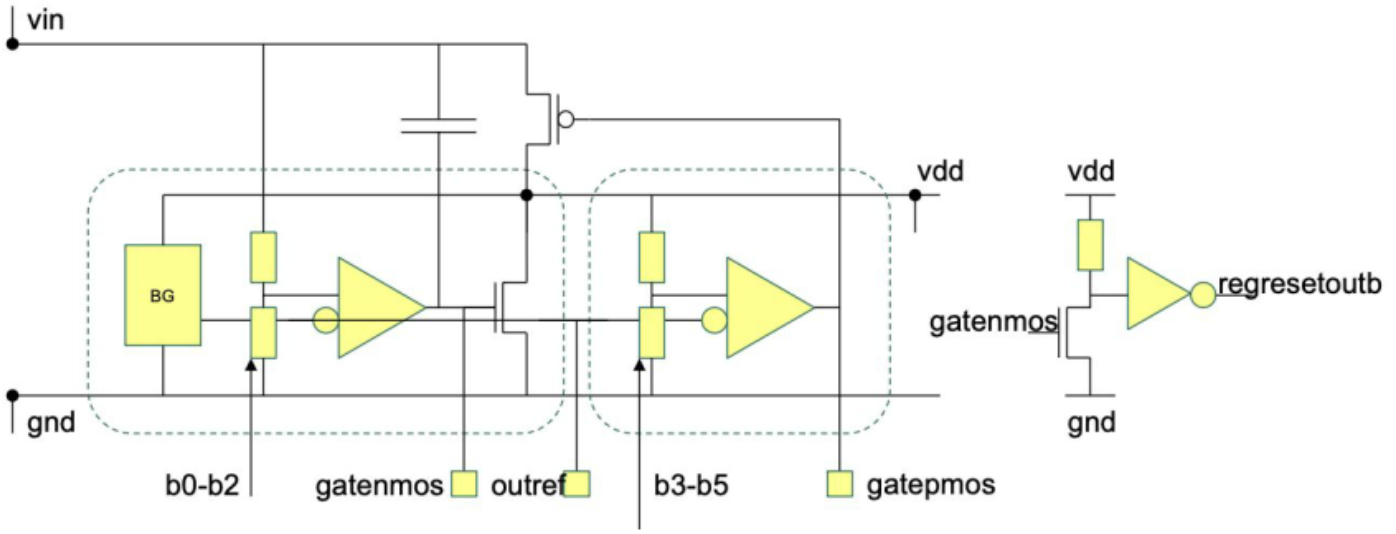
- Serial powering chain: all biases generated internally by shunt-LDO regulators
  - 1 LV and 1 HV line per "stave"
- chip-to-chip data transmissions: local data aggregation on module
  - 1 data-out per "module"
- LVDS module configuration with clock data recovery
  - 1 data-in per module
- **No current MAPS detector providing all these features**

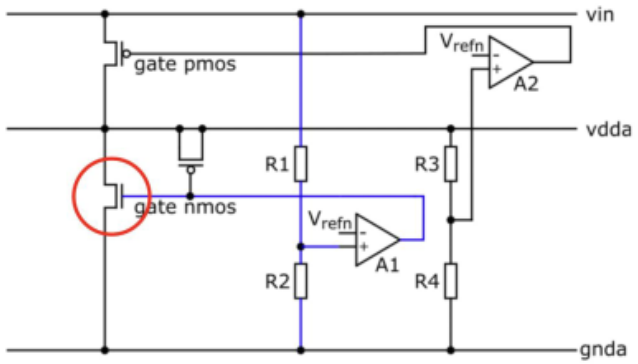
**Reducing material by developing PCB with Al as conductor**



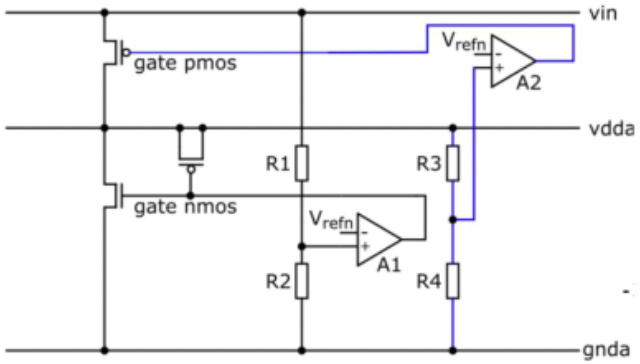
# ATLASPIX3 Serial Powering

- Version **ATLASPix3.1** has possibility for **serial powering** through **two shunt/low dropout regulators**
  - **digital** and **analog** (VDDD/A)
  - **3 bits** to tune threshold of shunt regulator
  - **3 bits** to tune VDD
  - gatenmos, outref, gatepmos are for monitoring
  - regresetoutb can be used as power on reset
- Possibility to use a **single power supply for all the 6 alimentation needed to operate the chips**



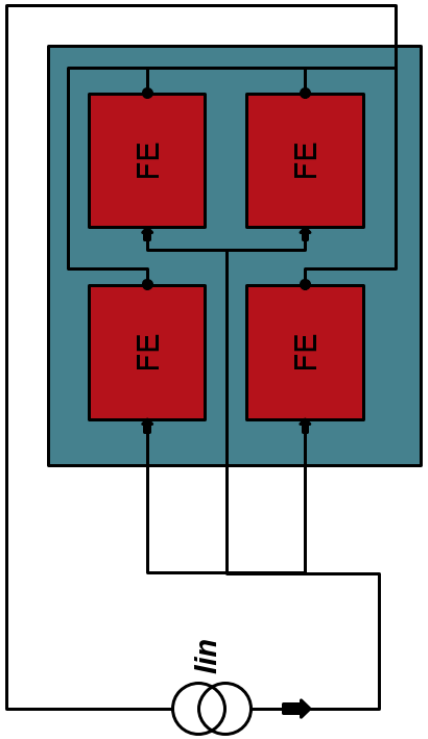

- First loop defines **shunt regulators**

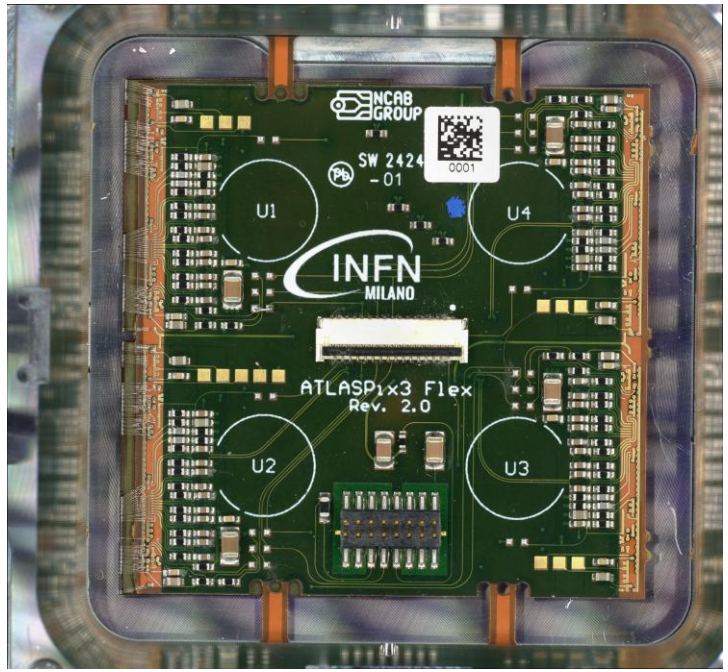


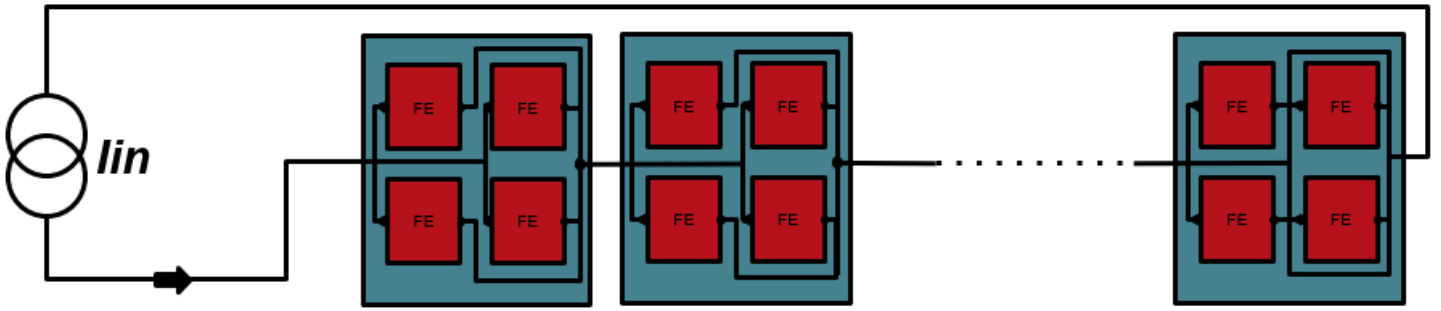

- Second loop **regulates VDDD/As**

# CMOS modules (1)

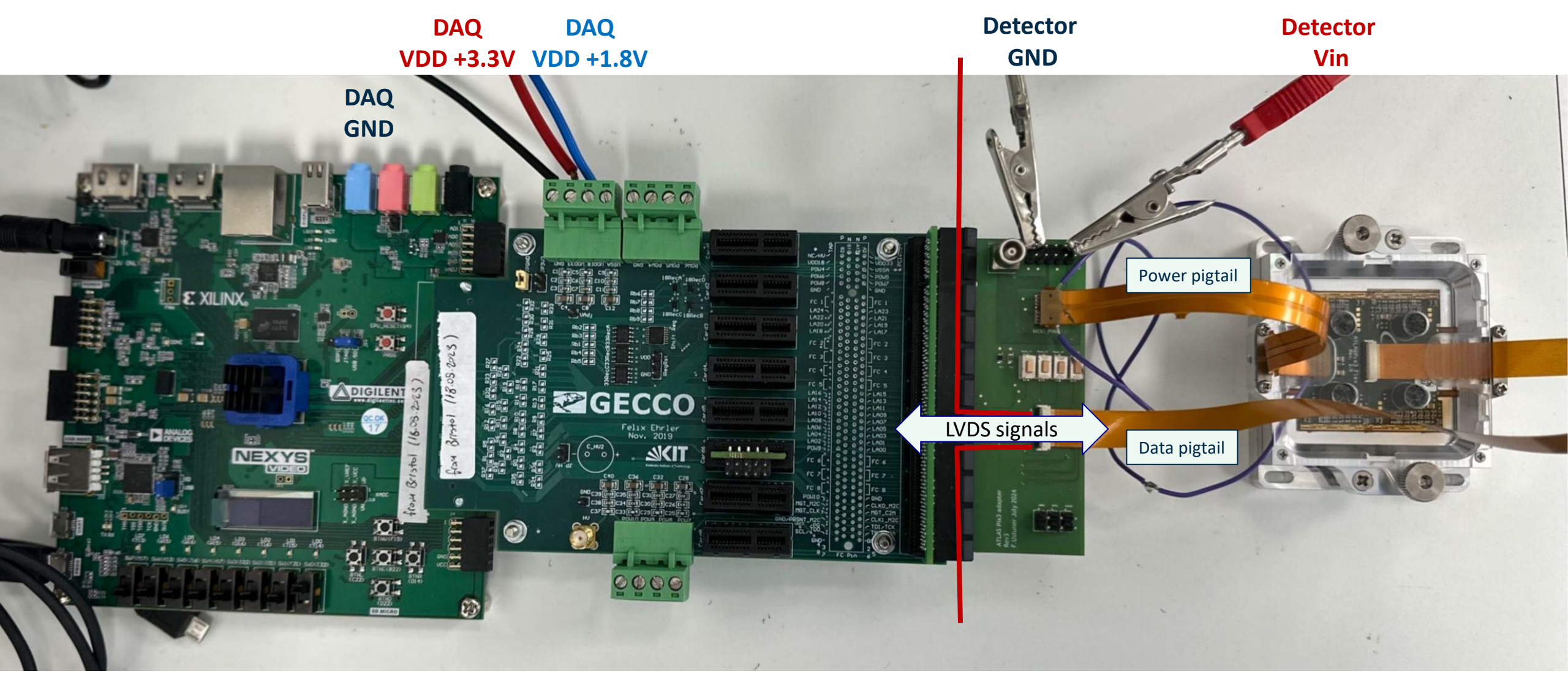
- Prototyping with ATLASPIX3.1 sensors
  - TSI 180 nm CMOS process
  - Almost full-reticle size 2 × 2 cm$^2$
  - 150 mW/cm$^2$
- Multi-chip modules
  - Single LV and HV bias line
  - Common data-in LVDS lines: command, clock, synch, trigger
  - Individual modules data-out LVDS lines
  - AC coupling to DAQ
- Possible to build a serial powering chain
- Probing of SLDO operation before assembling



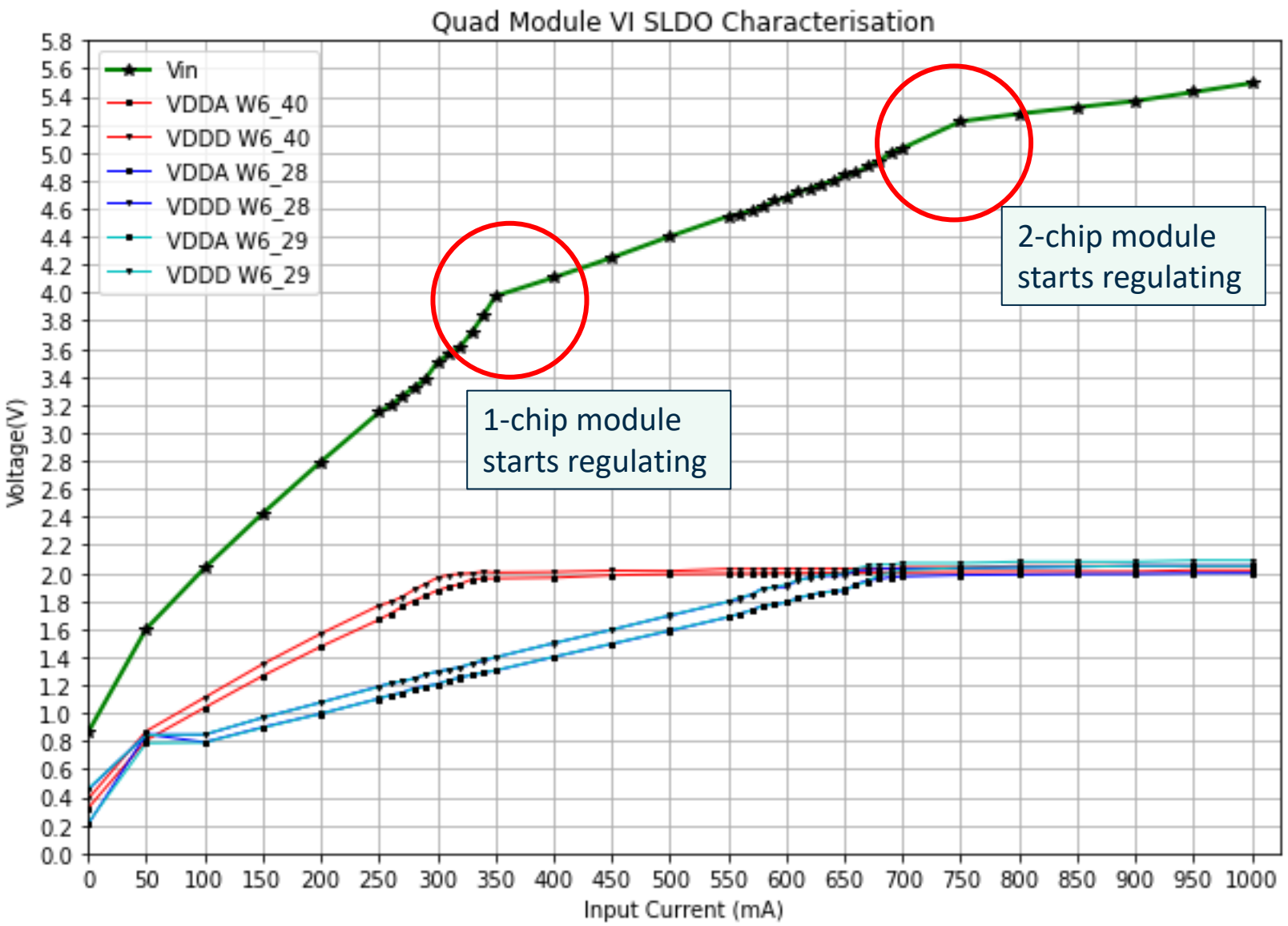



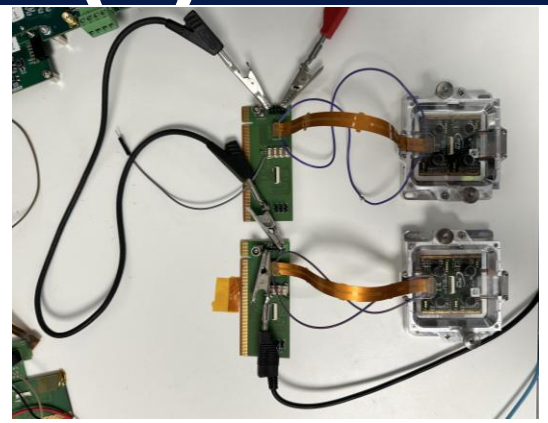
# Module testing setup




- GECCO, flexible readout system developed by KIT
- Firmware and sofware adapted to module operation
- Adapter card splitting the two power domains
- LVDS signals decoupling on the flex PCB

# CMOS modules (2)

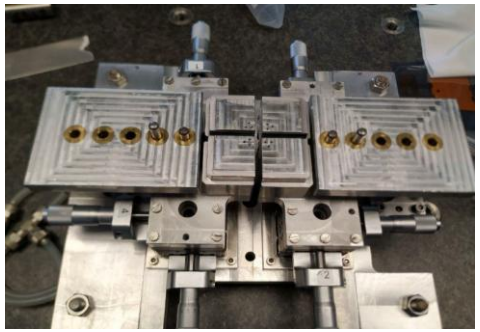


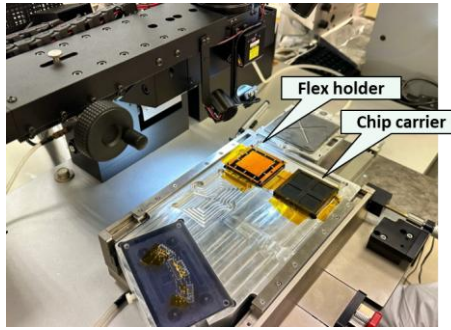



- The serial powering chain for two modules
  - "test modules" with 1 and 2 chips respectively
- Each module has an individual regulation process
  - **1-chip module**
    - VDDD/A = 1.99/1.97 V
    - @ 350 mA
  - **2-chip module**
    - VDDD/A = 2.04/2.00 V
    - @ 700 mA

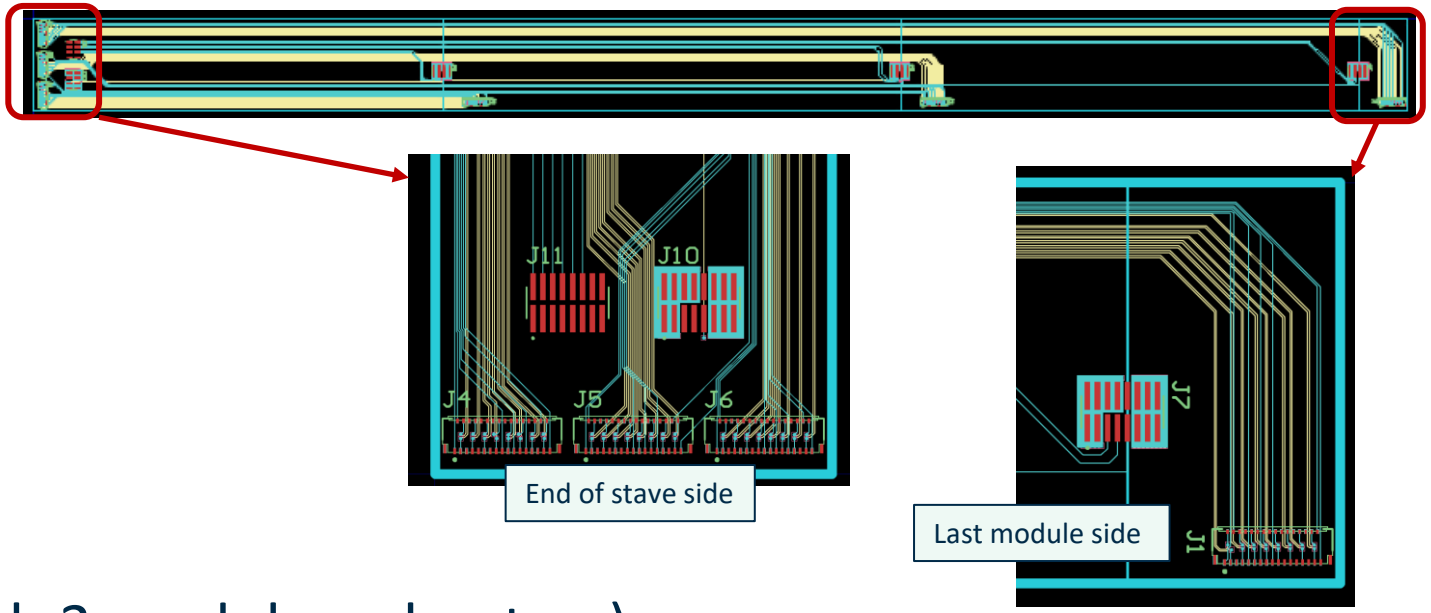
# Al power and data bus

- Assembled modules with ATLASPIX3.1 chips
  - ~7 full modules with 150 μm sensors probed by Milano/Edinburgh
  - Dedicated jig and pick and place available





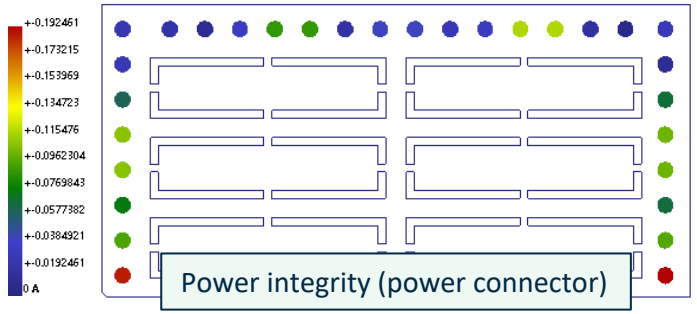

- Designed a power bus to test a multi-module serial power chain
  - Aluminium conductor to reduce thickness in radiation lengths
  - Connecting to modules by pigtails
  - 4 cm × 60 cm size to match CERN Microfabrication Lab capability
  - In production at **CERN** (Rui De Oliveira)




- Loading of cold plate (half stave with 3 modules + heaters)
  - CEPC long-stave design protype available in Pisa

# Al Power and Data Bus

- Large size PCB, "standard" features, with different conductor
  - 4 layers, 15 μm thick Al conductor
    - power and return  in the central layers
    - Data in/out lines in top and bottom layer
  - 100 μm wide lines (~200 μm gap for impedance matching)
  - pass-through vias, 150 μm diameter
    - Copper plated
    - Disuniformity in the layer crossing, but no via above the IPC-2221 standard  of 210 mA

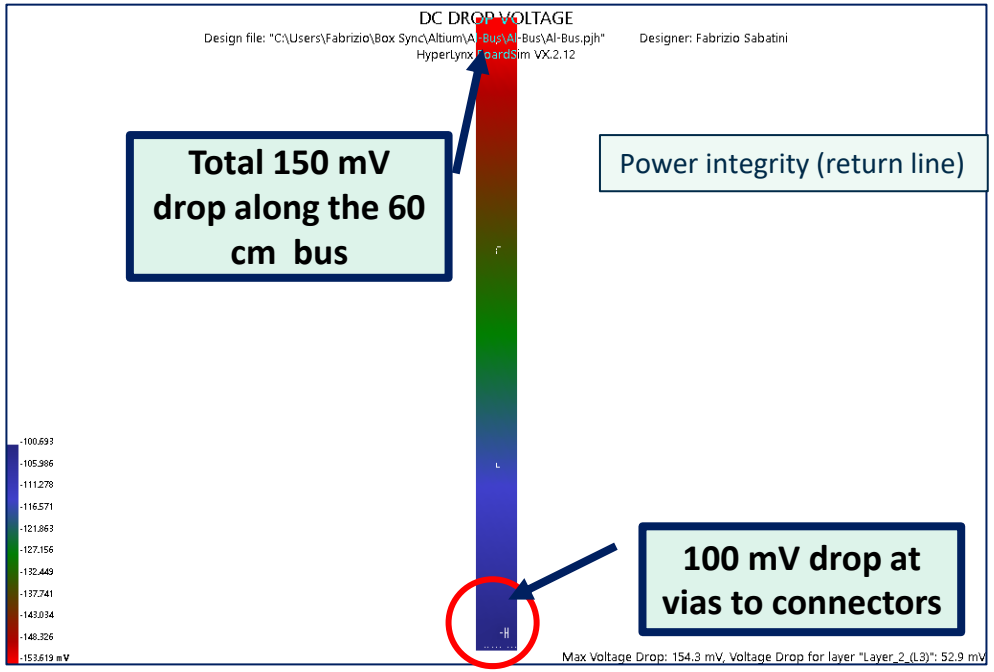



Basic | Dielectric | Metal | Z0 Planning | Manufacturing | Custom View

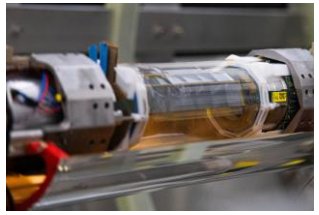
| | Layer Name | Usage | Thickness um | Er | Diff Z0 ohm | Width um | Gap um | Z0 Curve |
|---|---|---|---|---|---|---|---|---|
| 1 | Solder_Mask | Solder Mask | 25 | 4.5 | | | | |
| 2 | FCCL(L1) | Signal | 15 | <Auto> | 100 | 92 | 186.009 | |
| 3 | ADH(1) | Adhesive | 5 | 3.5 | | | | |
| 4 | FCCL(L1)_PI | Substrate | 50 | 3.5 | | | | |
| 5 | ADH(2) | Adhesive | 5 | 3.5 | | | | |
| 6 | FCCL(L2) | Plane | 15 | <Auto> | 1000 | 1000 | <Error> | |
| 7 | ADH(3) | Adhesive | 5 | 3.5 | | | | |
| 8 | FCCL(L2/L3)_PI | Substrate | 50 | 3.5 | | | | |
| 9 | ADH(4) | Adhesive | 5 | 3.5 | | | | |
| 10 | FCCL(L3) | Plane | 15 | <Auto> | 1000 | 1000 | <Error> | |
| 11 | ADH(5) | Adhesive | 5 | 3.5 | | | | |
| 12 | FCCL(L4)_PI | Substrate | 50 | 3.5 | | | | |
| 13 | ADH(6) | Adhesive | 5 | 3.5 | | | | |
| 14 | FCCL(L4) | Signal | 15 | <Auto> | 100 | 92 | 183.938 | |
| 15 | Solder_Mask | Solder Mask | 25 | 4.5 | | | | |

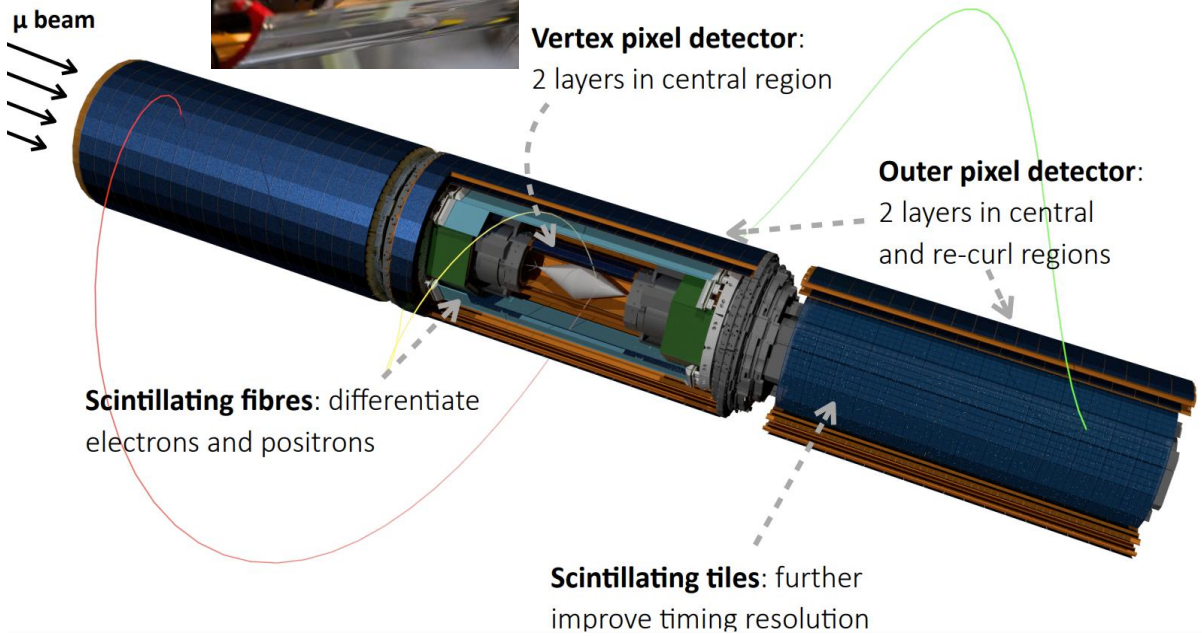
Plan for: Differential pair | Apply as Test Width

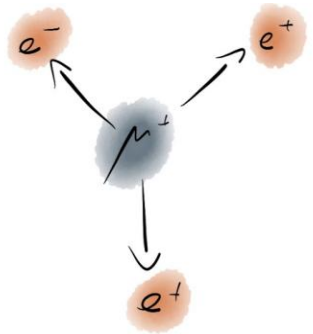
Strategy: Solve for separation | Hint: Move mouse over cell with <Error> for details.



# Mu3e Experience

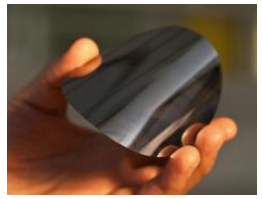


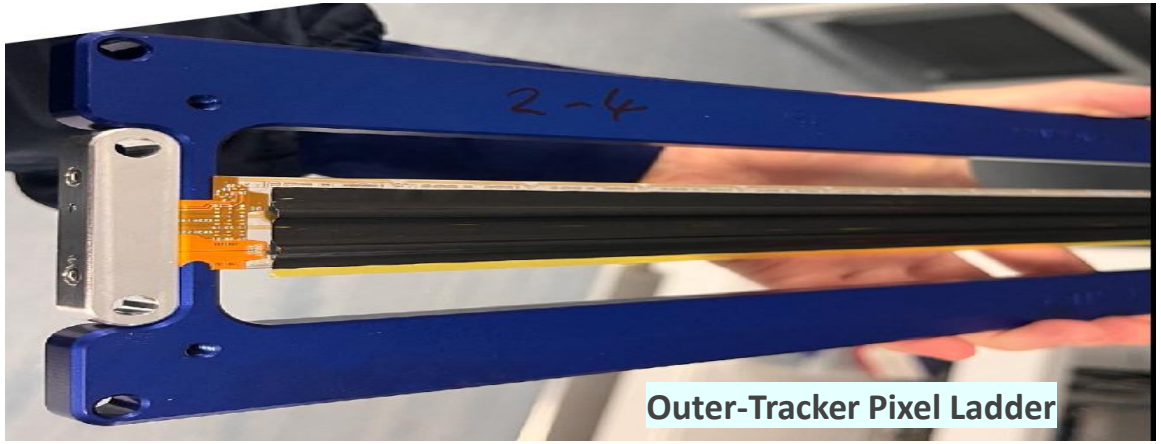


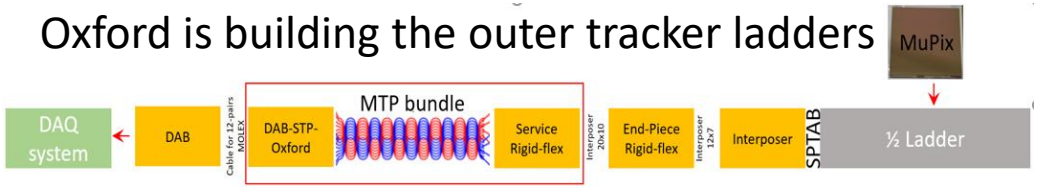





- Mu3e @PSI Phase-1 Data-taking expected in 2026.
- The experiment targets BR (μ —> eee) < $2 \cdot 10^{-15}$ (2000x better than the current limit of BR (μ —> eee) < $1 \cdot 10^{-12}$ @ 90% CL)
- Homogeneous solenoidal magnetic field B = 1T.
- Target momentum resolution < 0.5 MeV/c for **10-53 MeV/c** electrons.
- **Low mass material** is the key requirement to limit multiple scattering in the detector system. (0.1 % $X_0$/Layer)
- Low mass **helium cooling**.
- Oxford is building the outer tracker ladders



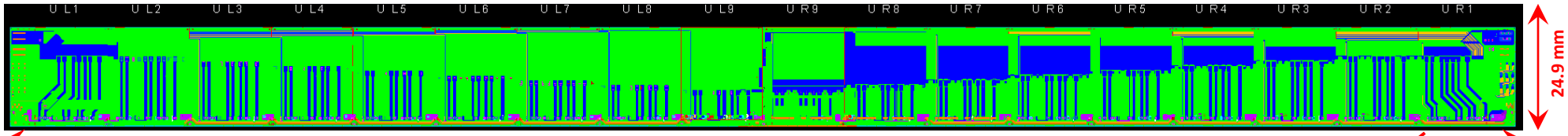



Signal Chain of the Mu3e Outer Tracker

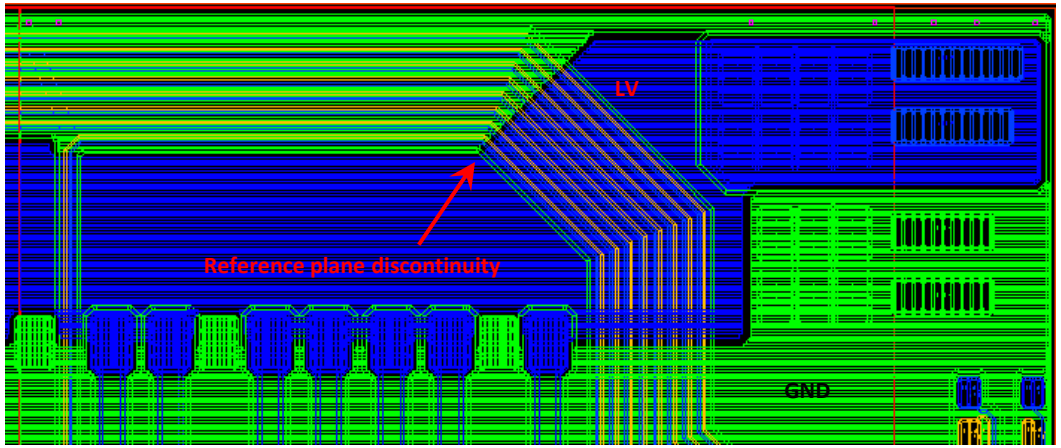
# LTU Low Mass HDI flex

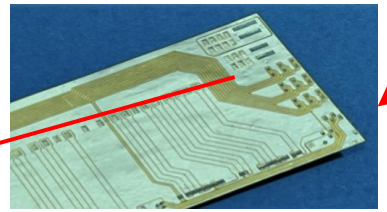
Outer layer L4 HDI-Flex (18-chips)





380.4 mm

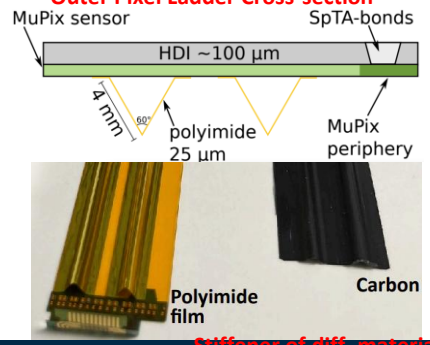


- Ultra-light Aluminium-based HDI Flexes produced by LTU.
- Automatic Gantry at OPMD (Oxford) is used for precision chip-loading of ~40 ± 10 µm intra-chip spacing.
- Limited space constraints required deviations from IPC high-speed design rules. (i.e., displacement-current discontinuity) Talk @ 2nd DRD8 collaboration meeting

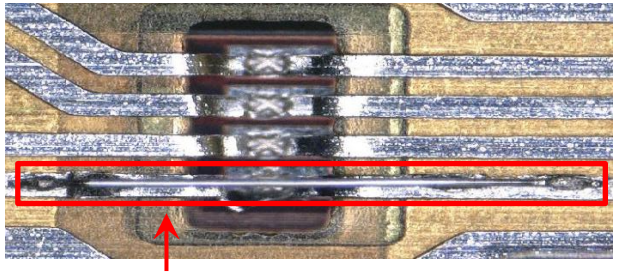
- All signals are routed on the top layer, requiring SP-TAB bonding. Broken traces can be repaired by wire bonding, which is not always reliable. (Routing critical signal traces to the bottom layer will be implemented in the future.)
- To tackle ladder bowing and vibration stability, Oxford explored several mechanical support options.

Outer Pixel Ladder Cross-section



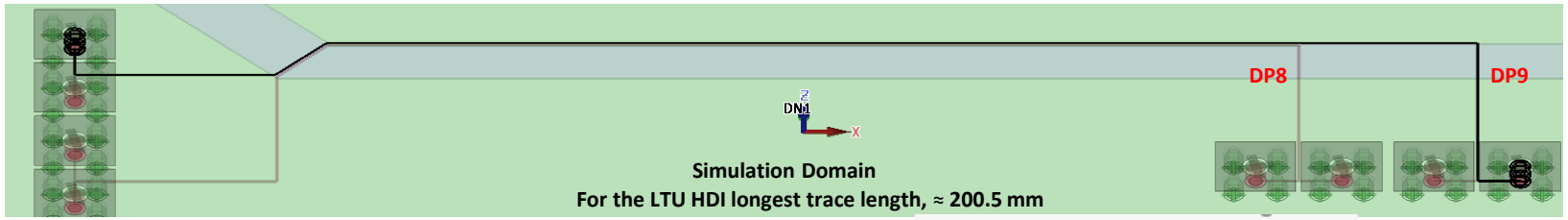

Stiffener of diff. materials

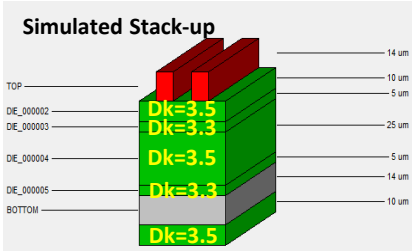
Chip sP-TAB to a LTU-flex

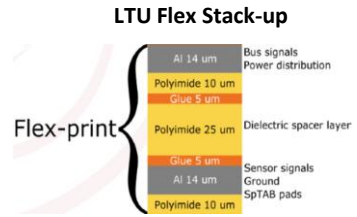


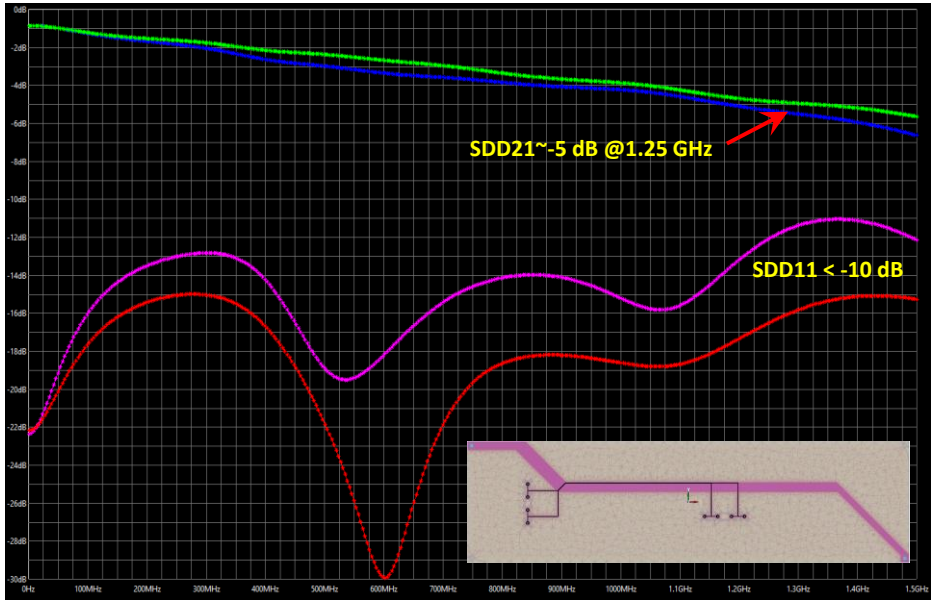
Ripped trace fix with wire-bonding

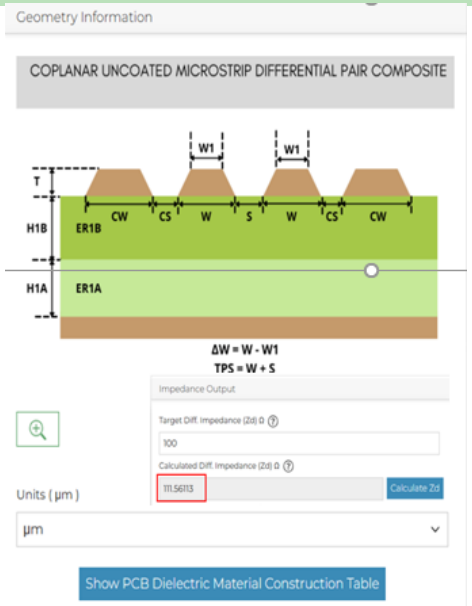
# Flex design and simulation

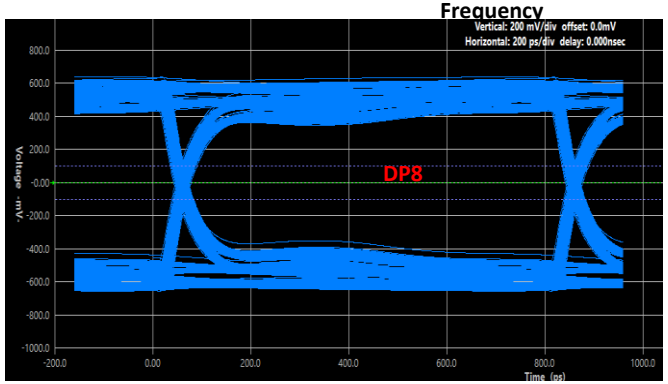


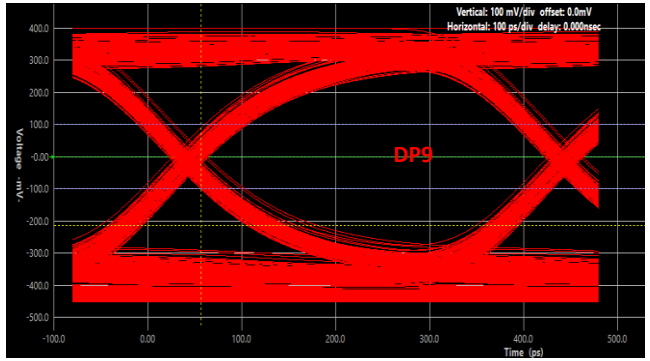



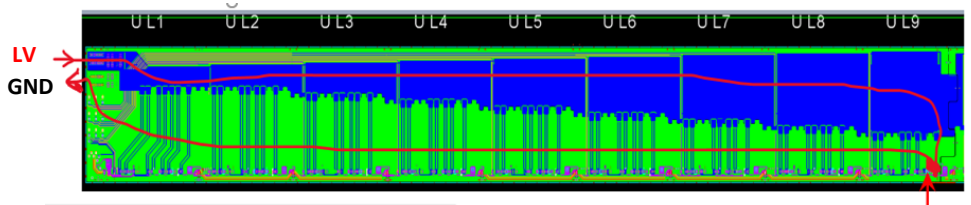



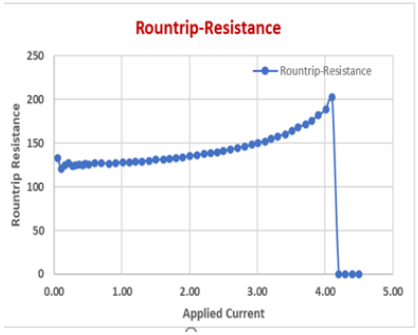



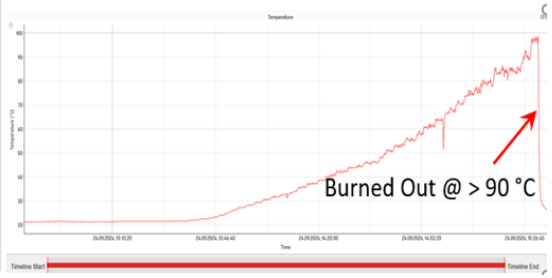




- LTU stack-up and design remained proprietary (not disclosed), which limits the realism of full simulation studies.
- Cadence Allegro used to construct a 2 Al-layer (std. ED-type, Rz ≈ 6 µm) based flex along standard dielectric materials, rated to ~1 MHz.
- A 2D numerical solver reports the **differential pairs' characteristic impedance ~ 110 Ω.**
- HyperLynx EDA tools applied for 3D field-solver–based S-parameter extraction.
- Inter-pair mutual coupling was ignored (led to a completely closed eye).
  - **LTU intra-pair spacing: 109 µm** (≈ 1.7 × **trace width 63 µm** — below the typical ~3× spacing guideline).
- 8b/10b encoded data of 1.25 Gbps were applied to differential pairs of LTU length (~200.5 mm).
- Signal-integrity results:
  - **insertion loss (SDD21) ≈ –5 dB,**
  - **reflection loss < –10 dB**
- Expected noise contribution observed, but eye open enough to transmit MuPix11 chip's required data rate of 1.25 Gbps.

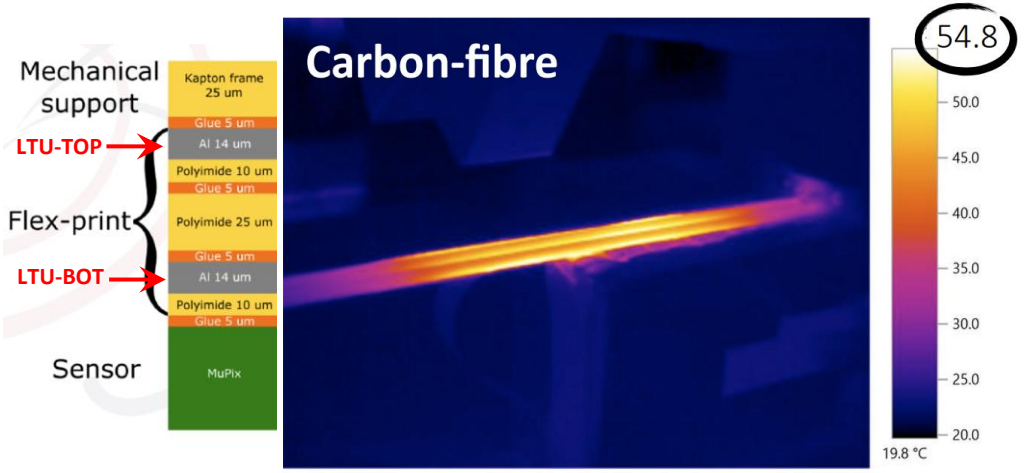
# Electrical and thermal test results



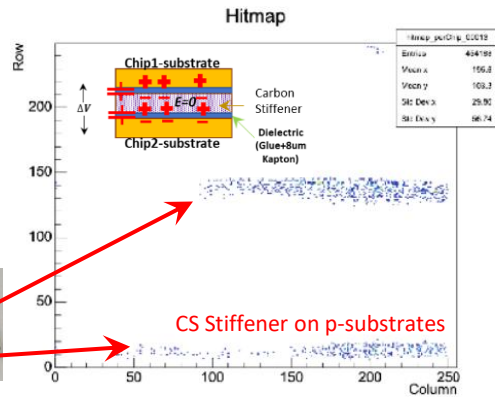




- A ladder is powered into halves with 9 MuPix chips, known as UpStream (US) and DownStream (DS).
- Noise scan at a nominal threshold performed on an electrically functional ladder (w/o stiffener) showed almost no hot pixels on the US side**, confirming a reliable 1.25 Gbps operation**.
- Power consumption of **~190 mW/cm²** per chip corresponds to a current load of ~3.42 A on a half-ladder at an applied voltage of 2 V.
- Round-trip tests show stable resistance up to a 3 A load.
- Burnout tests indicate a critical flex-operation temperature of ~90 °C, beyond which blistering occurs.
- Oxford's current choice of a 25 µm Carbon Stiffener (CS), which is electrically and thermally conductive, can keep the ladder temperature below 60 °C.








- Chip-side (LTU-BOT) CS integration on chips' P-substrates can introduce capacitive HV-noise coupling if the potential difference (ΔV) exists in applied HV on US and DS nodes.
- Flex-side (LTU-TOP) CS integration may instead lead to additional bounce-back noise and cross-talk if glue is on high-speed lines. (due to impedance degradation)
- Carefully dispensed glue on the LTU-TOP side for CS integration shows no noise pattern.

# FUTURE PERSPECTIVES

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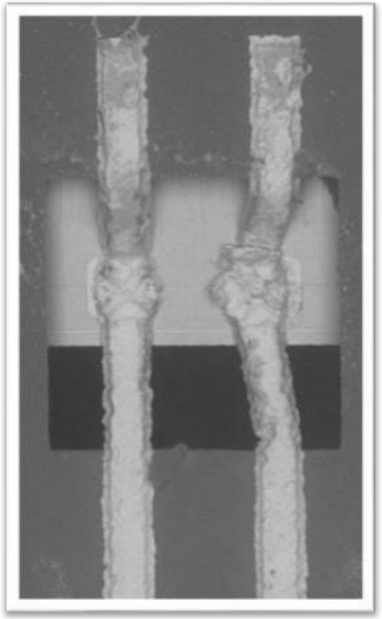
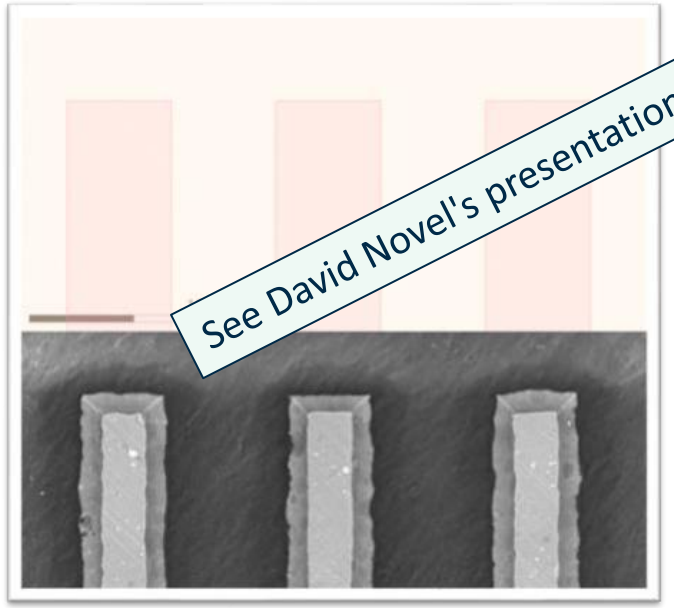
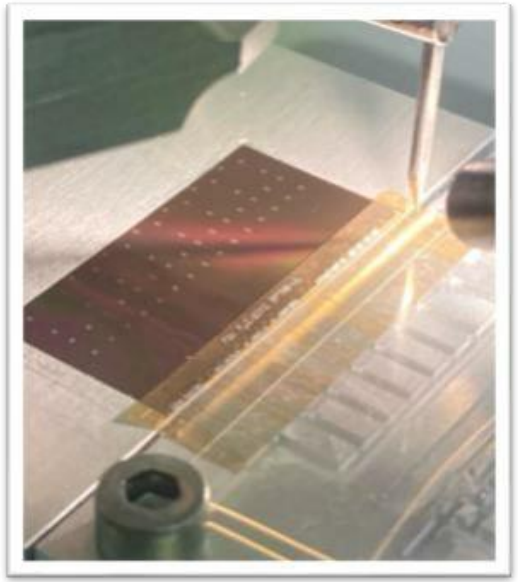
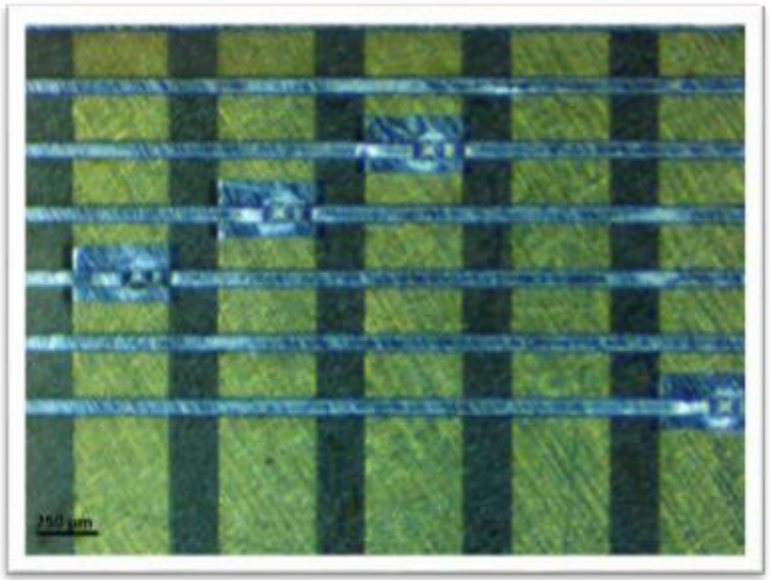
# Thin flex option for Module Flexes

- Fabrication process inspired from the state-of-art LTU-Kharkiv [DOI: 10.15407/fm24.01.143]
- Processing inside FBK cleanrooms
- Kapton-Al PCBs
  - 20 μm Al thickness
  - 25 Kapton thickness
  - **Wafer level manufacturing (6" wafers)**
- Feature size
  - minimal size is 2 × Al thickness = 40 μm
  - very high line density (90 μm pitch)
- Interconnection
  - spTAB 75 × 75 μm tool tip
  - flex-to-chip TAB
  - flex-to-flex TAB:
    - use TAB as vias to reduce overall material
    - connection to additional flexible PCB





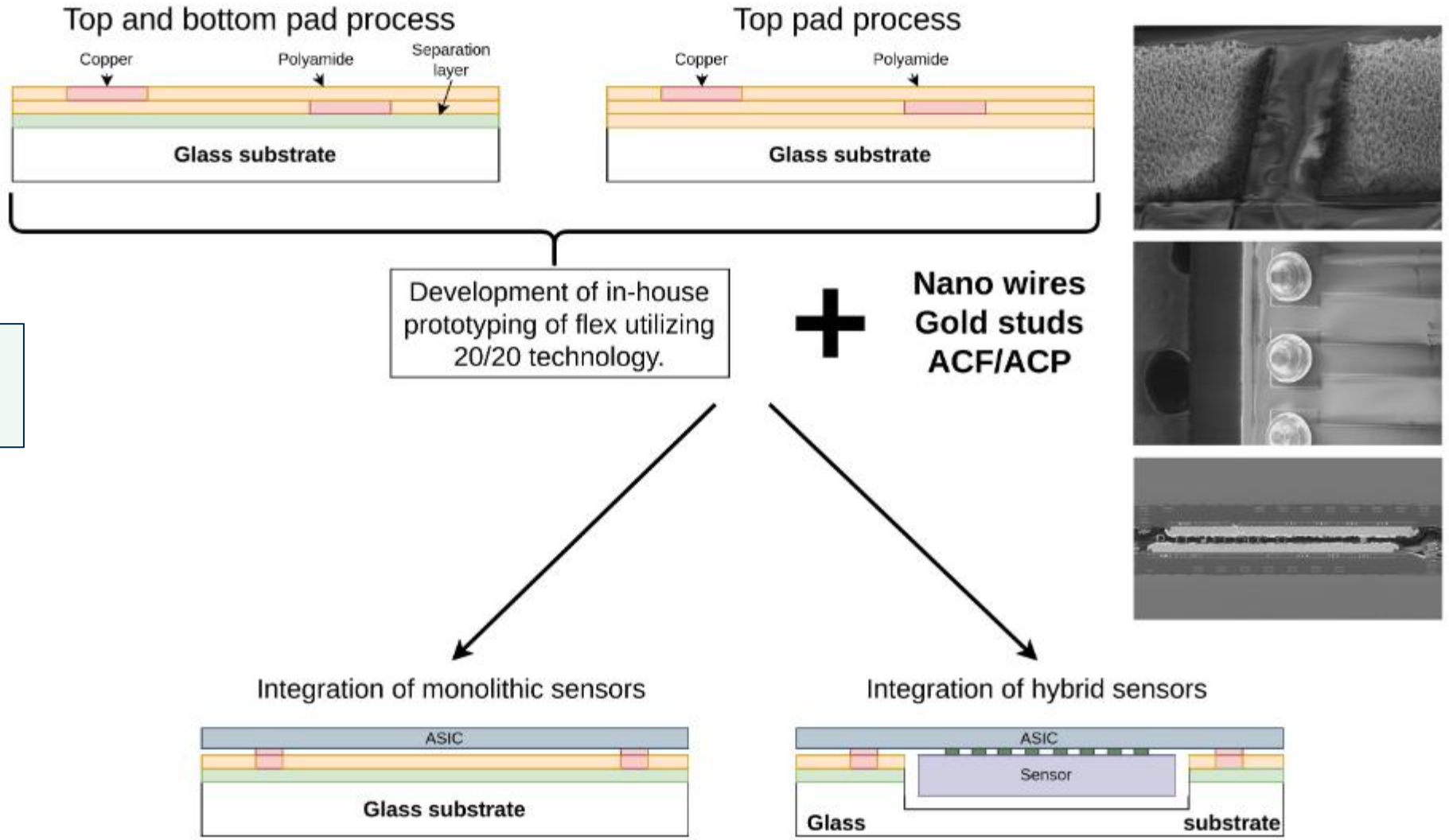





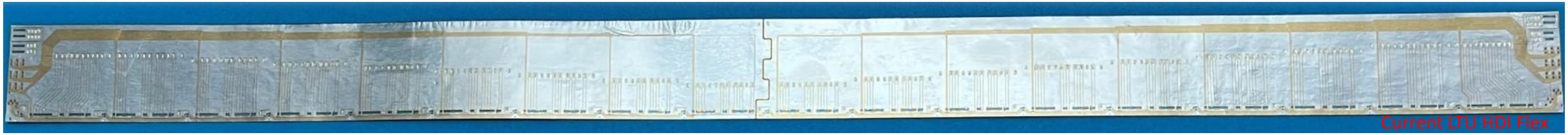
# DRD3 – WG 7 development

EP R&D CERN

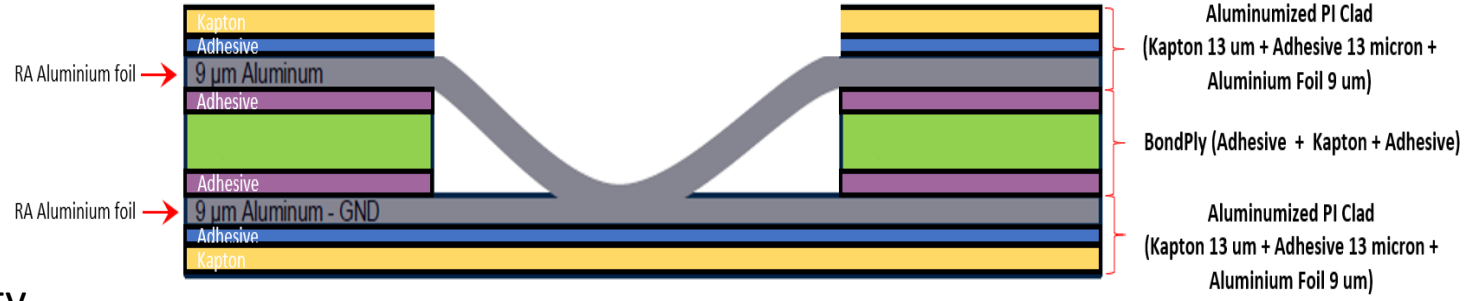
CERN Development of thin flexes and interconnections
J. Weick @ DRD3 week,



# Oxford in-house flex production

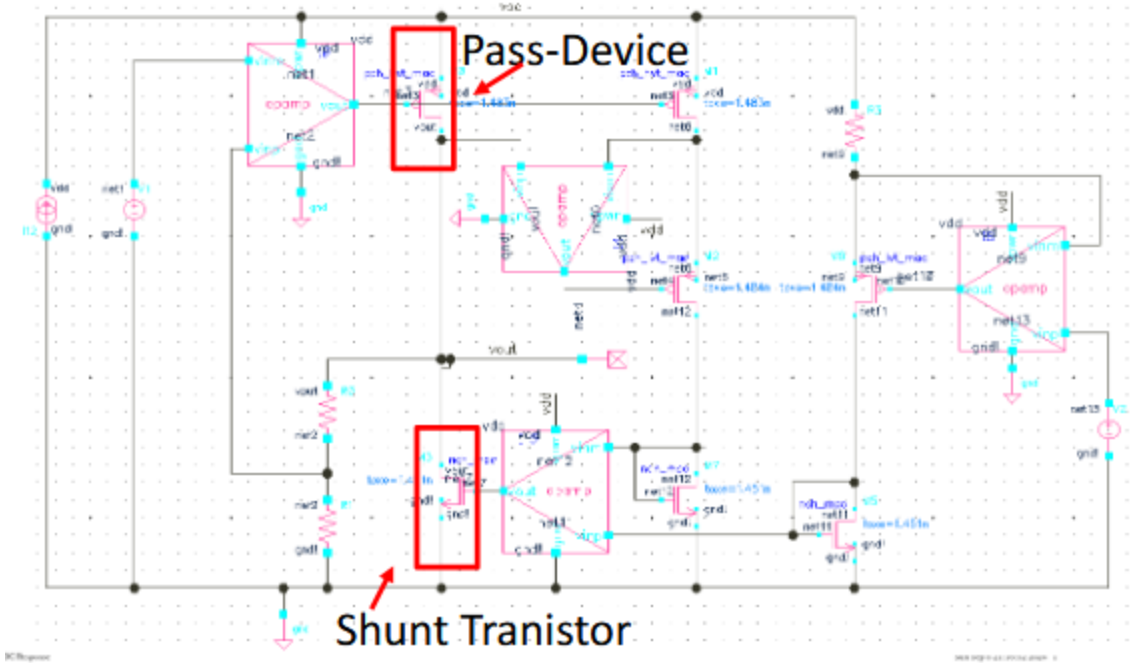


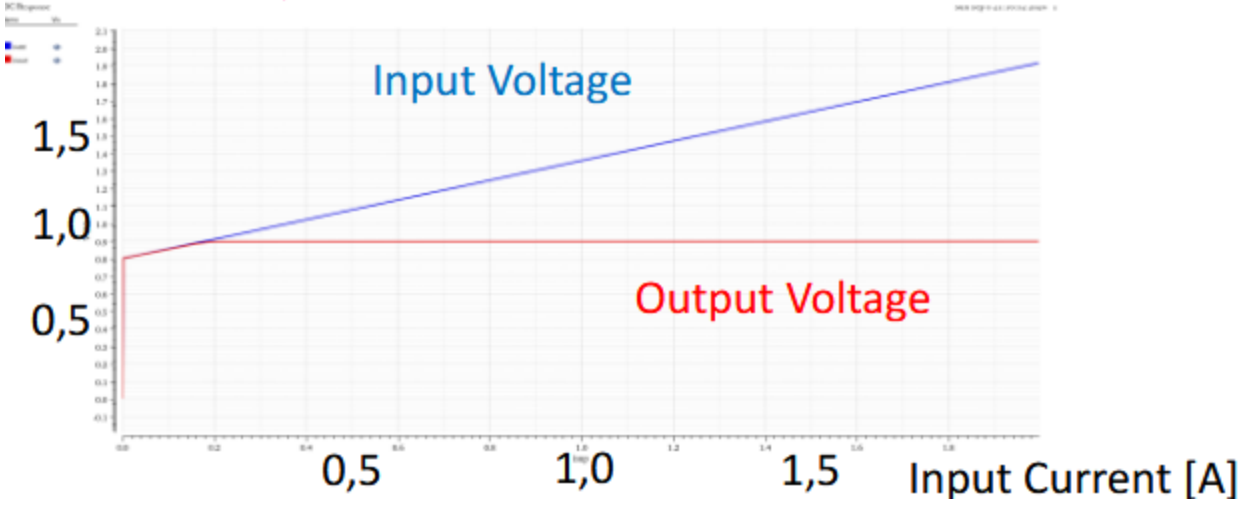

- An uncoated microstrip is vulnerable to radiative losses and electromagnetic interference (EMI).
- A shielded (embedded) microstrip design could mitigate this by adding a proper ground plane, preventing the displacement-current discontinuity observed on the current LTU HDI flex.
- High-speed-grade aluminium foil (Rz < 1.5 µm) suppliers are being explored.
- High-speed adhesive, coverlay, and bond-ply materials are preferred for reliable Gbps transmission; potential suppliers have been identified.
- Oxford already operates a high-precision laser ablation system capable of producing fine traces (20 µm pitch).
- A FPCB lamination press unit is necessary to support multilayer structure fabrication.




**Oxford Proposal**

# DRD7 Activity on Serial Powering



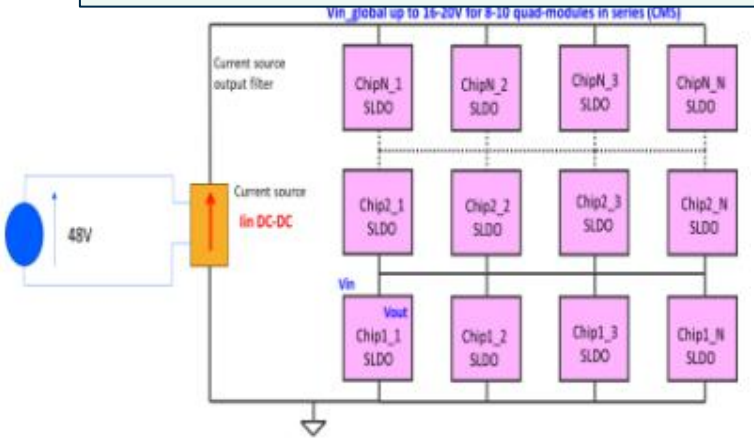

- First simulation studies performed in 28nm based on Verilog-A amplifier models
- Devices types and dimensions studied for shunt and pass-device
- Studies show SLDO thin-gate oxide core transistor implementation feasible in 28nm
- Technology limits maximum input voltage to 1.8V with overvoltage tolerant design (2V @ 65nm)
- Transistor level schematics imported (manually) into 28nm kit
- Design of subblocks ongoing

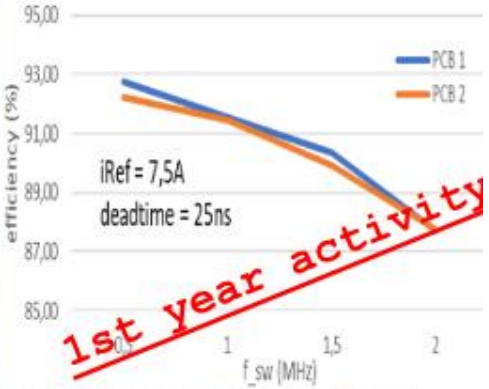
Serial powering for next generation chips:
SLDO implementation in the TSMC 28 nm technology node
M. Karagounis @ DRD7 Annual Workshop

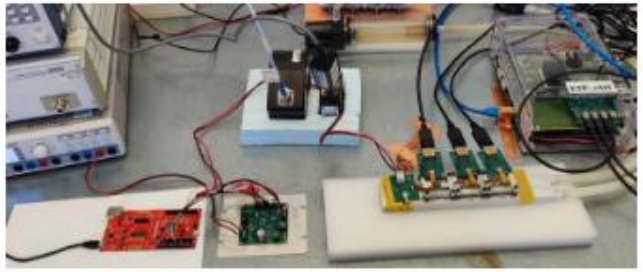
# DRD7 Activity on Serial Powering

GaN based DC-DC converter for Serial Powering by ITA
M. Karagounis @ DRD7 Annual Workshop

- The main goal of this task is to assess the feasibility of utilizing GaN-based DC-DC converters (current source) for serial powering applications.
- Several critical issues have been identified to optimized the design of these units
  - ➢ Design implications associated to GaN switching
    - ✓ High frequency (MHz) and short transition times (ns)
    - ✓ Precise Duty Control & deadtimes (High Resolution PWM modulator)
  - ➢ EMI filter design: Filter embedded in the PCB & magnetic components
  - ➢ Radiation hardness
  - ➢ Modular/Multiphase concept
- Activities 2023-2024
  - ➢ Design & Develop a preliminary prototype (2023)
  - ➢ Performance evaluation, regarding efficiency, dissipation and EMI testing (2024-2025)
    - ✓ This evaluation also involved combined EMI testing in radiation environments



# Conclusions

## Activity going on in experiment and DRDs to develop high-integration low material techniques

- Serial powering demonstrated on HVCMOS sensors
- Gaining experience with Al flexes and further developments on small feature size and innovative interconnections of interest for both the Vertex and the Si Wrapper

## What is missing?

IDEA Silicon Wrapper barrel has a hit rate of ~17 kHz/cm$^2$ (see Armin's presentation)

- Assuming 48 bits/hit, a Si Wrapper layer of 32 m$^2$ have a total data rate of 260 Gbps (with safety factor)
- 80000 HV CMOS chips may be readout by only 260 x 1 Gbit links
- provided a very aggressive data merging scheme can be implemented

Vertex and wrapper endcaps have hit rates up to O(1-4 MHz/cm$^2$)

- 1 Gbps link needed per 4-5 chips

But very few devices (MALTA, ATLASPIX4) implement data aggregation at the sensors level to experiment this feature in an integration process.

# BACKUP

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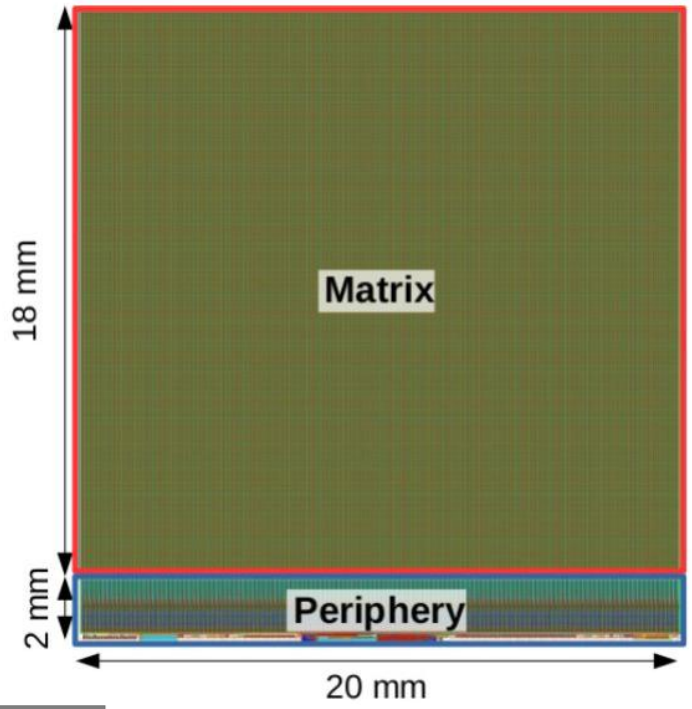
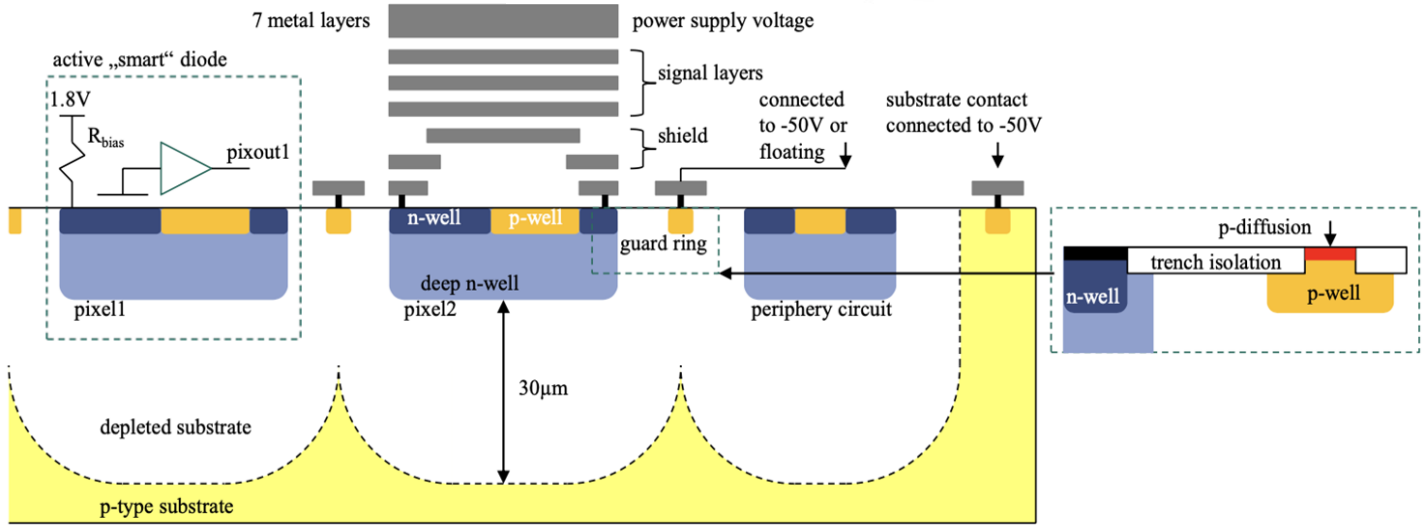
# Institutes and Contact Persons

| Institute | DRD3 | RD50 | Project contact |
|---|---|---|---|
| University of Birmingham | x | x | James Glover |
| University of Bristol | x | | Jaap Velthuis |
| University of Edinburgh | x | | Yanyan Gao |
| University of Heidelberg | x | | Heiko Augustin |
| Hochschule RheinMain | x | | Daniel Muenstermann |
| IHEP | x | x | Yiming Li |
| INFN and University of Milano | x | | Attilio Andreazza |
| KIT | x | | Ivan Peric |
| University of Lancaster | x | x | Harald Fox |
| INFN Pisa | x | x | Fabrizio Palla |
| FBK Trento | x | x | David Novel |
| TIFPA and University of Trento | x | | Roberto Iuppa |
| INFN Torino | x | x | Stefania Beolé |
| **Participating institutes** | **13** | **6** | |

# ATLASPIX3

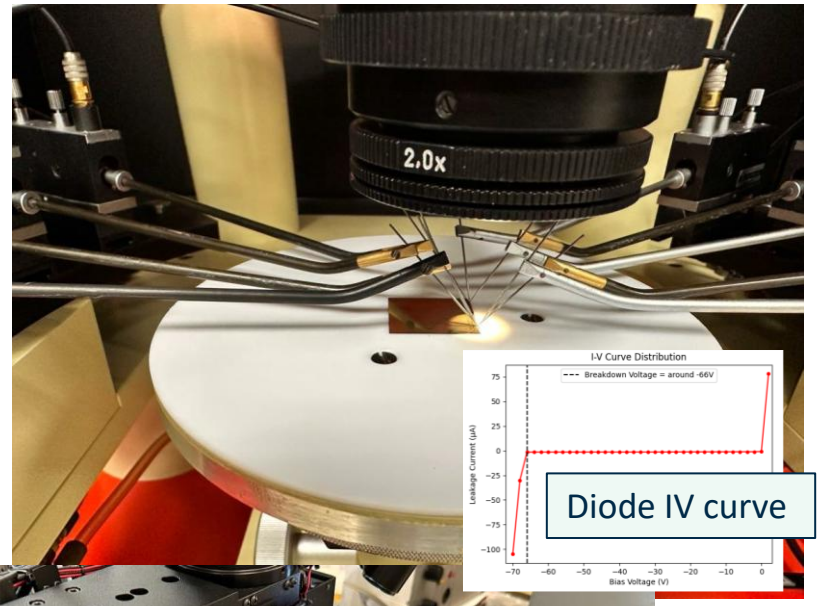
- **ATLASPIX3 general features**
  - **TSI 180 nm HVCMOS** technology
  - full-reticle size **20×21 mm²** monolithic pixel sensor
  - 200 Ωcm substrate (other substrates up to 2 kΩcm also possible)
  - **132 columns of 372 pixels**
  - **pixel size 50×150 µm²** (25×150 µm² on recent prototypes)
  - **breakdown voltage ∼-60 V**
  - up to **1.28 Gbps downlink**
  - **25 ns timestamping**
  - analog pixel matrix, digital processing in periphery
- Both **triggerless** and **triggered** readout modes:
  - two End of Column buffers
  - 372 hit buffers for triggerless readout
  - 80 trigger buffers for triggered readout

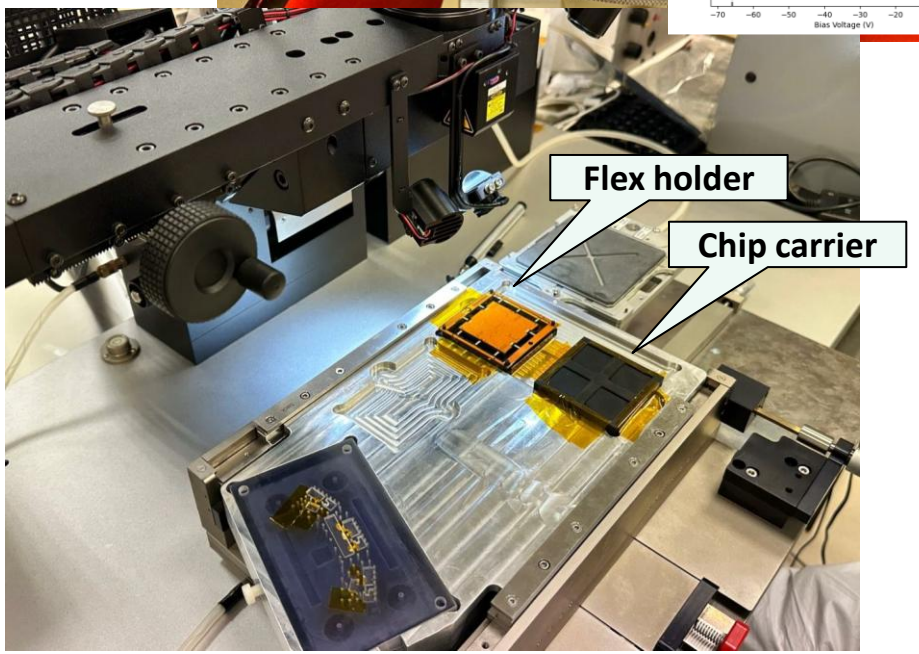


# Module assembly

- I-V test for HV functionality under probe station before assembly
  - failure mode observed during the production of quad modules with direct powering
  - a short on one chip may jeopardize the operation of the other chips in the module
- Finetech pico die bonder
  - used also for the assembly of ATLAS ITk 3D modules
  - manual optical alignment between chips and flex-hybrid
- Araldite 2011 deposited by stamps method on flex backside



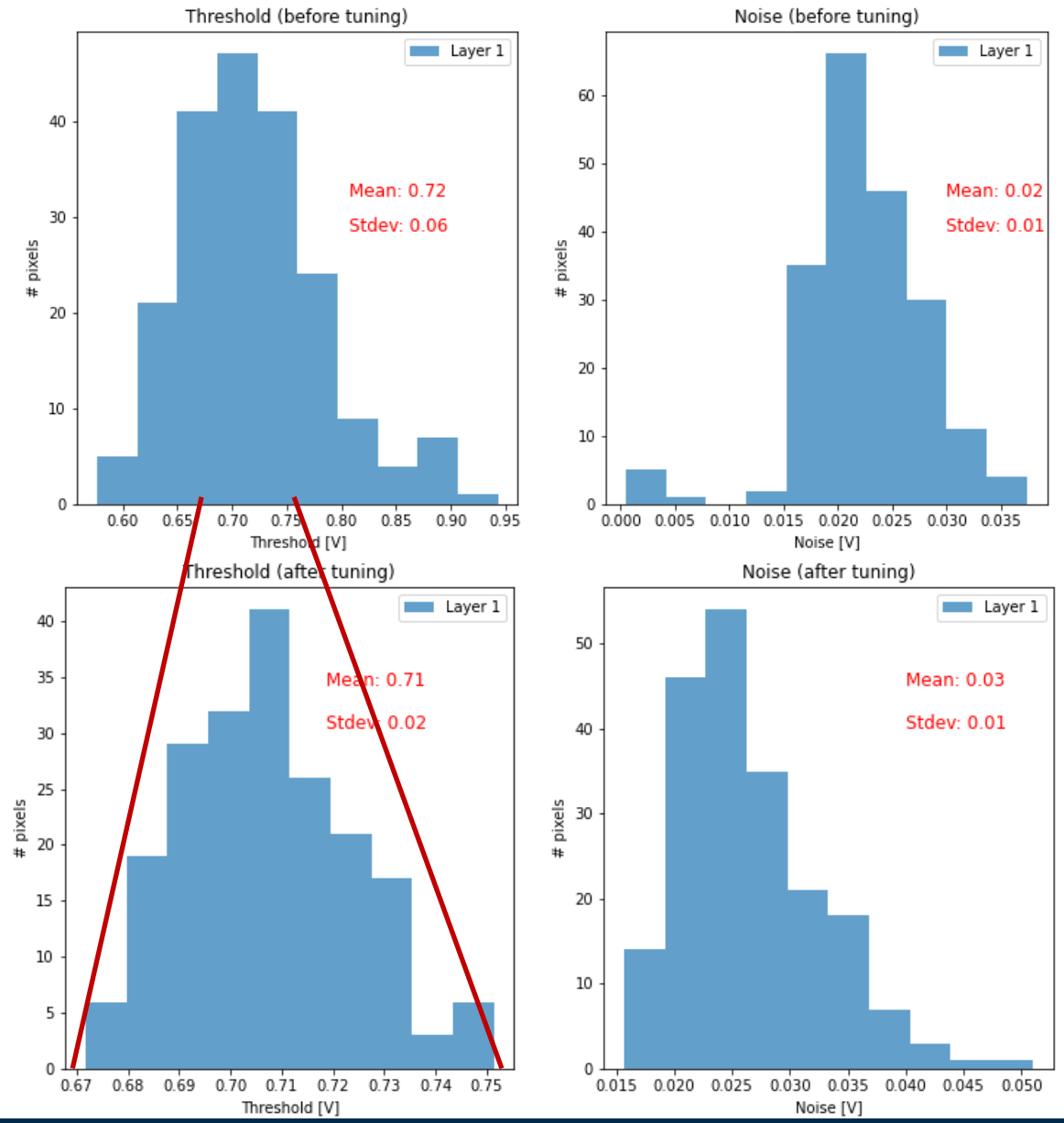



# Threshold Tuning

- Quad module – 3: single wire bonded chip
- Fixed wire bonding diagram  to have proper setting of configuration pins
- Configuration and operation shows the decoupling scheme implemented on the hybrid has good performance

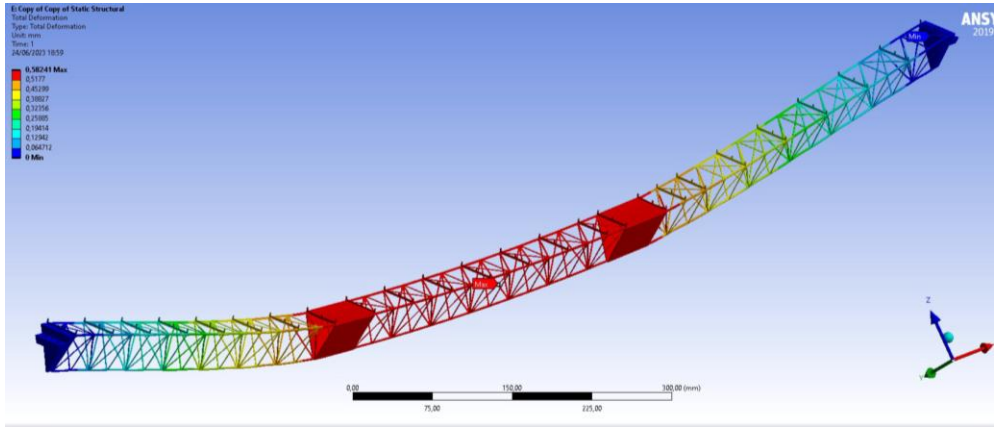
- Threshold and noise measurement using s-curve method
- Threshold tuning by a 3-bit trimming DAC

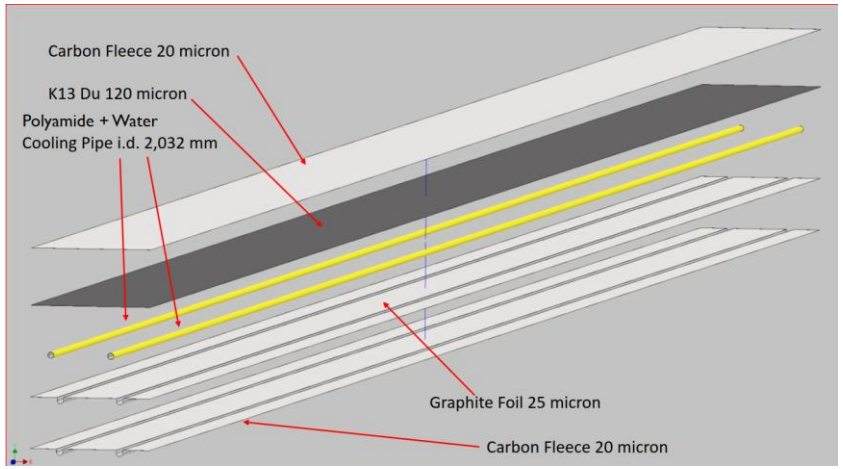
- Performance (on a sample matrix) comparable with operation on a carrier board

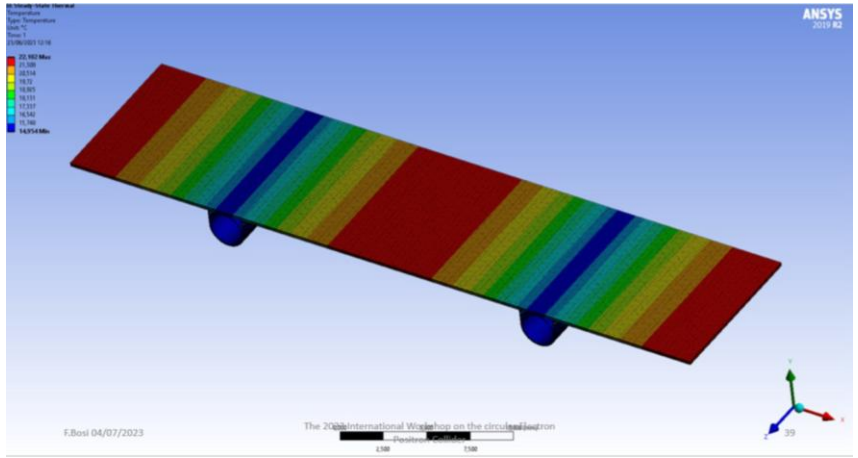


# Low mass mechanical support

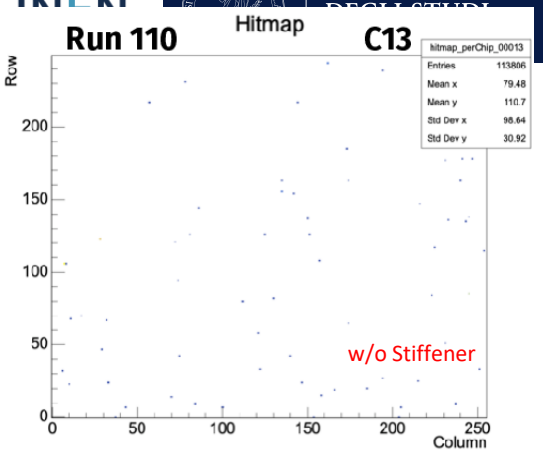
- Low mass stave prototype
  - long barrel layout (1332 mm length)
- Light support structures
  - water jet truss cutting and structure assemblying
  - design checked by FEA
  - support constructed and tested in Pisa
- Low-mass cooling interface
  - carbon cold plate
  - 2 mm diameter Kapton cooling pipes for water cooling

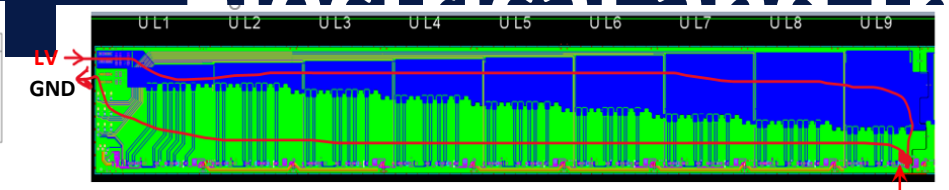


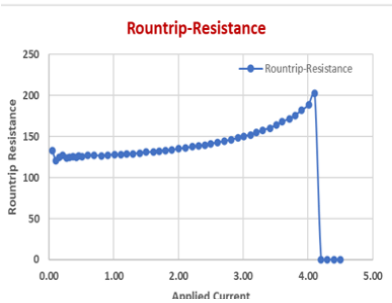


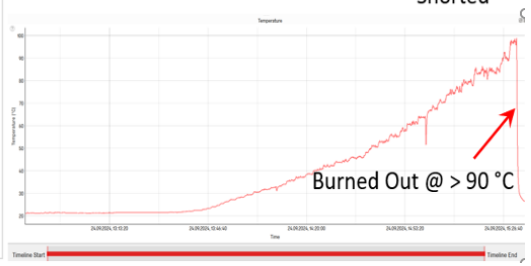



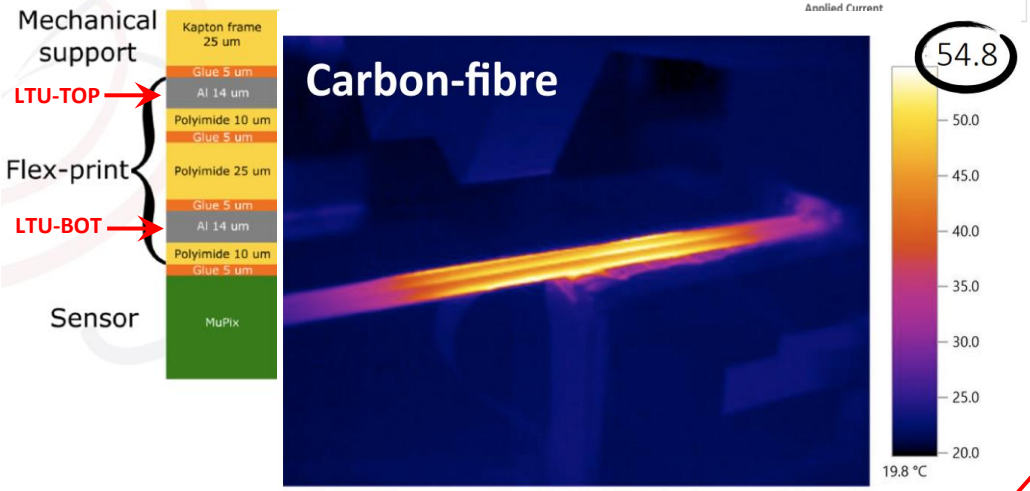
# Electrical and thermal test results

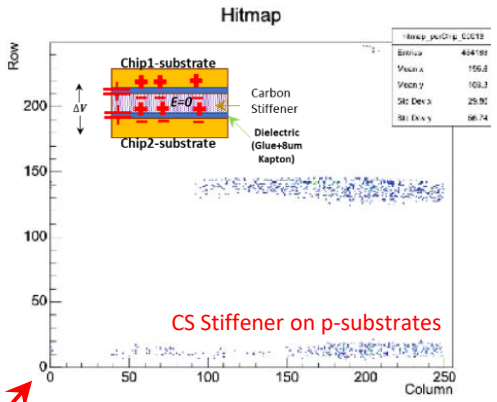


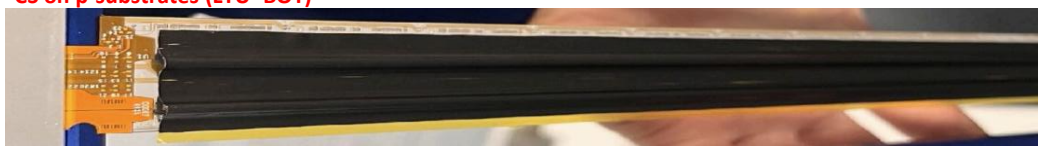



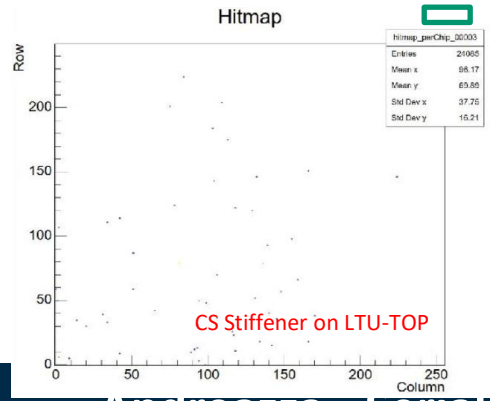




CS on p-substrates (LTU- BOT)



CS on LTU-TOP



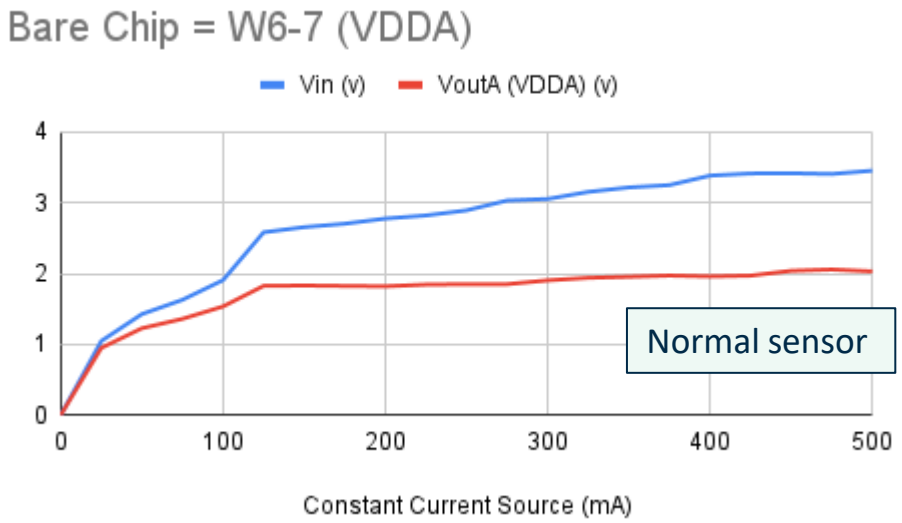

- A ladder is powered into halves with 9 MuPix chips, known as UpStream (US) and DownStream (DS).
- Noise scan at a nominal threshold performed on an electrically functional ladder (w/o stiffener) showed almost no hot pixels on the US side, confirming a reliable 1.25 Gbps operation.
- Power consumption of ~190 mW/cm² per chip corresponds to a current load of ~3.42 A on a half-ladder at an applied voltage of 2 V.
- Round-trip tests show stable resistance up to a 3 A load.
- Burnout tests indicate a critical flex-operation temperature of ~90 °C, beyond which blistering occurs.
- Oxford's current choice of a 25 µm Carbon Stiffener (CS), which is electrically and thermally conductive, can keep the ladder temperature below 60 °C.
- Chip-side (LTU-BOT) CS integration on chips' P-substrates can introduce capacitive HV-noise coupling if the potential difference (ΔV) exists in applied HV on US and DS nodes.
- Flex-side (LTU-TOP) CS integration may instead lead to additional bounce-back noise and cross-talk if glue is on high-speed lines. (due to impedance degradation)
- Tests with carefully dispensed glue on the LTU-TOP side for CS integration show no observable noise pattern.

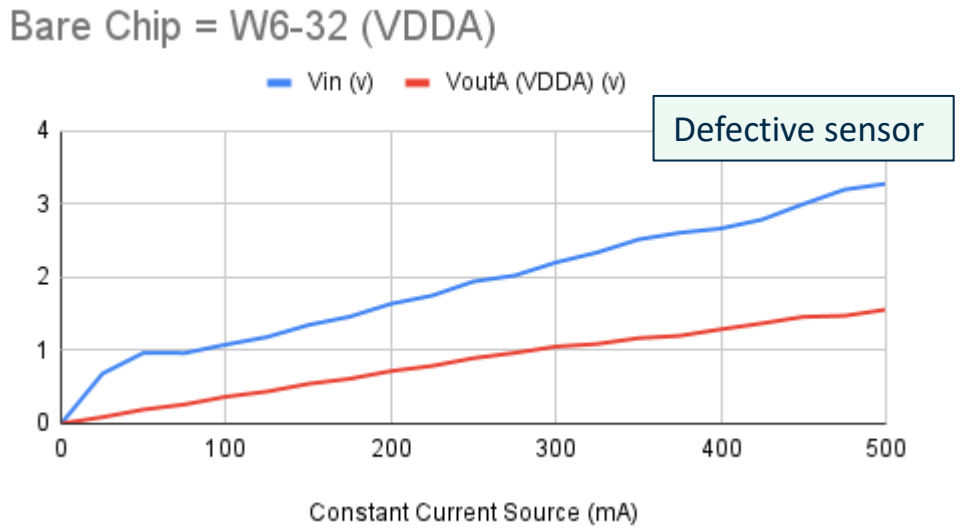
# ATLASPIX3.1 Wafer 6 Probing

- Initial probing setup was not testing correctly the VDDD regulator: needle configuration changed in March

- The **VDDA** is regulated at 2.1 V after ~250 mA input current
- The **VDDD** is regulated at 2.1 V after ~150mA input current
- Large voltage drop is an issue of the testing setup (long cable and needle contact resistance)

- Tested all chips from wafer #6
  - 11/48 show anomalous behaviour
  - Large sensor power consumption
  - Does not turn on even at rather high bias currents
  - Chip selection critical since module yield is chip yield to the 4th power

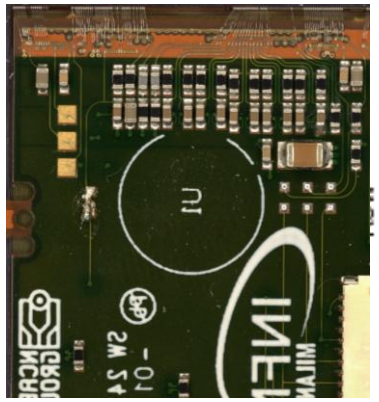


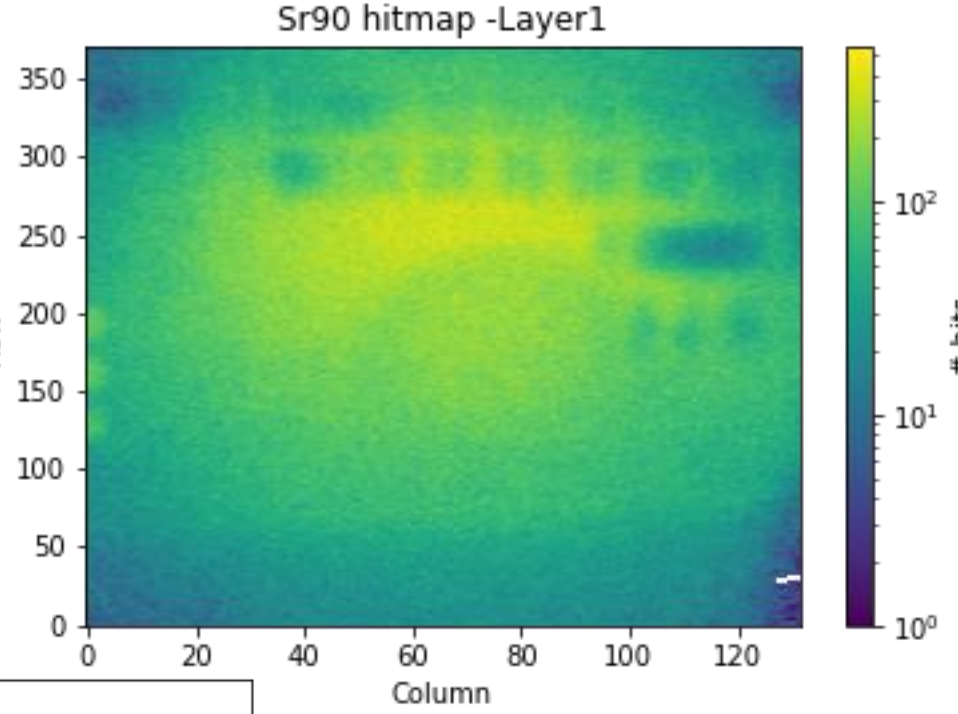



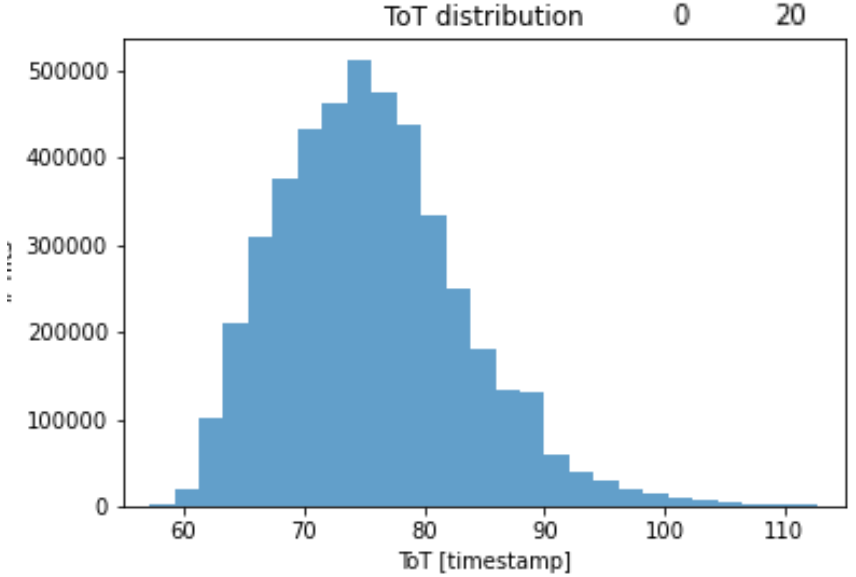
# Source Scan

- Quad module – 3: single wire bonded chip
- Fixed wire bonding diagram  to have proper setting of configuration pins
- Configuration and operation shows the decoupling scheme implemented on the hybrid has good performance

- Measurement with $^{90}$Sr beta source
- Full 132x372 pixel matrix
- Pulse height measurement with ToT





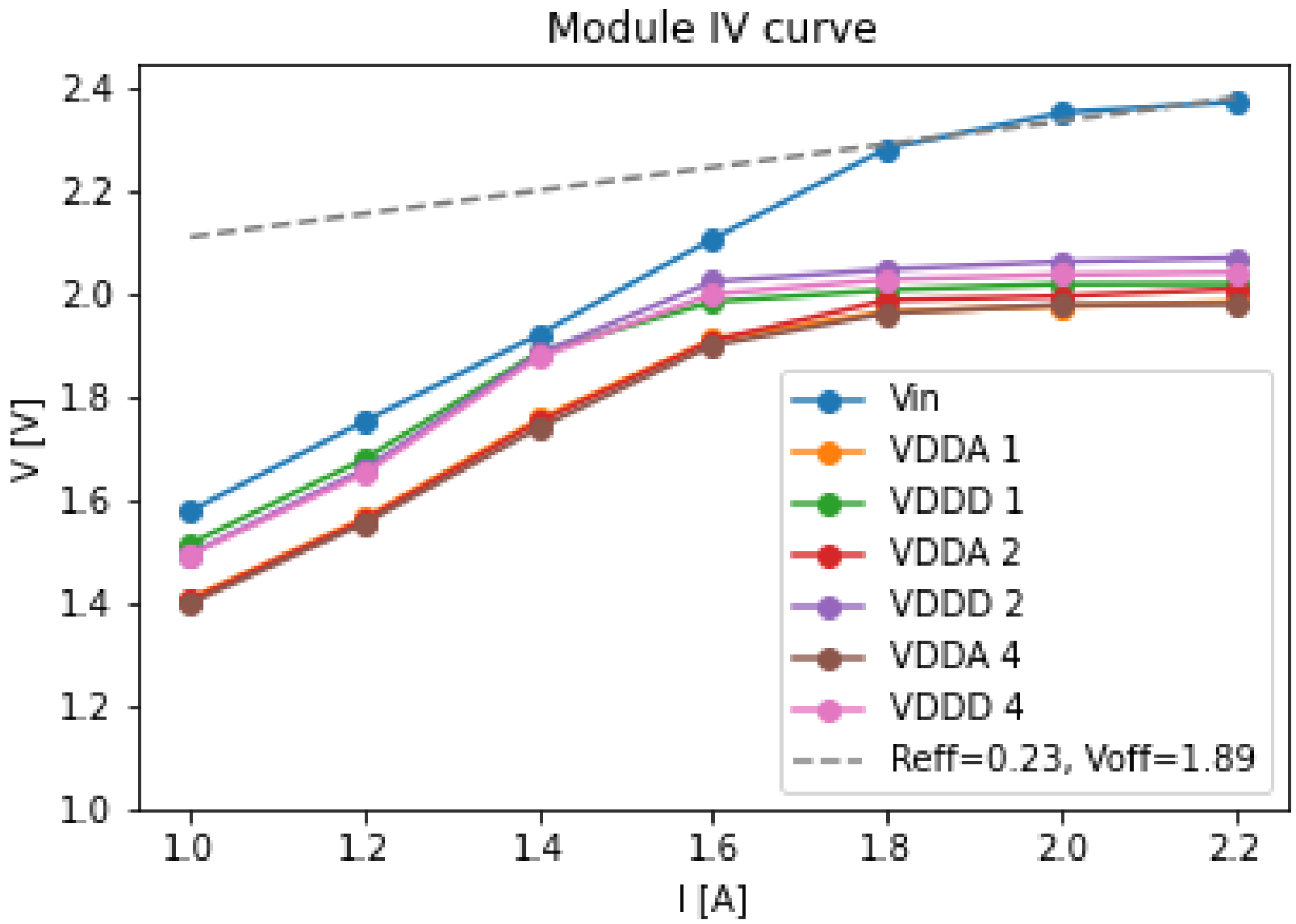
# Risk assessment (What if...?)

- **LF submission will not provide suitable chips**
  - hold some ATLASPIX3.1 chips till result of submission is known
  - perform stage 2 with P2Pix sensors
  - "digital modules" using RD53 pixel chips for HL-LHC (no physical signal, electrical only test – too high power consumption)

- **Do not get INFN funding for FBK flexible PCB production**
  - build module flex with standard wire bonding technique
  - explore another vendor

# Si tracker: system considerations

- **Complete system consists of 900'000 cm² area / 4 cm² chip = 225k chips (56k quad-modules)**
  - aggregation of several modules for data and services distribution is essential
  - inner tracker will be 5--10% of this
- **Data rate** constrained by the inner tracker
  - average rate $10^{-4}$ - $10^{-3}$ particles $cm^{-2}$ $event^{-1}$ at Z peak
  - assuming 2 hits/particle, 96 bits/hit for ATLASPIX3
  - **640 Mbps link/quad-module** (assuming local module aggregation) provides ample operational margin
  - 16 modules can be arranged into **10 Gbps fast links**: **3.5k links**
    - can also assume 100 Gbps links will be available: 350 links
- **DAQ architecture**
  - **triggerless readout** will fit the data transmission budget but requires off-chip re-ordering of data
  - **triggered readout** will be **simpler** and would also reduce the bandwidth occupancy
- **Power consumption**
  - ATLASPIX3 power consumption **150 mW/cm²**
  - 600 mW/chip → 2.4 W/module → **total FE power 130 kW**
  - additional power for on detector aggregation and de-randomizations **~2W/link**


Module IV curve
V [V]
I [A]
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
1.0
1.2
1.4
1.6
1.8
2.0
2.2
Vin
VDDA 1
VDDD 1
VDDA 2
VDDD 2
VDDA 4
VDDD 4
Reff=0.23, Voff=1.89