NAPA: nanosecond timing pixel for future colliders

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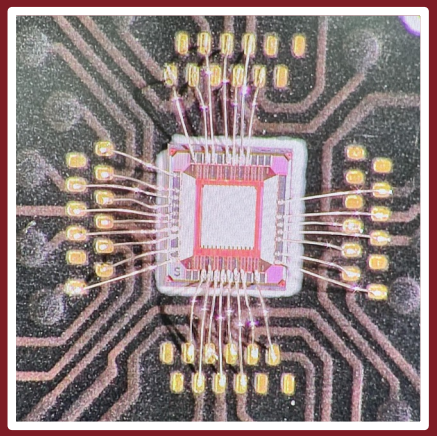


U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

NAPA - MAPS focus at SLAC

At SLAC we have a long time interest in MAPS technology (beyond HEP, XFEL…)

- Last few years of developments have been focused on applications for future detectors at e+e-
  - Cost effective solution for high granularity tracking and calorimetry
- Part of CERN WP 1.2 collaboration and now DRD7 working on TPSCo 65nm

Focus on long-term R&D, targeting simultaneously:

- ~ns timing resolution
  - beam induced background suppression (IPC)
- Power consumption compatible with large area and low material budget
- Fault-tolerant circuit strategies for wafer-scale MAPS

Highlights:

- 1st SLAC prototype on TPSCo 65nm (2023) as part of a CERN WP1.2 shared run
  - NAPA_p1: NAnosecond Pixel for large Area sensors – Prototype 1
- 2nd SLAC prototype on TPSCo 65nm (2025) as part of a CERN WP1.2 shared run

Next steps:

- New design combining O(ns) timing precision and low-power (2024/2025).
- **Next 2-3 years:** design of a wafer-scale ASIC (design only)

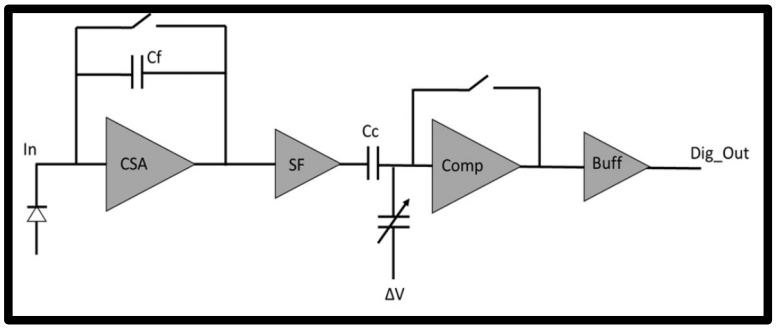
NAPA-p1 Design

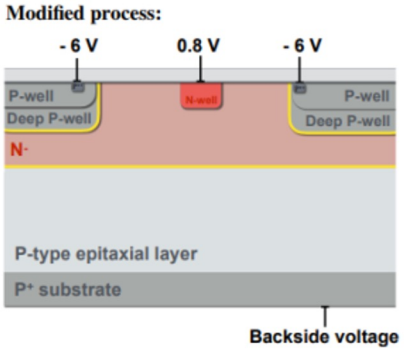
Nanosecond timing **P**ixel for large **A**rea sensors- **p**rototype**1**

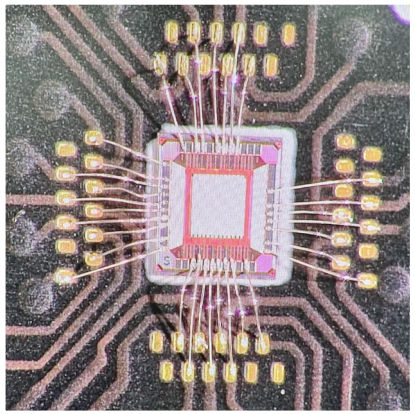
SLAC prototype submitted with CERN WP1.2 in Tower Semiconductor 65 nm technology

- The chip has total area of 1.5 mm x 1.5 mm, with a 24 x 24 matrix of pixels with pitch 25 um.
- Synchronous architecture with CDS helps reduce low-frequency noise and allowing minimum size transistors.
- Power pulsing reduces average consumption

Acknowledgement: Gained a lot of experience testing DPTS with ALICE(testbeams, irradiation, and climatic chamber tests). Demonstrated technology choice, confirming <5 μm spatial, >99% efficiency, even after ITS3 irradiation targets (10 kGy + 10^{13} n_{eq}/cm^2).





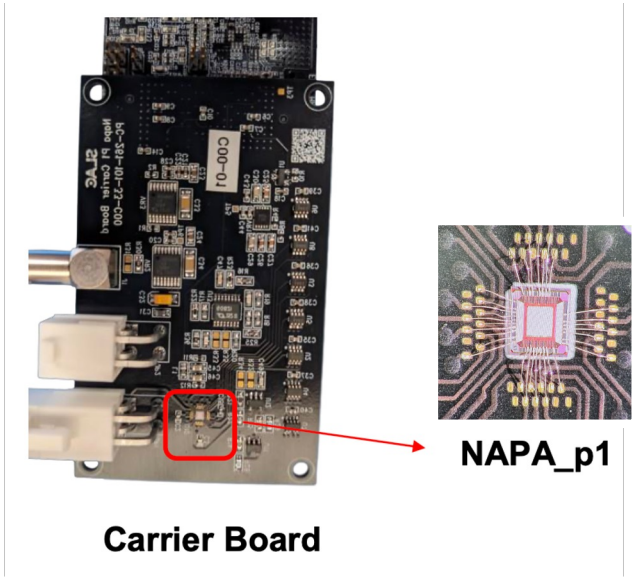


JINST 19 (2024) 04, C04033

Test Setup

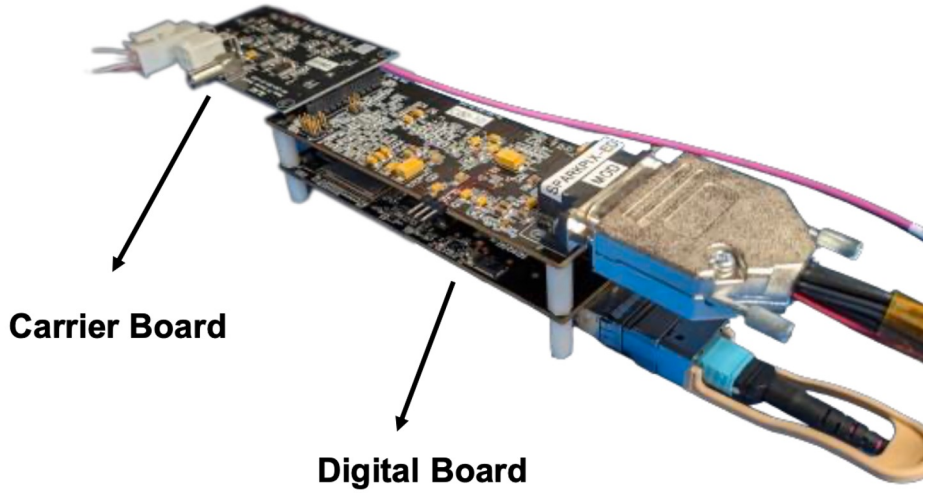
The chips were wire bonded at SLAC and a custom carrier was designed to provide all analog references.

- Digital board with FPGA and several DACs
- Wire bonded at SLAC
- Configurable threshold settings: 0 to 7



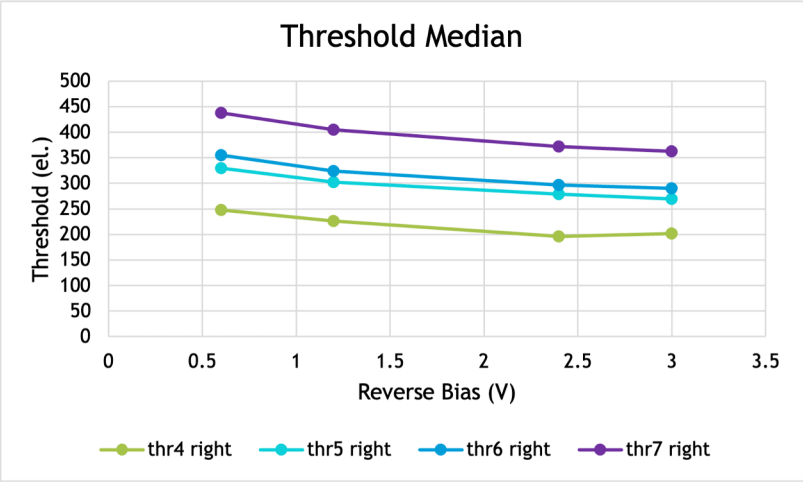
	Specification	Simulated NAPA-p1
Time resolution	1 ns-rms	0.4 ns-rms ✓
Spatial Resolution	7 µm	7 um ✓
Noise	< 30 e-rms	13 e-rms ✓
Minimum Threshold	200 e-	~ 80 e- ✓
Average Power density	< 20 mW/cm^2	0.1 mW/cm^2 for 1% duty cucle ✓

Simulations show it is possible to achieve specifications, assuming a low duty cycle machine.



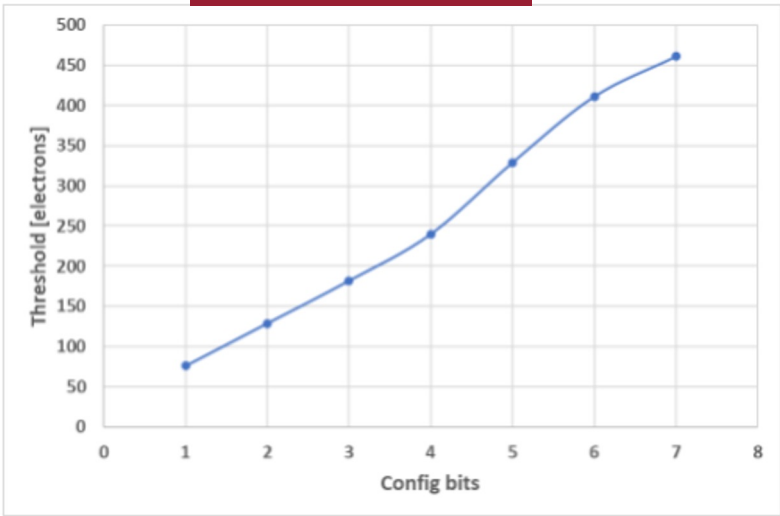
Pixel Front-End Characterization

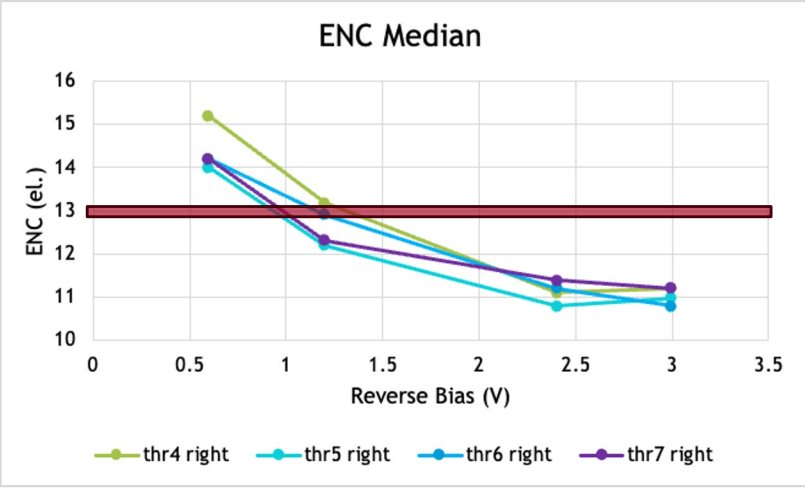
Testing



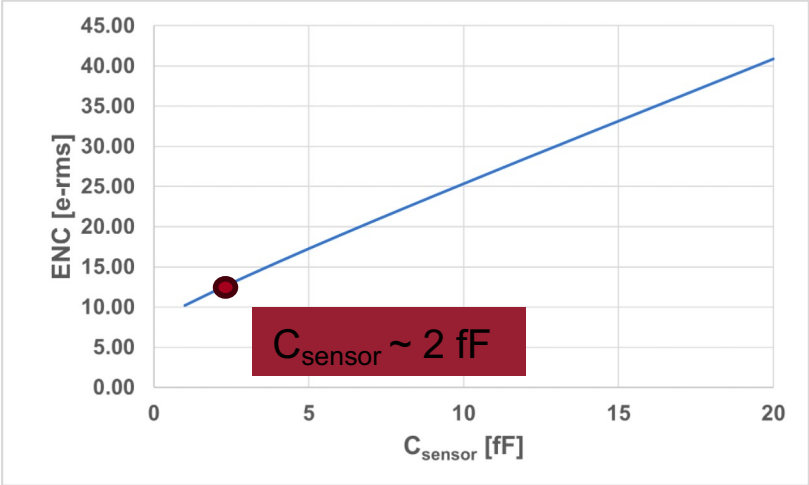
As expected, decreasing the configurable threshold or increasing the bias voltage leads to smaller threshold and ENC.

Simulation

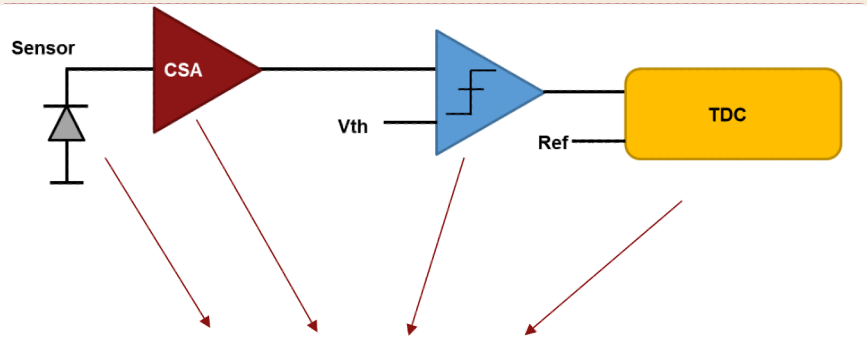




Front end characterized over various threshold and reverse bias. Data generally agrees with simulation.

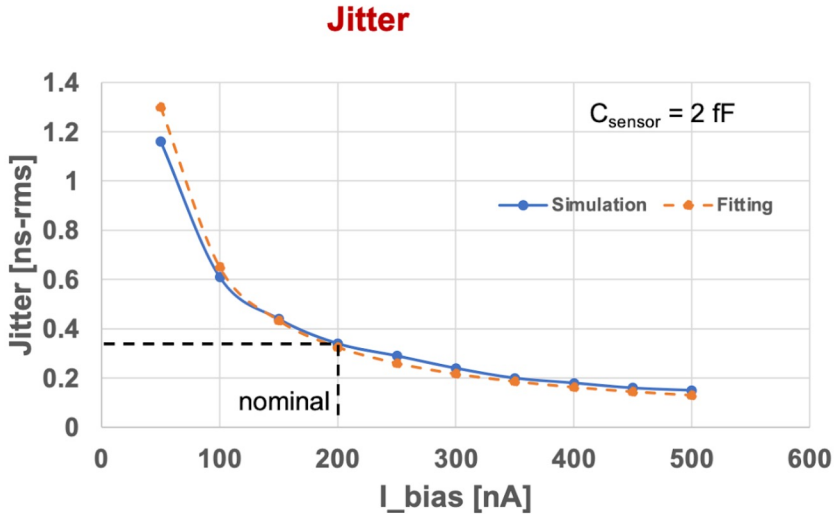


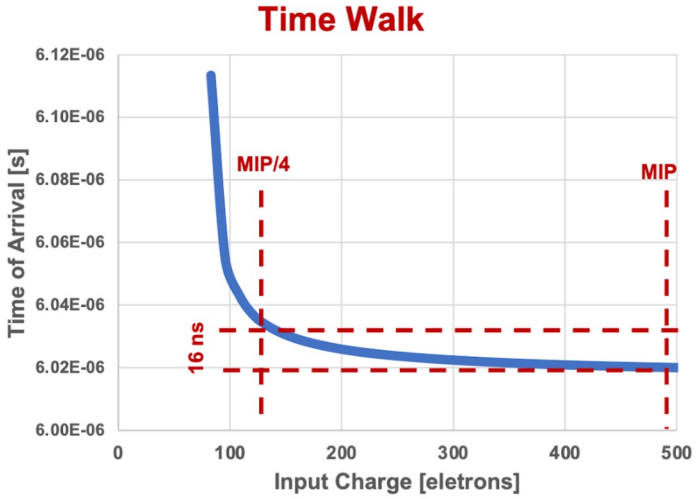
Timing Limitations



$$\sigma^2_{Total} = \sigma^2_{TOA} + \sigma^2_{FE} + \sigma^2_{Timewalk} + \sigma^2_{TDC}$$

- Time-walk can be corrected with TOT (currently not implemented in circuitry)
- TDC and TOA <150 ps-rms
- **Focus on FE jitter**; achieving timing while **maintaining power constraints is limiting factor.**

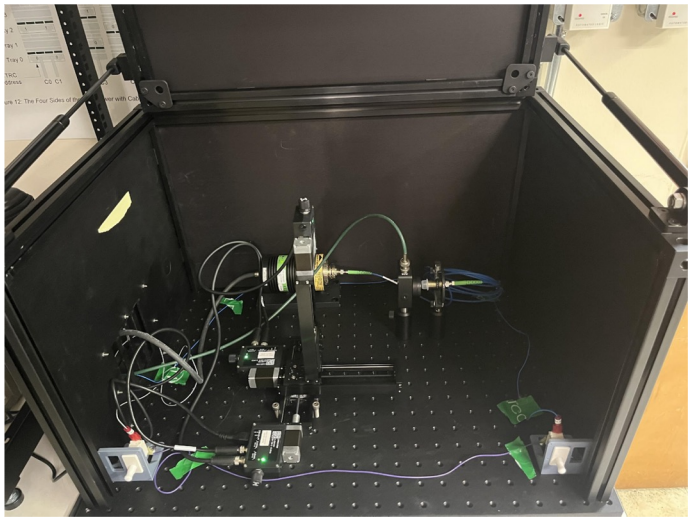


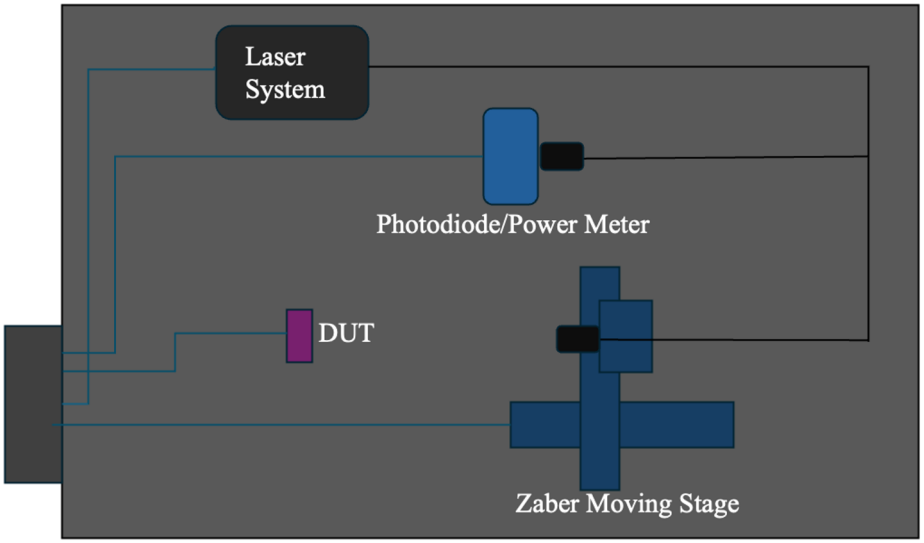


Laser Setup

Currently setting up pulsed laser for timing and efficiency measurements, to **compare to simulation**. Should start testing by end of the year.

- 1080 nm laser, collimator-micro focus optics to focus to ~6 μm. Pixel pitch is 25 μm.
- Measurements: in-pixel efficiency, time-walk, jitter.

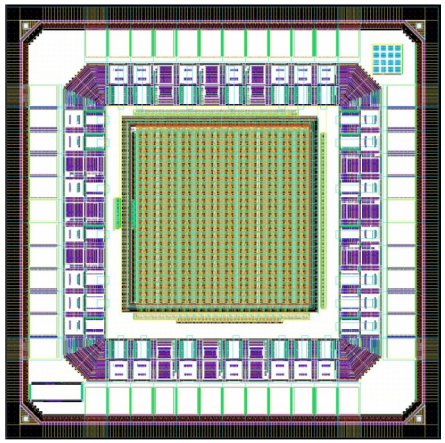




NAPA_p2

Prototype submitted in CERN ER2 run to further study timing and power trade off. In particular, want to integrate a compact, low power TDC into MAPS prototype.

- Napa-p2 contains a **Vernier delay line**, with a programmable time resolution down to 20 ps. **Building block of TDC**.
- Designing remaining part of TDC and engaging with DRD3/7 on how to integrate TDC into a pixel design.



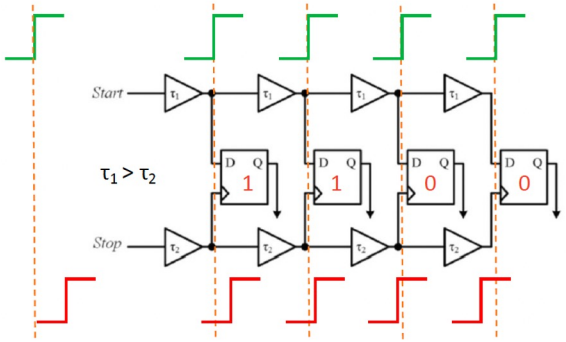
Napa-p2

TDC Design

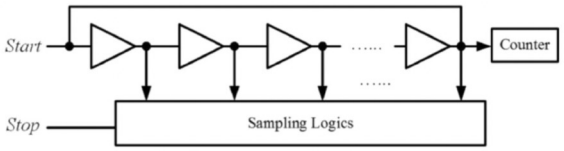
TDC Architecture:

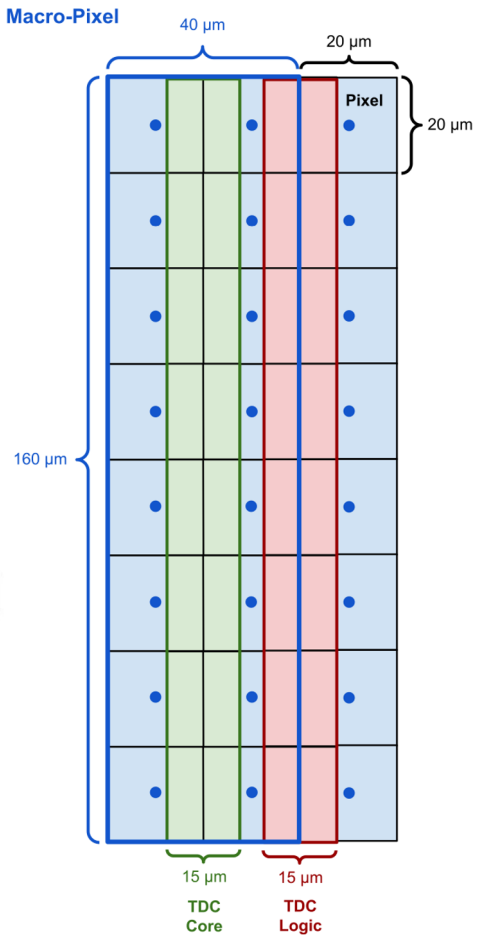
- **Vernier Delay line:** high resolution (τ_1-τ_2)
- **Ring Oscillator:** large dynamic range with counter

Vernier Delay Line



Ring Oscillator (RO)





Macro-Pixel: Multiple pixel analogue FE connected to one TDC

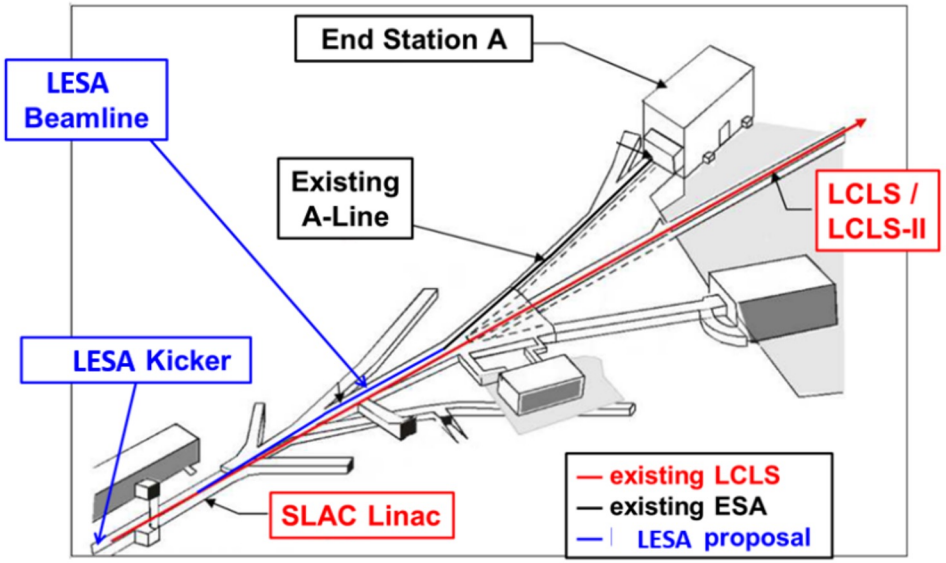
- Need to optimize the macro-pixel size TDC layout

More Details: CPAD, DRD7.6 Meeting

Looking ahead : LESA Facility

Linac to End Station A (LESA) beamline is being constructed at SLAC targeting operation in **2027**:

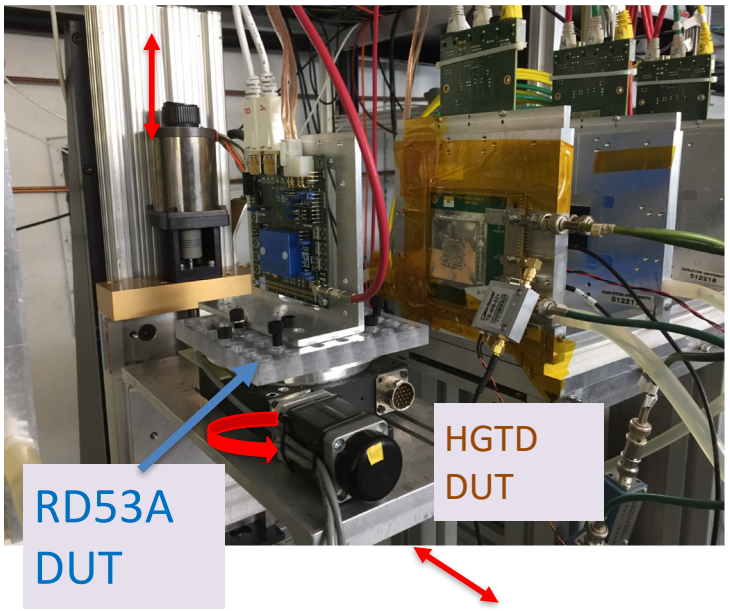
- Electron beam at 8 GeV
- User determined beam rate up to 37.1 MHz (27 ns)
- User determined # e^-/bunch
- Bunch spacing up to 10 Hz



- 6-8 campaigns a year with possible optimization across different efforts within HFCC & DRDx
  - As early as end of 2026.
- 1-2 weeks each

This new facility will enable beam validation of future MAPS prototypes (including NAPA)!

Current setup: Caladium EUDET Telescope + DUT



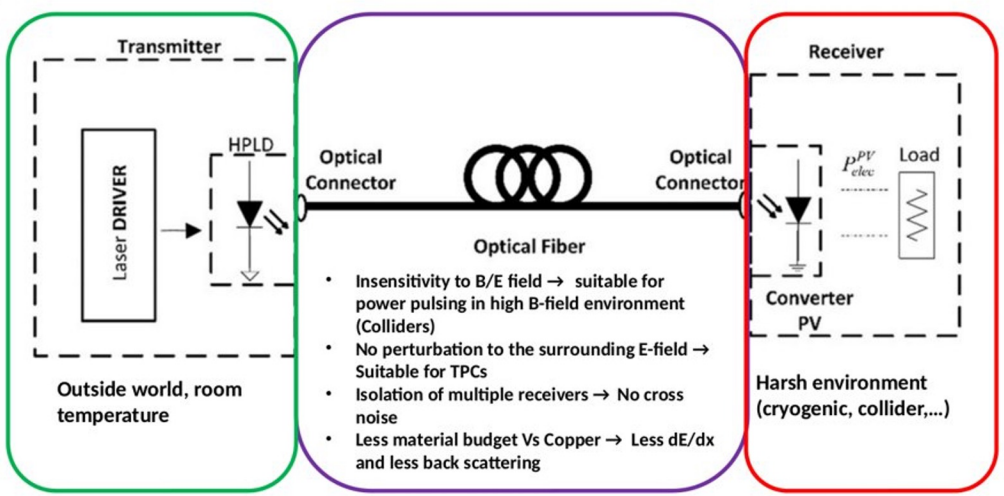
- **Caladium EUDET telescope** resident at ESTB since Dec/2015,
- Loan from Carleton University, **Thomas Koffas,** supporting/operating the telescope
- EUDET: 6 planes of CMOS MIMOSA-26 (up to ~10KHz trigger)
- 18.5x18.5µm pixels, X*Y aperture ~2x1 cm and **~3µm spatial resolution.**

- Augmented by remote controlled movers
- Overall XY stage for telescope+DUT
- Dedicated DUT XY & rotation stage (new: mounting electrical insulation)

Power over Fiber

New effort at SLAC targeting various experimental applications

- Power over Fiber (PoF) offers an innovative solution by delivering power through optical fibers, which are immune to electric and magnetic fields, and boast 1000X lower thermal conductivity compared to coax.
- **We are developing radiation-hardened photonic links that can be used in future e+e- collider environments, where radiation levels can exceed 100 krad.**
  - **At SLAC this development is led by the DUNE group**
- This approach will investigate advanced photovoltaic materials like perovskites and their potential to surpass current GaAs-based photodiodes in power-to-weight ratio and radiation tolerance.



Conclusions and next steps

- **Pulsed laser setup** will demonstrate **timing** and efficiency performance shortly. Napa-p1 simulations achieve 350 ps-rms.
- **Napa-p2** submitted with **TDC test structure** which should arrive and be characterized in early 2026.
  - Should achieve O(100) ps jitter.
- Besides NAPA :
  - Integrated test stands to test power over fiber with MAPS
  - At SLAC we plan to get started with vertex geometry optimization studies (and services distribution)
    - close synergy with MDI interests in the accelerator group and our BIB expertise
  - **LESA test-beam facility** at SLAC, expected in 2027, will enable **beam-based validation** of future MAPS prototypes

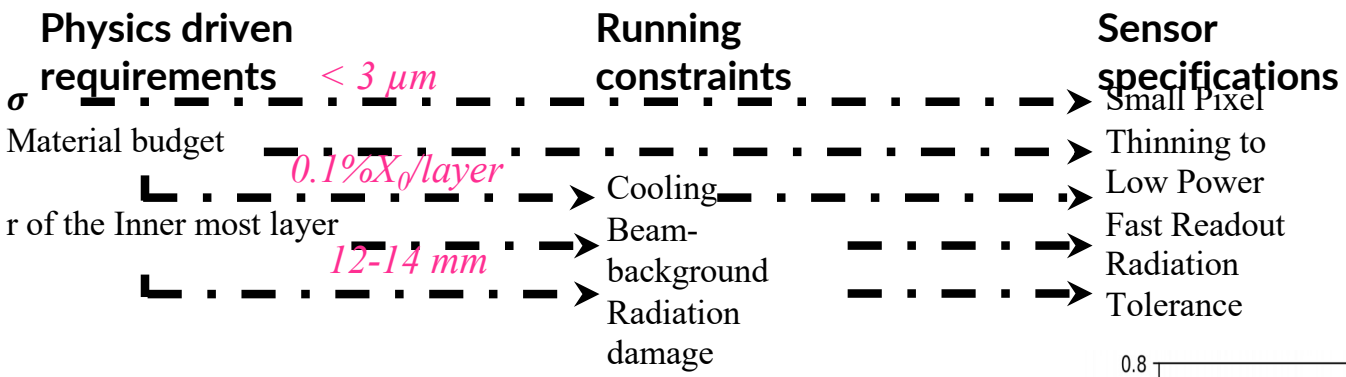
Additional material

Sensors technology requirements for Vertex Detector

Services cables + cooling + support make up most of the detector mass

Need new generation of ultra low mass vertex detectors with dedicated sensor designs

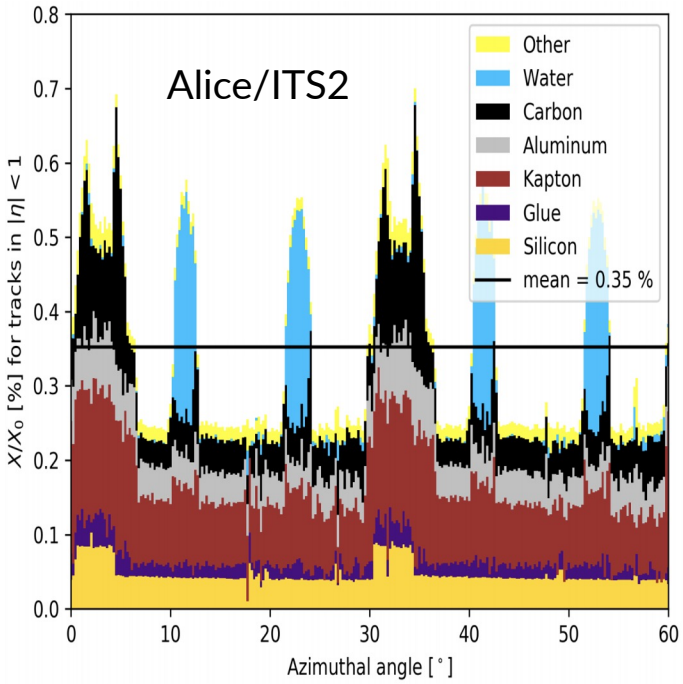
CERN-LHCC-2019-018



Dig 10μm or Analog 15-20μm
50 μm
20-50 mW/cm²
~1-10 μs
10 MRad, 10^{14} n_{eq} / /cm²

Serial Powering and Optical powering could further reduce the impact of the services

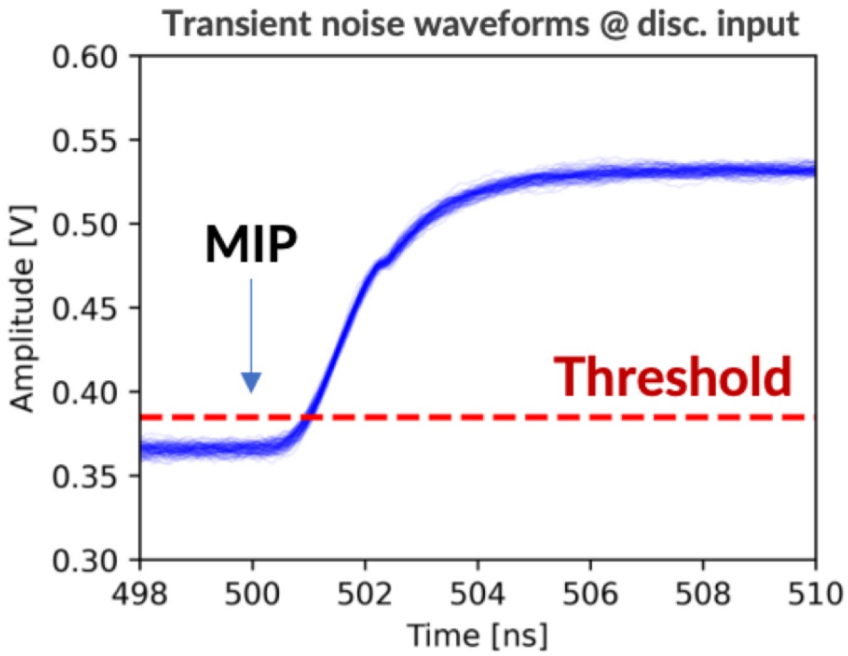
Sensor's contribution to the total material budget is 15-30%



Pixel front-end optimization

Pushing the timing resolution and better understanding of the power consumption

- Developed a more complete numerical simulation, including:
  - ENC from noise, bandwidth and noise shaping
- Digital signal from multiple front-ends sent to one TDC
  → "macro-pixel"
- Preliminary simulation results of pixel front-end:
  - ENC: 16 e-
  - Jitter: 36.8 ps
  - Current: 2.6 μA
  - Timewalk: 3 ns → "gating" accuracy of 15±3 ns
- Note that:
  - TOT not yet included,
  - It assumes 1 ns rise time for typical signal
- Power consumption estimated to be ~1W/cm^2
  - Timing resolution of ~40ps
  - Assuming 3 μW/pixel for the analogic component



For nsec timing resolution, power budget is within our target

Needs cont'd

Telescope - possible updates - SBU interested in a MALTA update

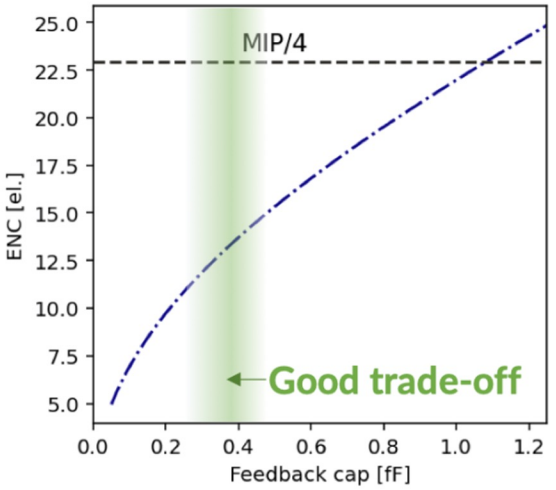
- Malta (36µm pitch, 25 ns) plane (3 available) as timing reference to improve track finding at higher intensities
  - Open to collaborating on an HFCC telescope with new technologies: can help with test, integration, DAQ/TLU, operations.

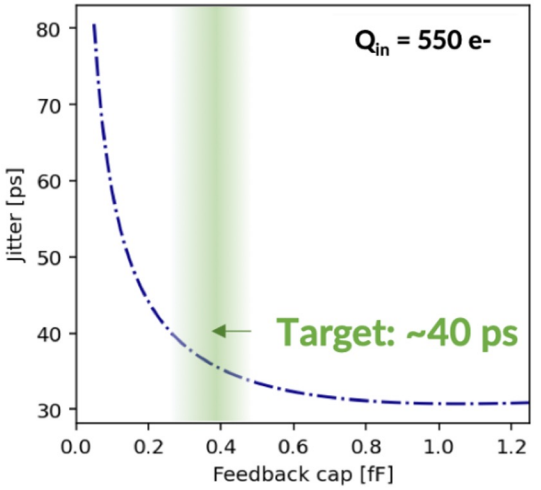
- 6-8 campaigns a year with possible optimization across different efforts within HFCC & DRDx
  - As early as end of 2026.
- 1-2 weeks each

V. Dao, G. Piacquadio (SBU)

Pixel front-end: timing optimization

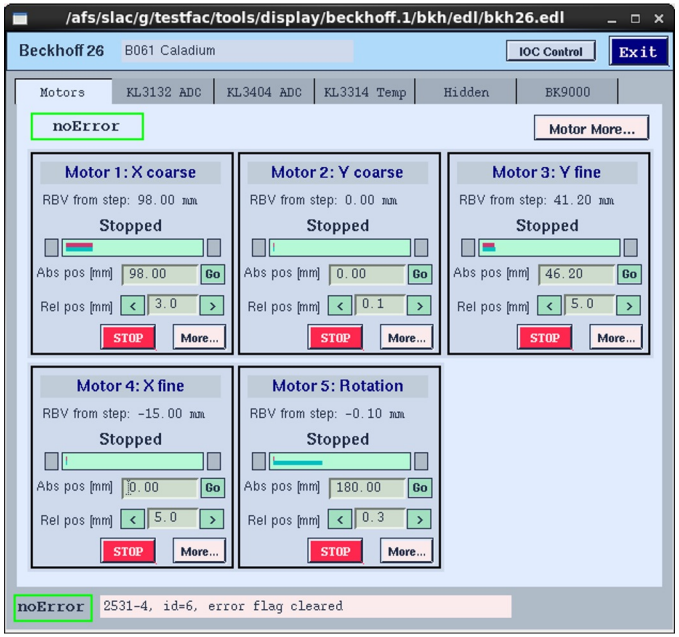
- Developed a more complete numerical simulation, including:
  - gm / power
  - ENC from noise, bandwidth and noise shaping
  - Discriminator noise
  - Threshold set to 6 × ENC
- Assuming 3 µW/pixel, simulations shown on right :
  - ENC versus C_{FB} → upper limit to feedback capacitance
  - Jitter versus C_{FB} → expected 1/ C_{FB} trend, with minimum
- Not shown, but equally important:
  - Lower C_{FB} → ↓ amplitude at CSA out → ↑ threshold dispersion
    → ↑ discriminator gain



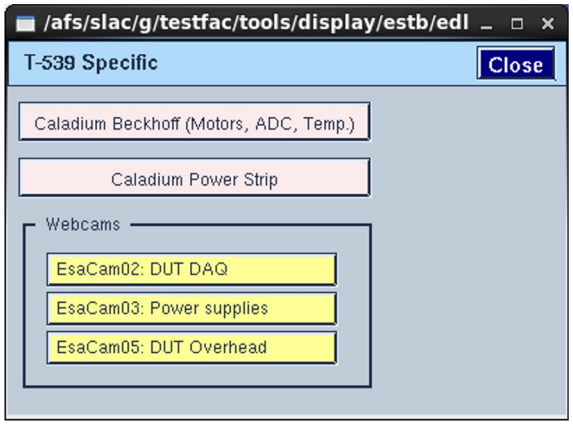


ESTB infrastructure

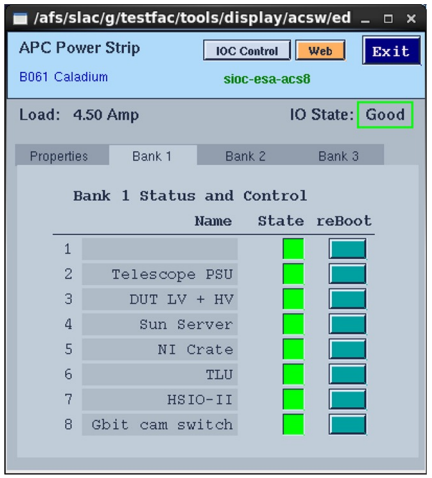
EPICS supported by SLAC Test Facilities



XY stage control & temperature probes



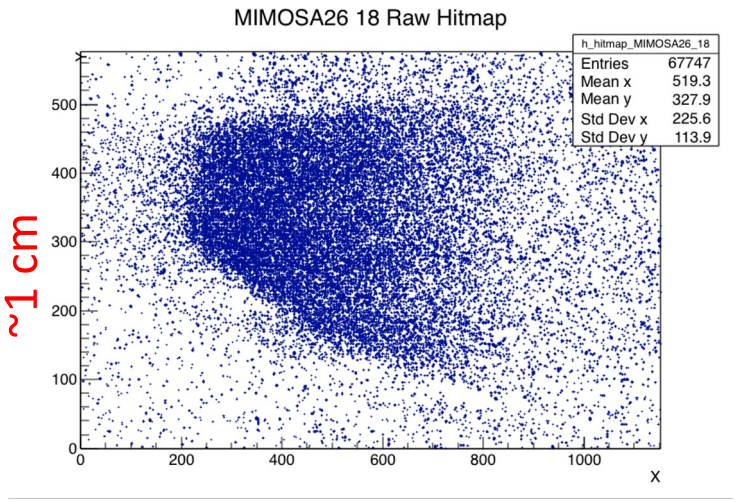
Web cams



Remote power control

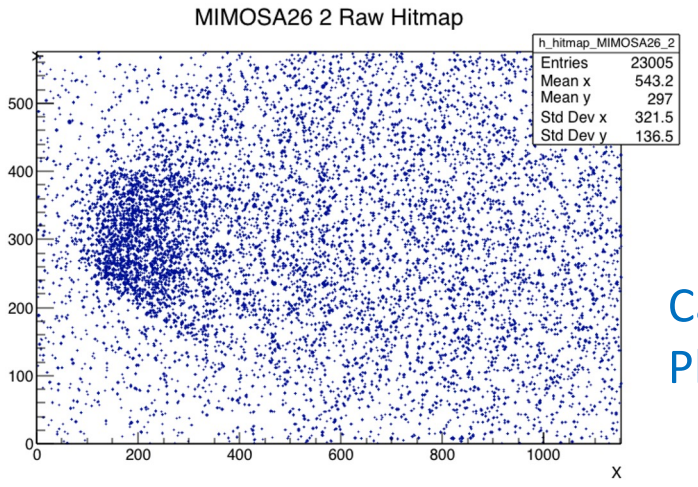
Beam Spot (from Su Dong, 2017)

~30 e/evt



~1 cm

~7 e/evt

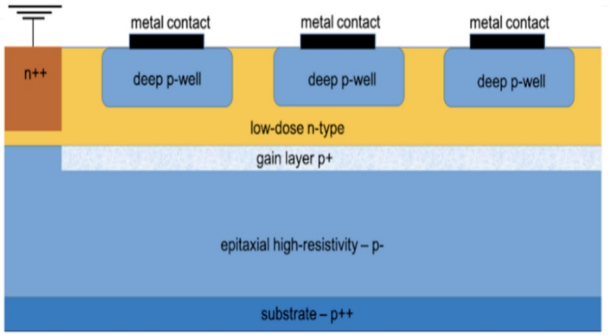


Caladium Plane 2

~2 cm

- Requested MCC to uniformly spread beam in 2x1 cm aperture
- Bulk of quality data taken at ~7 e/event to keep track density within reconstruction capability
- Rate and beam position can jump when LCLS changing primary beam energy

Interest from US FCC community



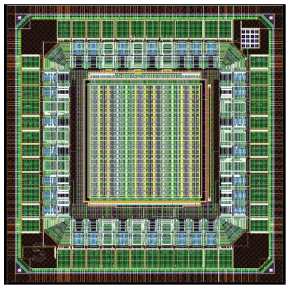
1. **LGAD-based detectors, for timing layer (FNAL/BNL)**
   few kHz particle rates

1. **MAPS sensors with spatial resolution < 3µm**

(Interest also from Alice ITS3, for large stitched sensors)

- **NAPA MAPS sensors with ns timing capability (SLAC)**
  1.5mmx1.5mm test structure

3. ETROC, **Future Precision Timing Detectors (FNAL)**
   - **1x1cm size, highest intensities**



4. **Scintillator based detectors** for radiation protection studies
   < 1 particle per pulse at different rep rates

Common needs:

- Large band-width oscilloscope with multi-channels, fast digitizers, fast triggering systems
- Remote controlled motion table, dry air supply, chillers, low and high voltage power supplies
- tracking telescope - see next slide