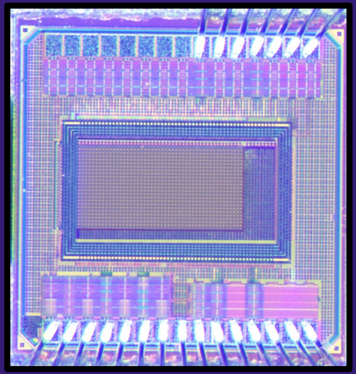


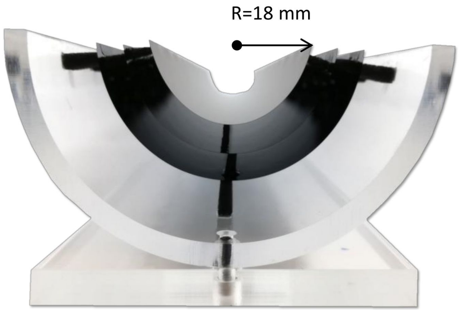
Characterisation of the CE-65v2 MAPS test structure

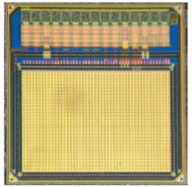
[FCC Vertex Detector Workshop - 30/10/2025]

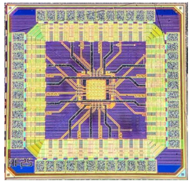
Eduardo Ploerer on behalf on the CE-65 team

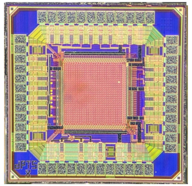
ALICE ITS3 and the TPSCo 65nm Process

- ➔ **ALICE Inner Tracker System upgrade (ITS3)** will be installed during LHC LS3 from 2026-2028
  - ◆ 3 inner layers of ITS2 MAPS will be replaced by **fully cylindrical** inner layers
- ➔ Fully cylindrical layers rely on stitching on 300mm wafers available in the **TPSCo 65 nm CMOS imaging process**
  - ◆ Smaller feature size allows denser logic, reduced power consumption
- ➔ First submission for test structures **MLR1** in December 2020
  - ◆ Small-scale prototypes: APTS, DPTS, **CE-65**
- ➔ Second submission for large stitched sensors (MOSS, MOST) **ER1** in 2022
  - ◆ Learn and study properties of stitched sensors
  - ◆ Evolution of some MLR1 prototypes, including **CE-65v2**



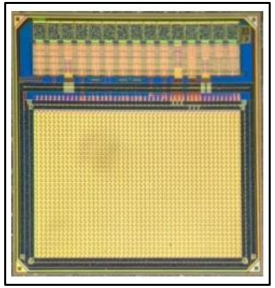

CE-65

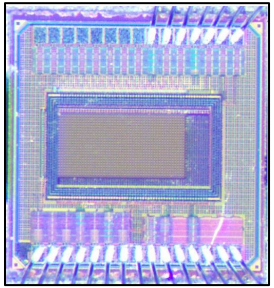

APTS

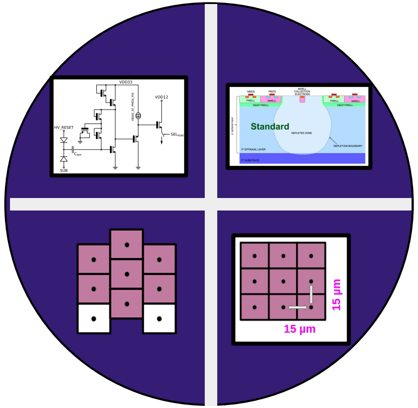

DPTS

CE-65 test structures: two generations, four design axes

- “Circuit Exploratoire”
  - Developed by IPHC Strasbourg
  - Implemented in **65nm TPSCo CMOS process**
- **Analog** rolling shutter readout
- Two generations
  - CE-65v1 (MLR1)
    - 64x32 (48x32) pixel matrix
  - CE-65v2 (ER1)
    - 48x24 pixel matrix
- Four design axes
  - Amplification Scheme: AC-amp., DC-amp., SF
  - Process variation: Standard, Modified, Modified w/ Gap
  - Pitch variation: 15 µm, 18 µm, 22.5 µm
  - Matrix geometry: square vs staggered







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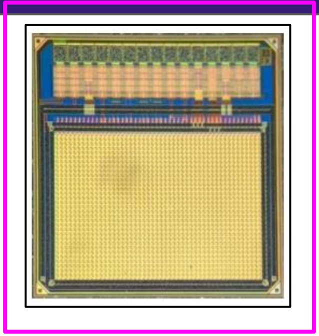

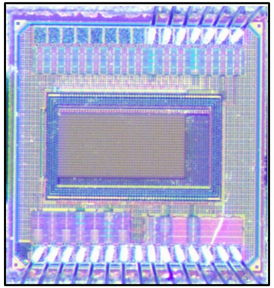

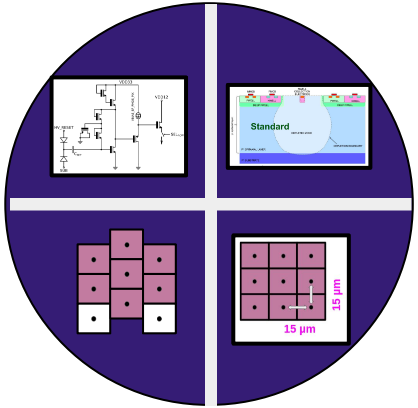

CE-65 test structures: two generations, four design axes

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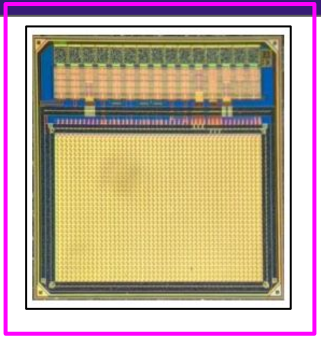

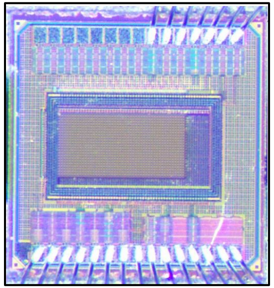

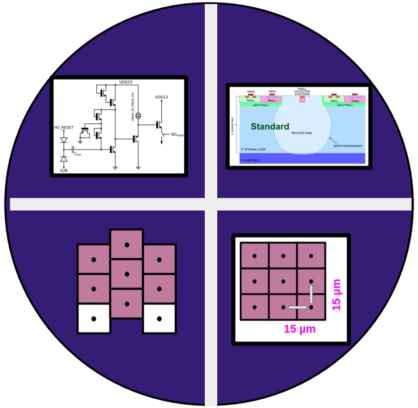

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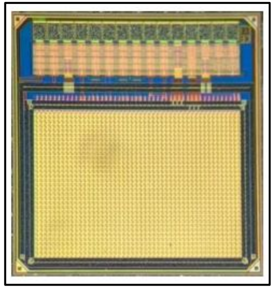

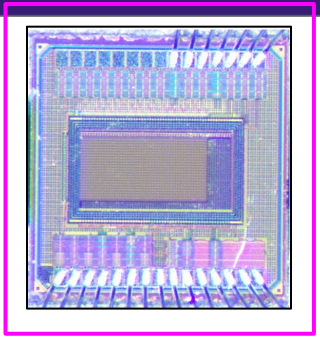

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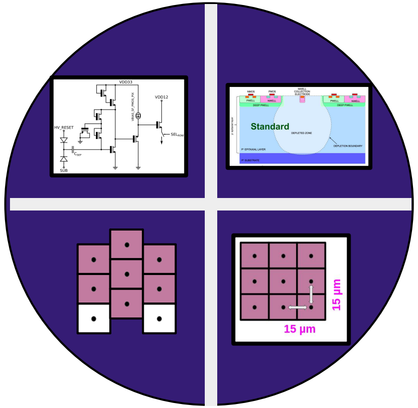

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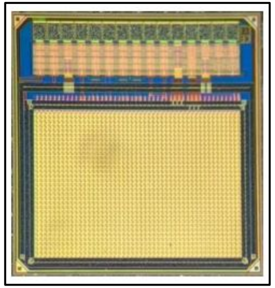

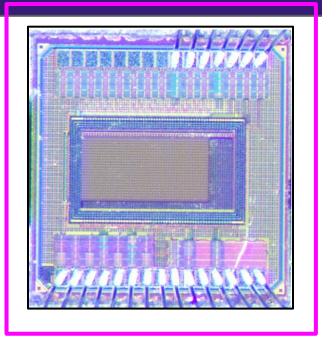

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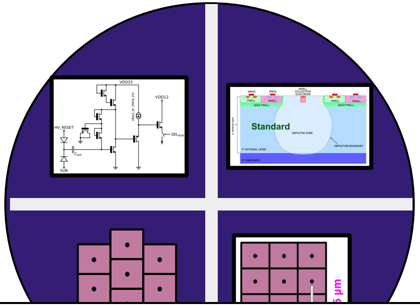
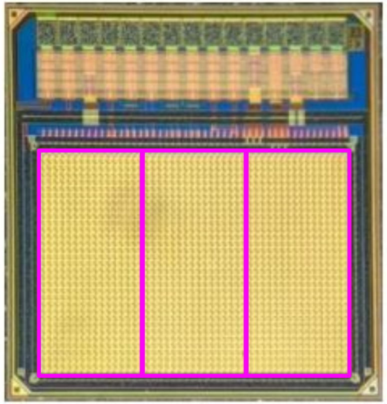


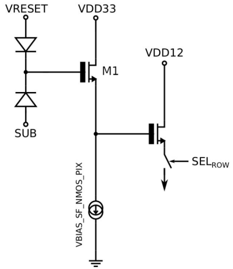
Goal:

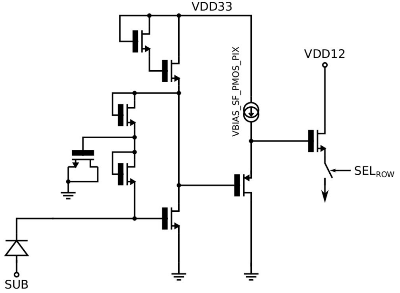
- ➔ **Validate** 65nm TPSCo CMOS process
- ➔ Target ultimate **spatial resolution** along four **design axes** as input for future MAPS test structures

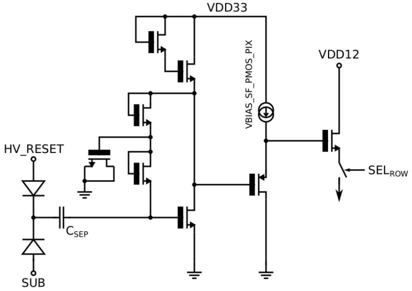
Looking Back: CE-65v1

- ➔ CE-65v1 chip implemented in 3 different **amplification schemes**
  - ◆ Source-follower
  - ◆ DC-preamp.
  - ◆ AC-preamp.
- ➔ Motivations for AC-coupling include
  - ◆ Depletion voltage can exceed supply voltage
  - ◆ Full depletion without substrate back-bias
  - ◆ **But**, reduced gain from parasitic capacitance
- ➔ During lab tests AC-preamp. emerged as most performant









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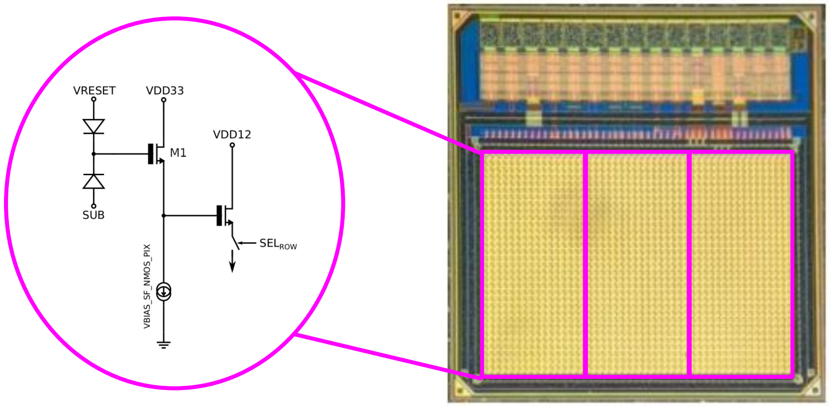

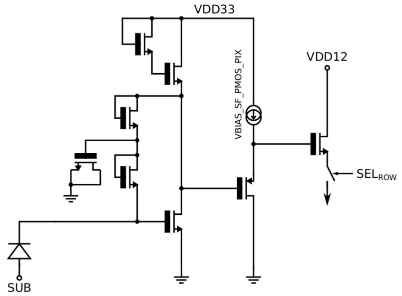

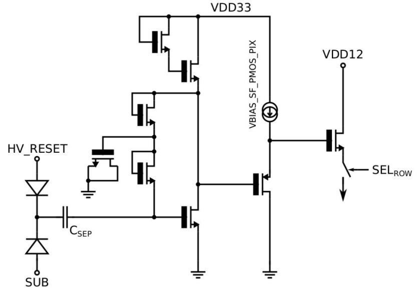

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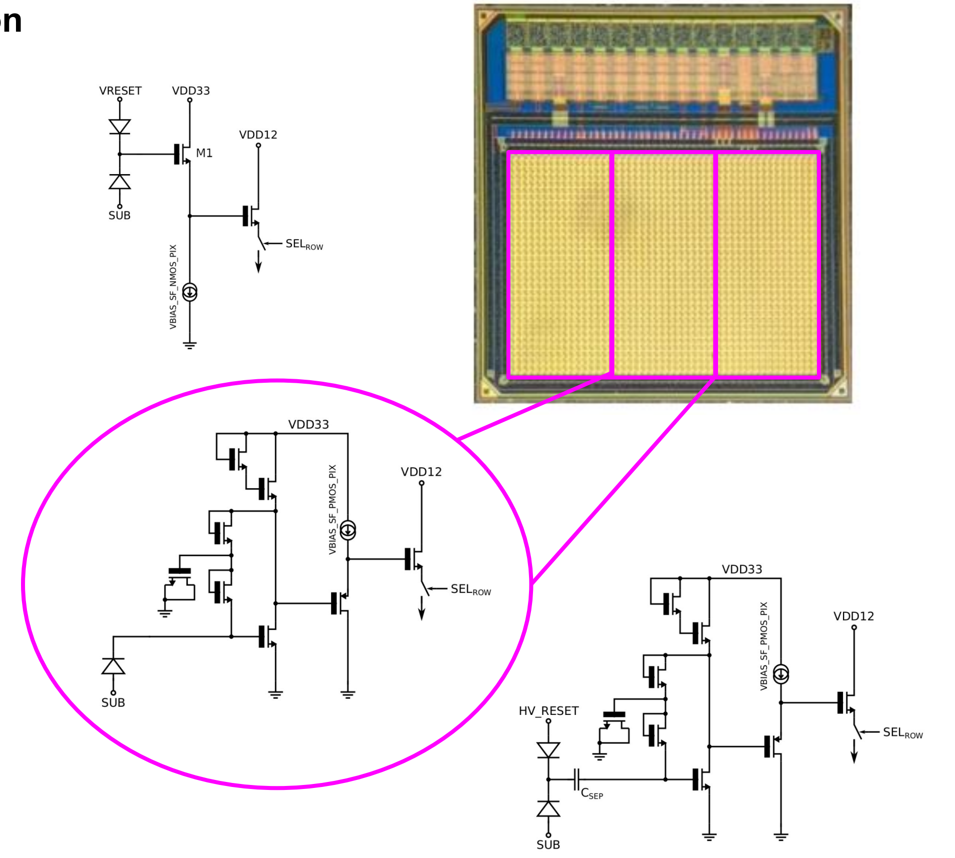

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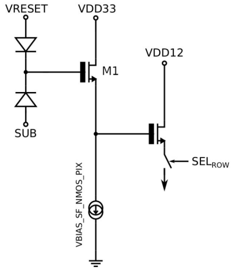

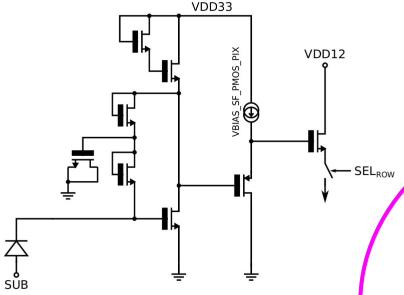

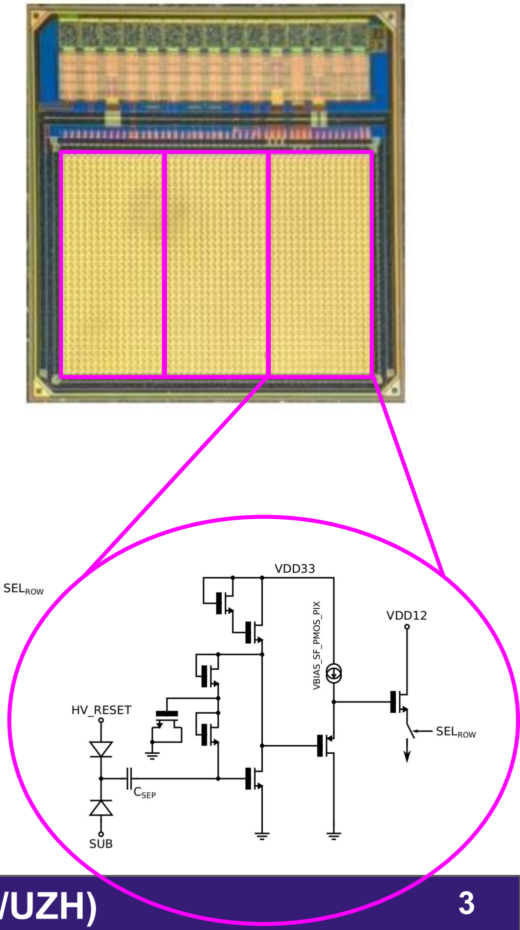

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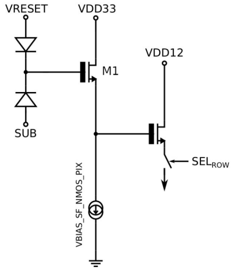

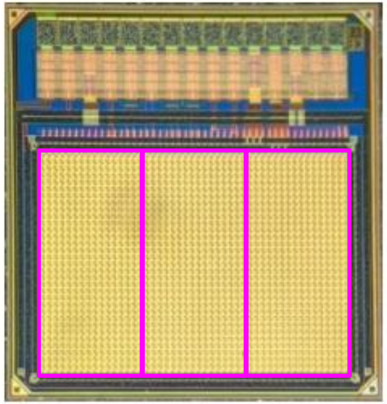

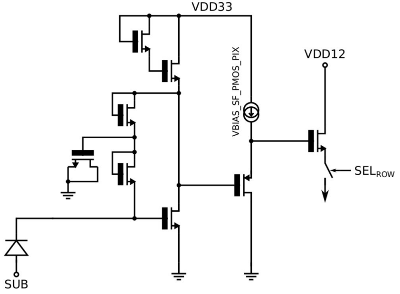

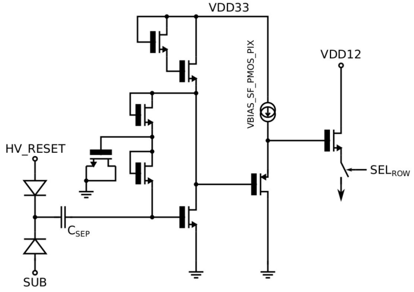

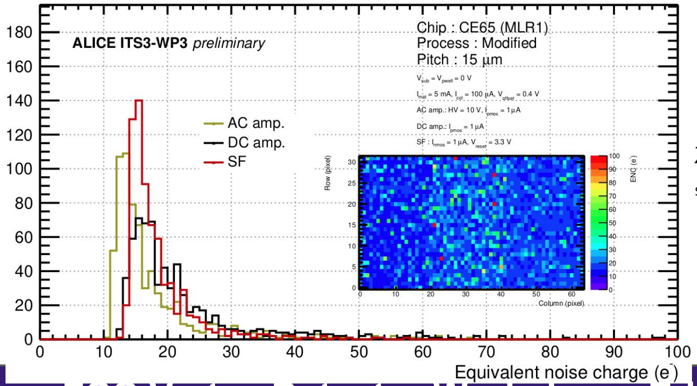

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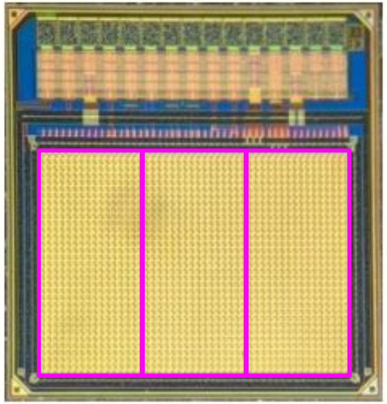
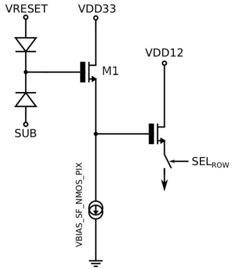
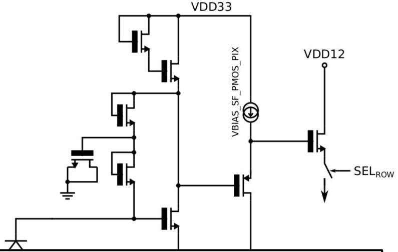
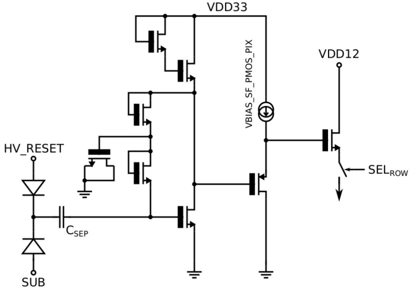
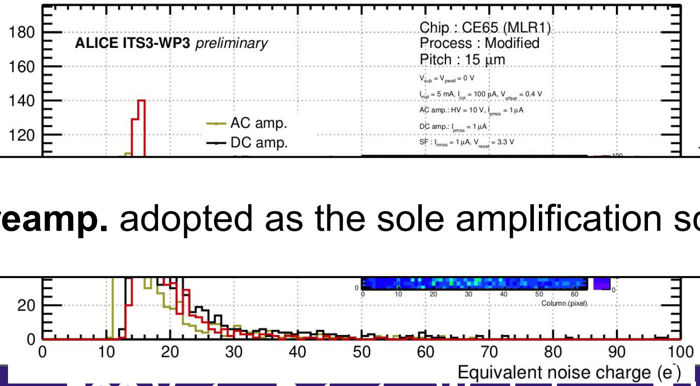




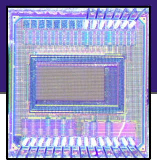


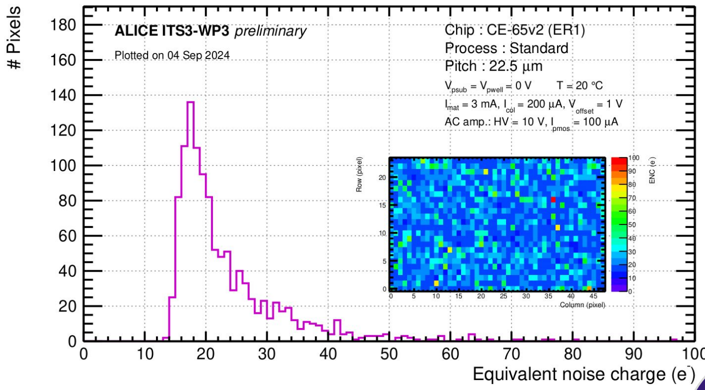




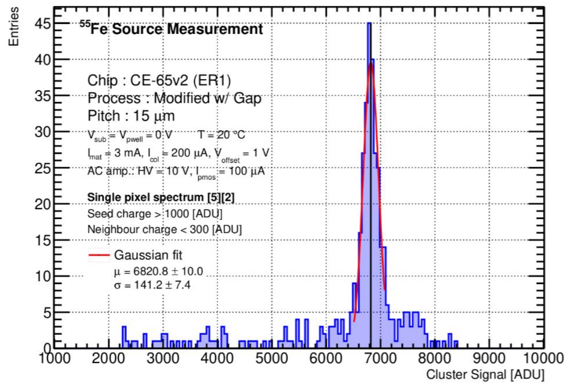
➔ **AC-preamp.** adopted as the sole amplification scheme for **v2 chip**

CE-65 Characterisation: Lab tests + Testbeam measurements





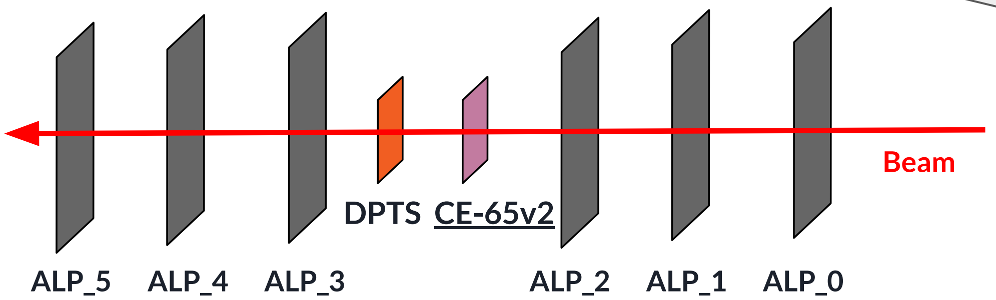
- ➔ Noise measurements in absence of signal
- ➔ Width of noise distribution defines performance



- ➔ Pixel gain calibrated from Fe-55 peak

Strategy

- ➔ Chip response to MIPs at test beam
- ➔ Testbeams at SPS + DESY



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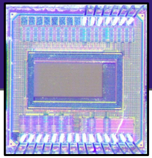

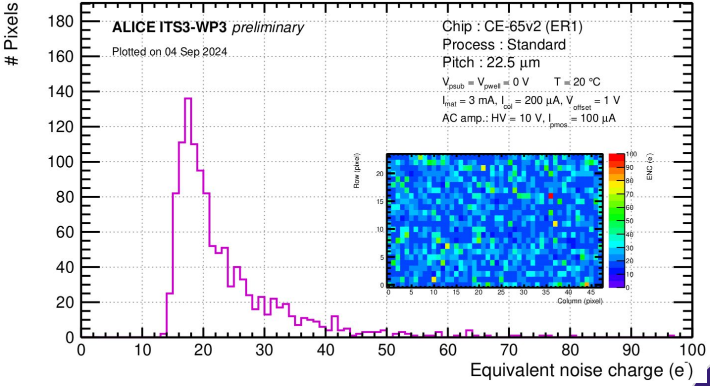

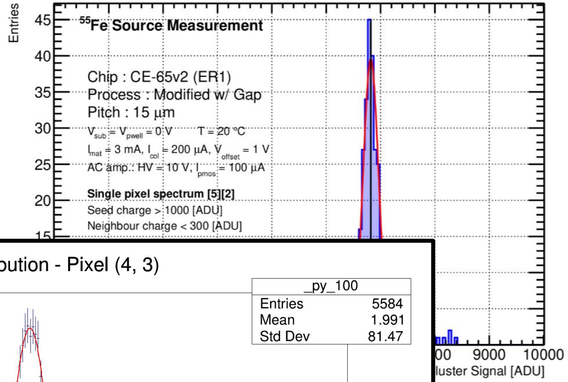

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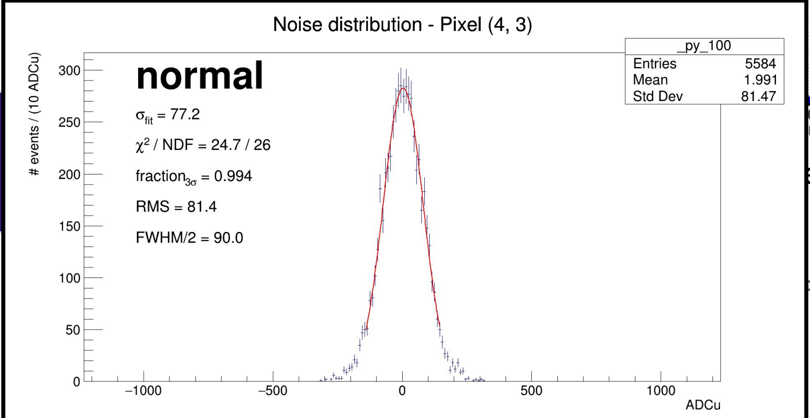


➔ Chip response to MIPs at test beam

➔ Testbeams at SPS + DESY

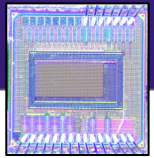
ALP_5

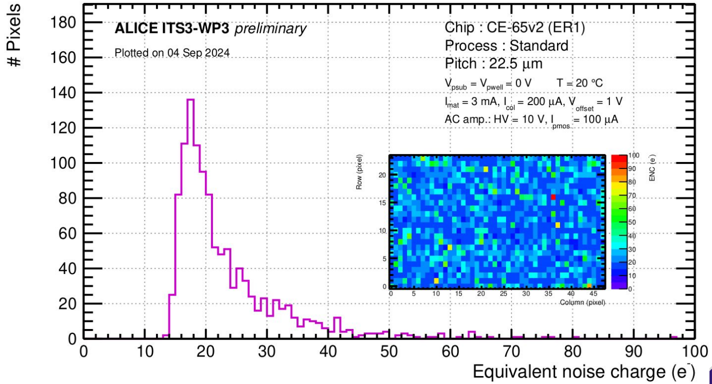
am

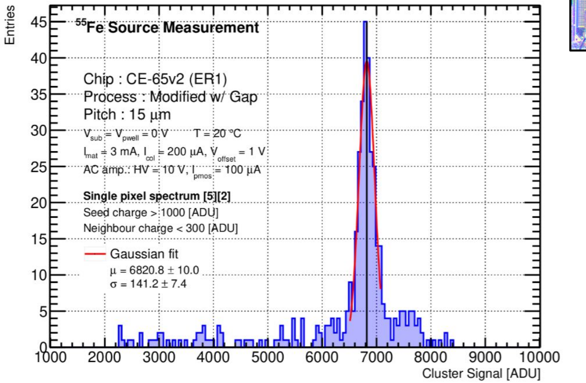
➔ Extract noise per pixel by fitting with Gaussian

➔ Majority of pixels in 15-25 e ENC range

CE-65 Characterisation: Lab tests + Testbeam measurements







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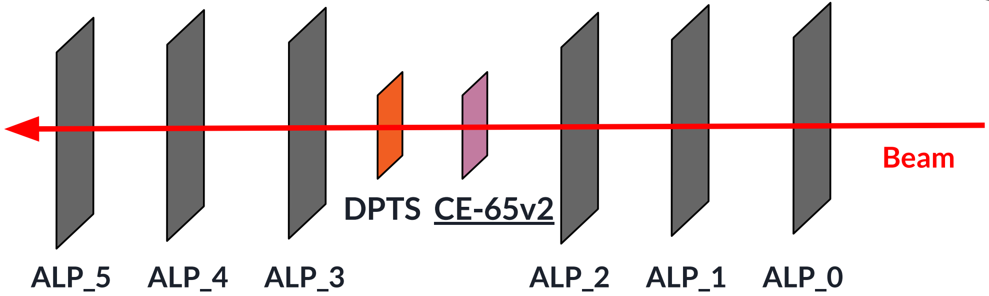

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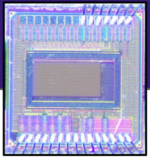
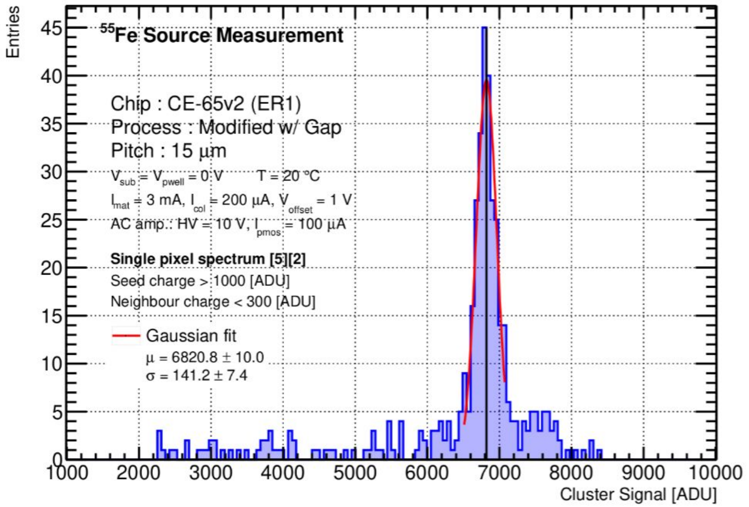
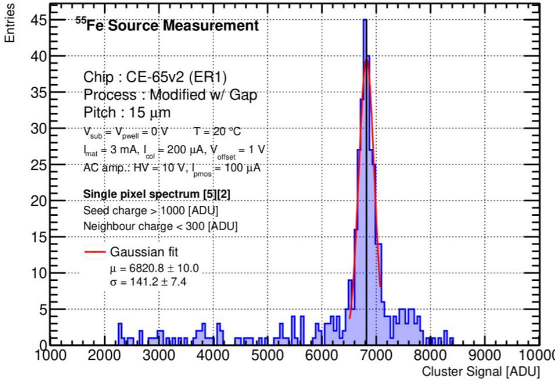




- ➔ Fit Kα peak position
- ➔ Similar response along design axes (~3.4%)

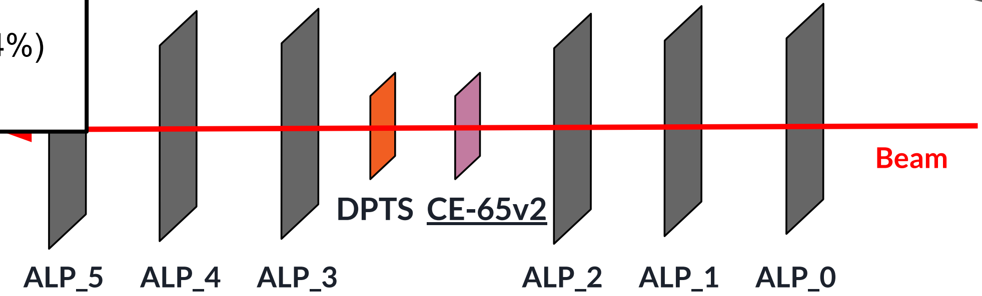
Strategy



- ➔ Pixel gain calibrated from Fe-55 peak

beam

- ➔ Testbeams at SPS + DESY



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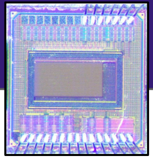

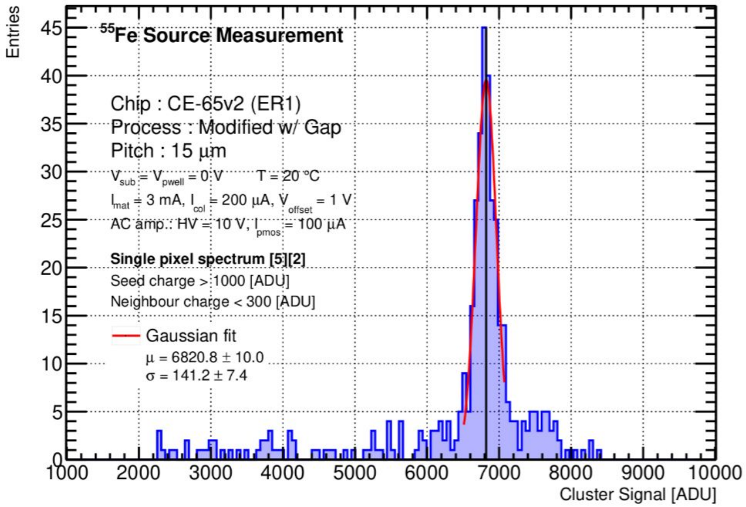

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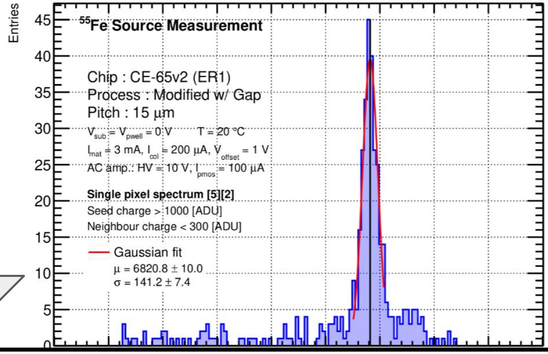
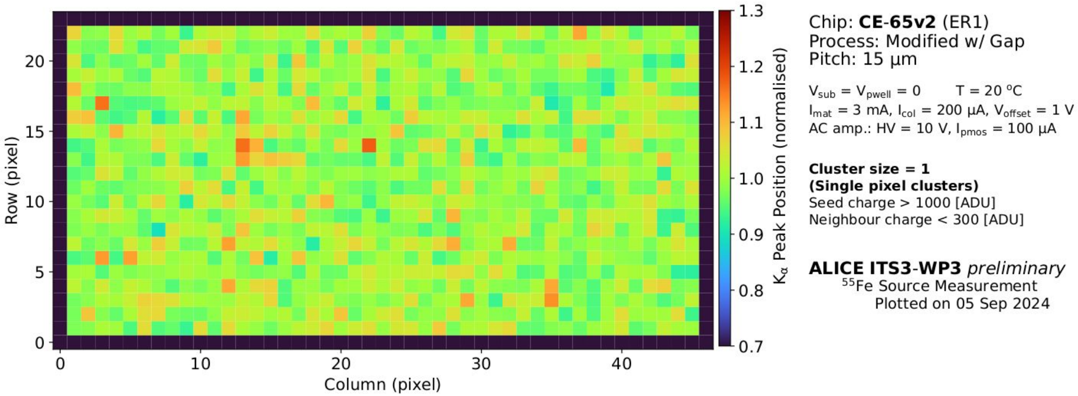




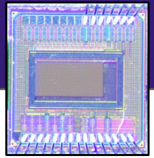
- ➔ Observe O(4%) gain uniformity

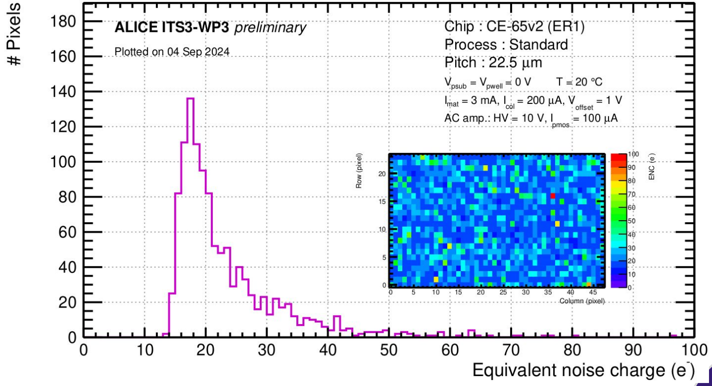
beam

- ➔ Testbeams at SPS + DESY

ALP_5

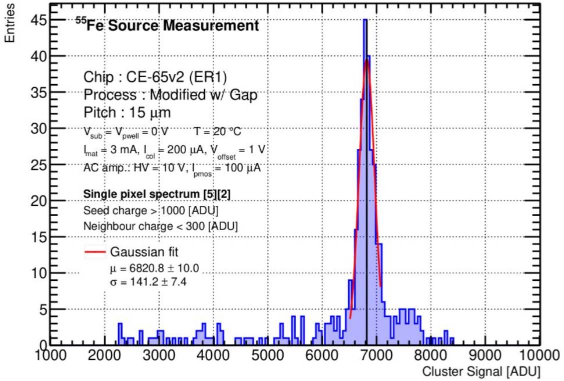
CE-65 Characterisation: Lab tests + Testbeam measurements





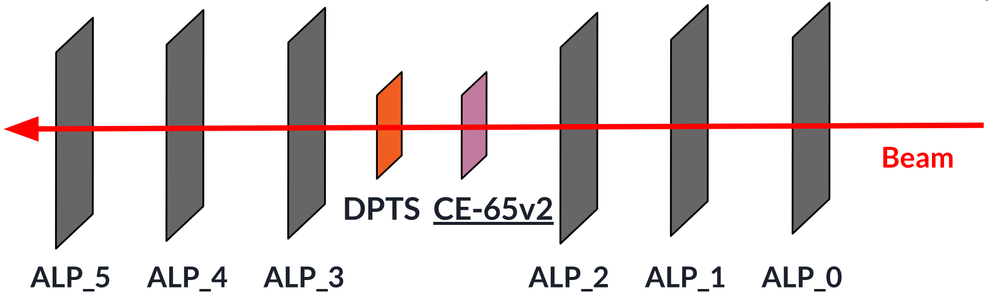
- ➔ Noise measurements in absence of signal
- ➔ Width of noise distribution defines performance

Strategy

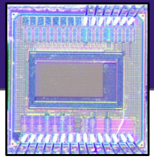


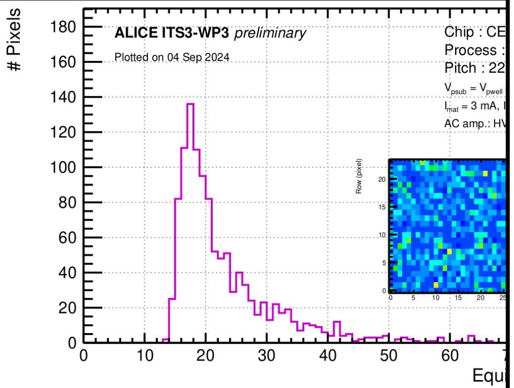
- ➔ Pixel gain calibrated from Fe-55 peak

- ➔ Chip response to MIPs at test beam
- ➔ Testbeams at SPS + DESY



CE-65 Characterisa easurements





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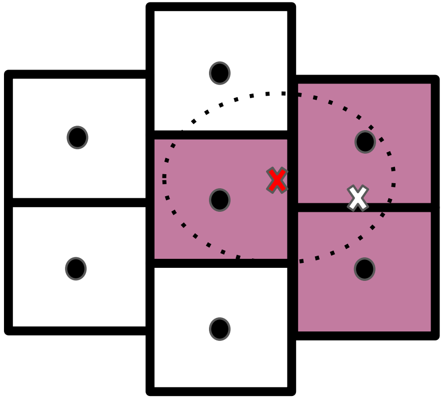
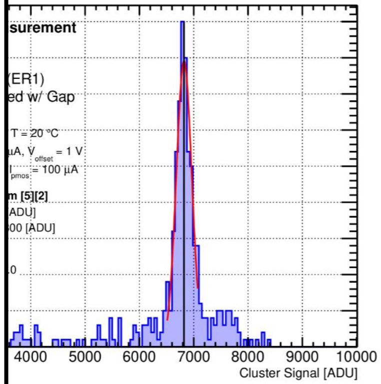


➔ Measure **Efficiency**



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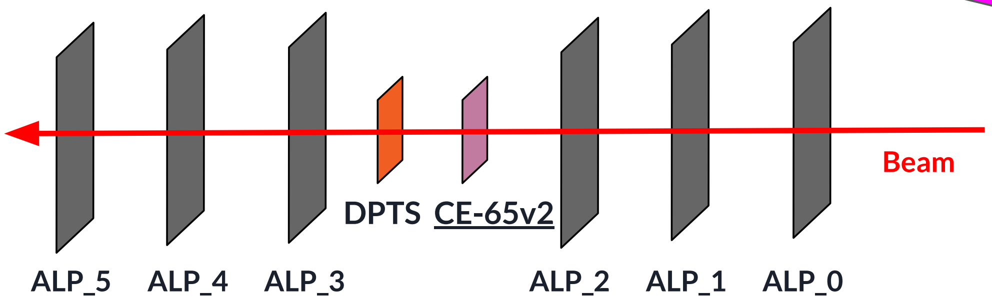
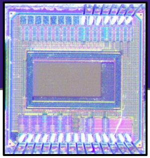
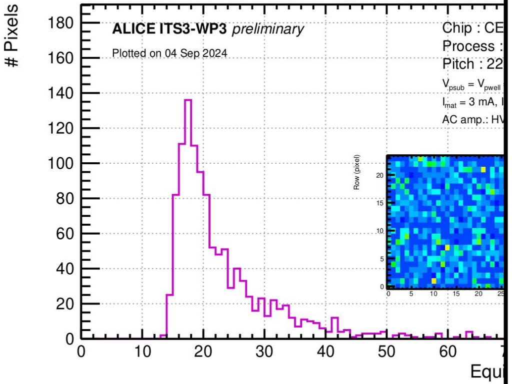


CE-65 Characterisa… easurements





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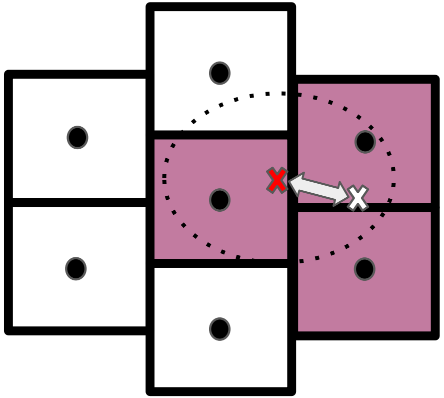
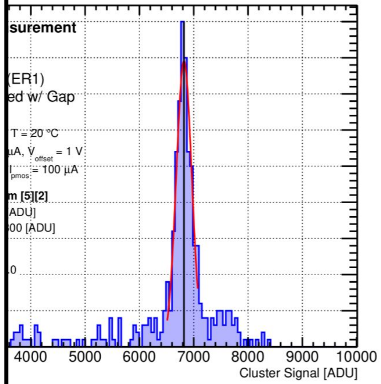
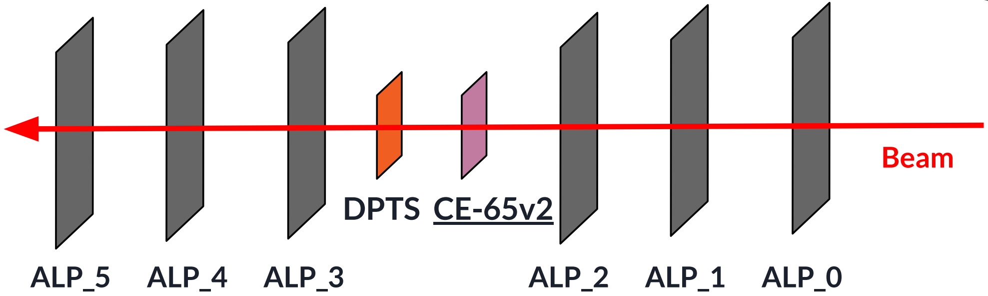


➔ Measure **Spatial Resolution**

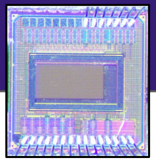


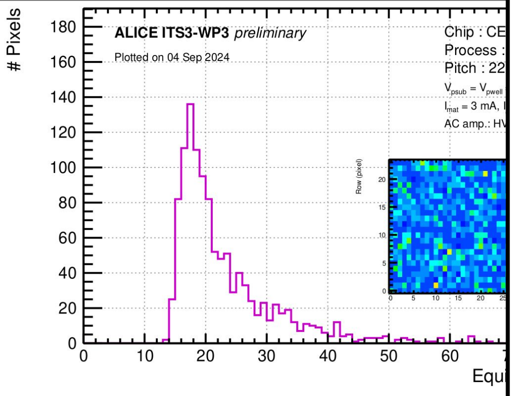
Pixel gain calibrated from Fe-55 peak

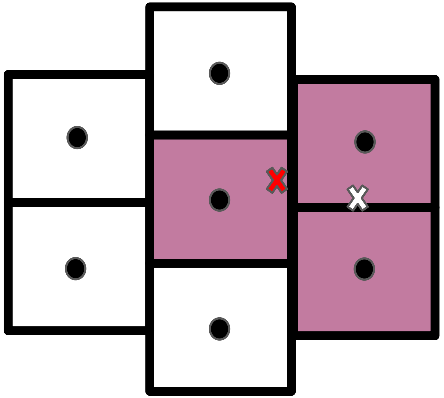
- ➔ Chip response to MIPs at test beam
- ➔ Testbeams at SPS + DESY



CE-65 Characterisa… easurements

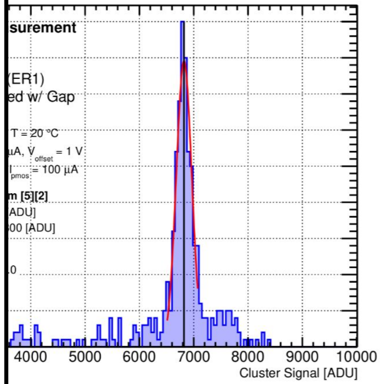






$$f^{i}_{acc.} = \frac{\sum_{j=1}^{i} Q_j}{\sum_{j=1}^{9} Q_j}$$

- ➔ Measure **Accumulated Charge Ratio** as
- ➔ Fraction of charge carried by first n pixels in cluster



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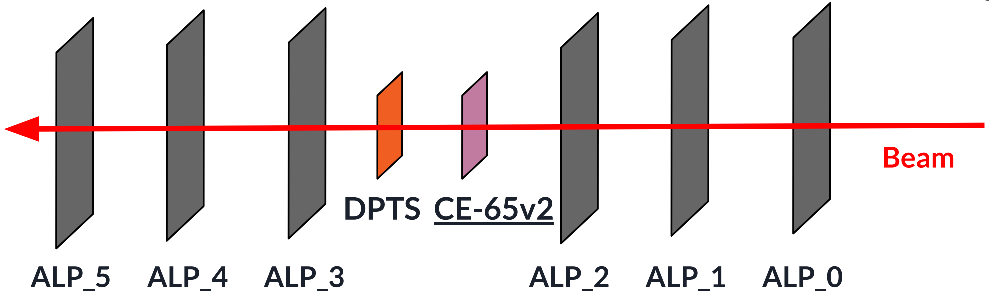
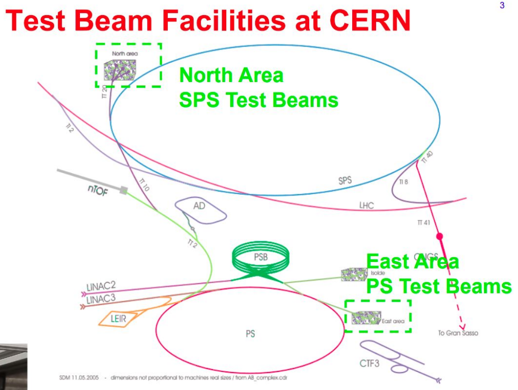


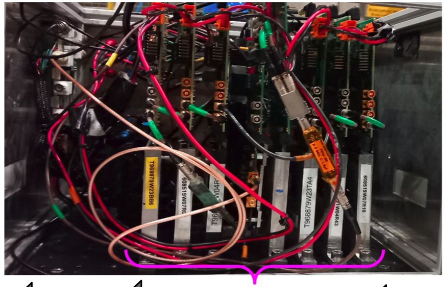
(SPS) Beam Test Campaign

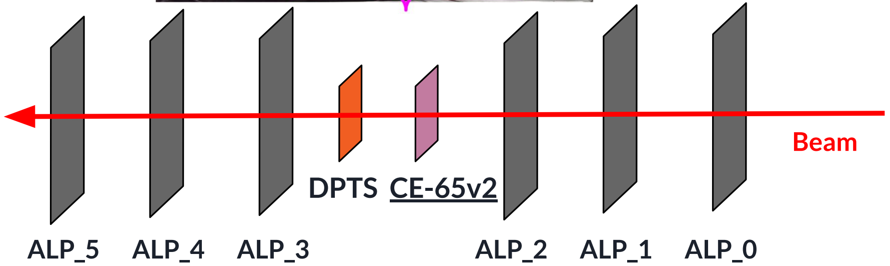
- ➔ Beam test at **CERN SPS** H6 beam line (17-24 April 2024)
- ➔ **120 GeV/c** mixed hadron beam
- ➔ Goal: Study efficiency/resolution of different variants of CE-65v2
  - ◆ Pitch comparison: **15 µm**, 18 µm, **22.5 µm**
  - ◆ Process comparison: **Standard** vs **Modified w/ Gap**
  - ◆ Matrix arrangement: **Squared** vs **Staggered**



- ➔ Telescope
  - ◆ 6 ALPIDE planes for tracking
  - ◆ DPTS as Trigger
    - ● Movable stage
  - ◆ CE-65v2 as DUT
    - ● Temperature held at 20oC

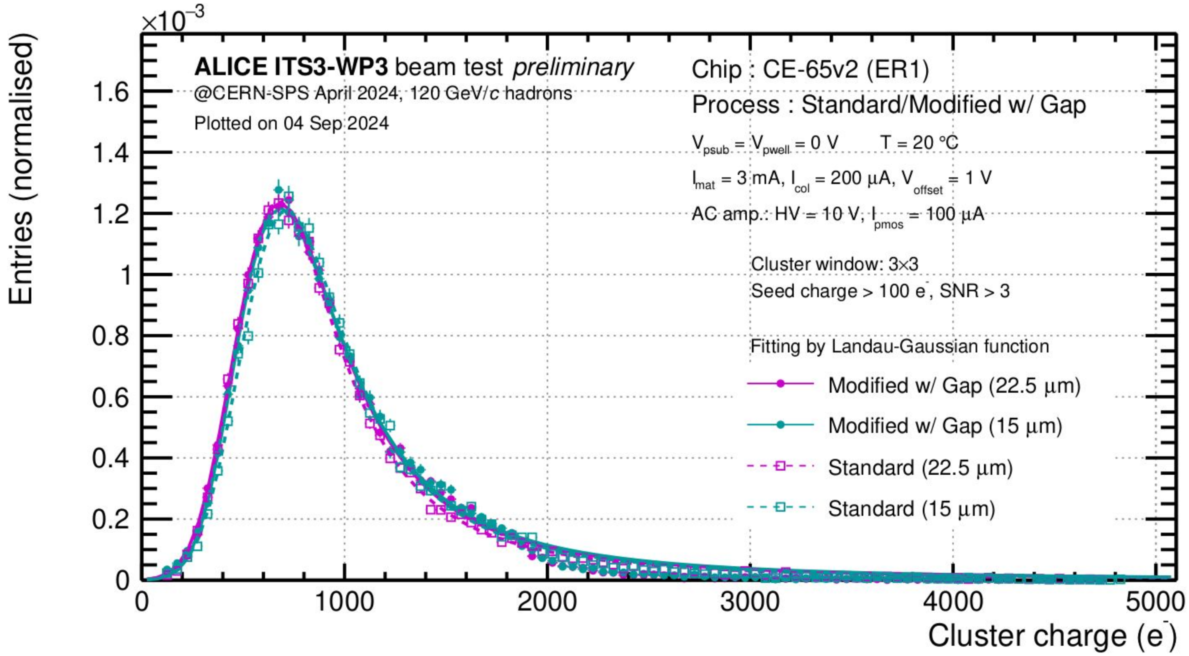
using chiller





Track resolution estimated **~2.2 µm**

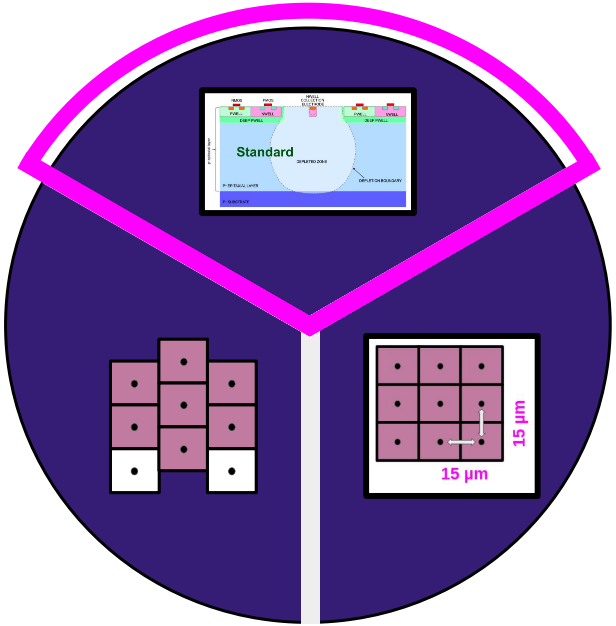
(SPS) Analysis results



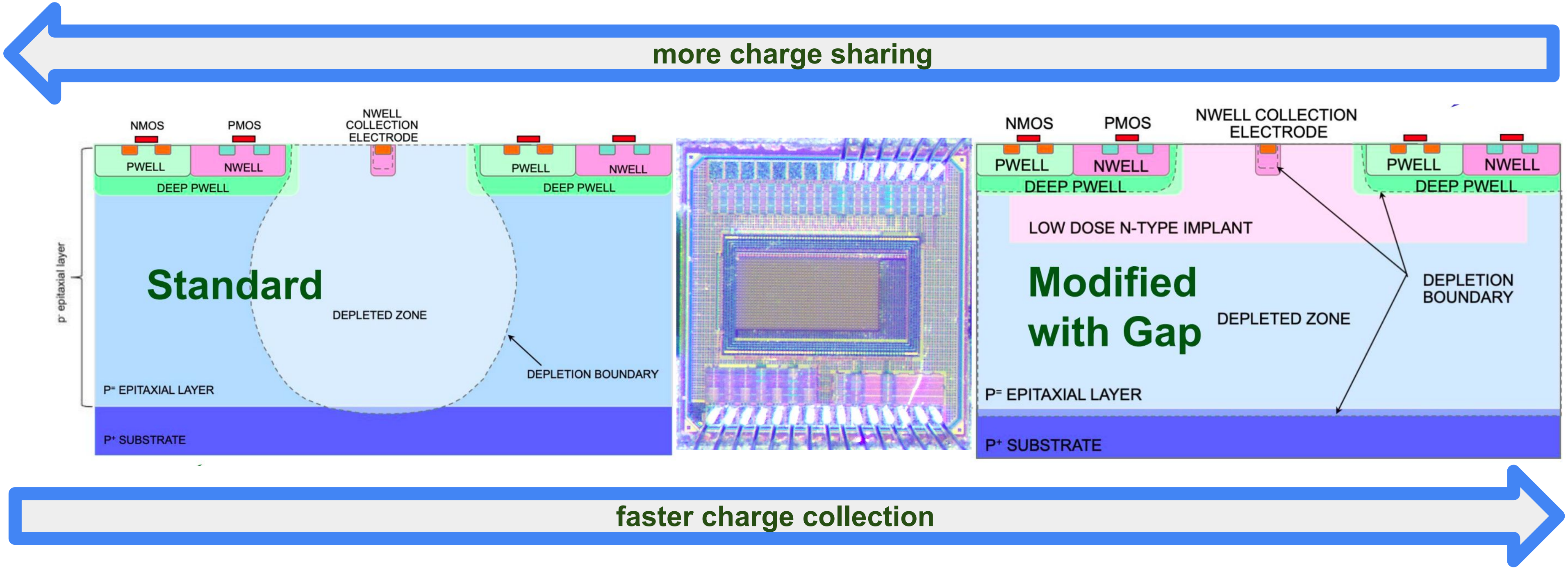
➔ Fit **cluster charge** to Landau-Gaussian

- ◆ Similar response for all 4 chips

Design Axis: Process

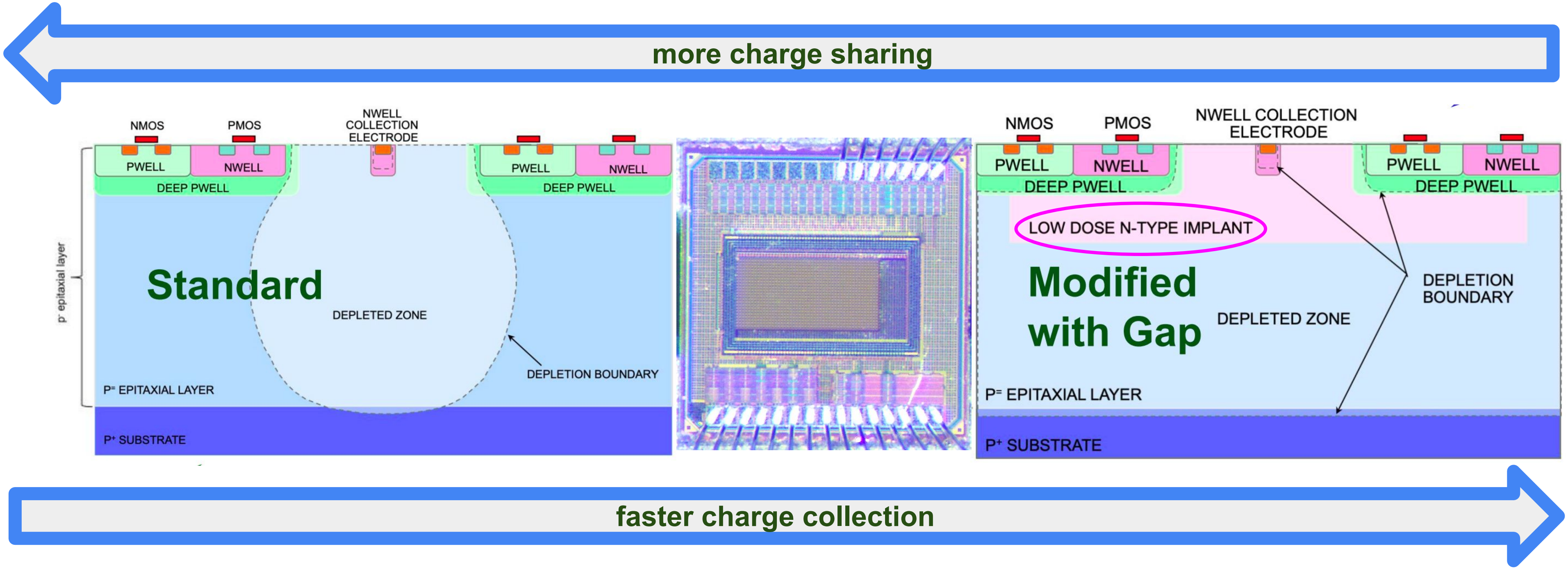


Process Modifications: “Standard” vs “Modified with Gap”



- ➔ “Circuit Exploratoire” implemented in three process variations
  - ◆ Modifications introduced following lessons learned from ITS2 upgrade

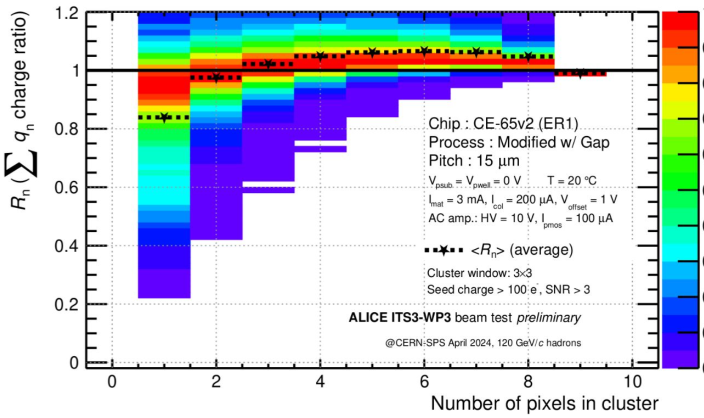
Process Modifications: “Standard” vs “Modified with Gap”

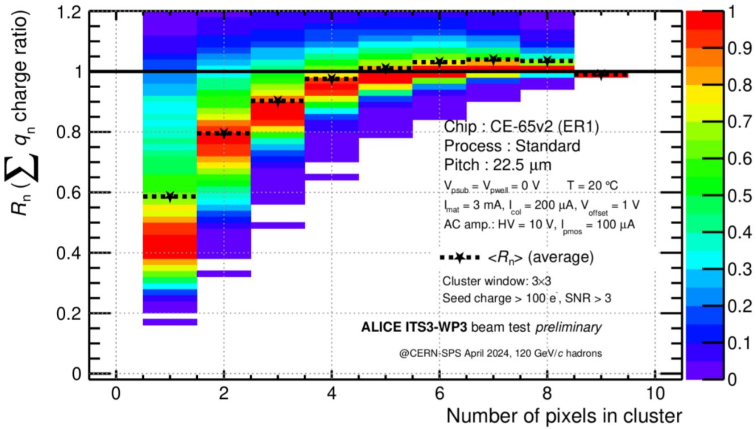


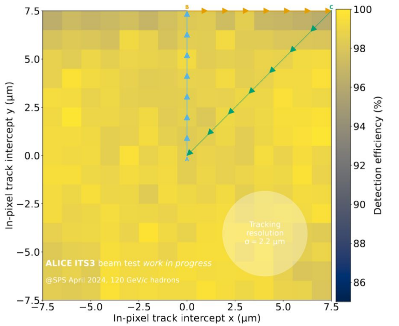
➔ “Circuit Exploratoire” implemented in three process variations

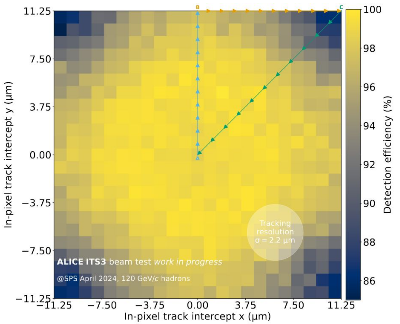
- Modifications introduced following lessons learned from ITS2 upgrade

Charge Sharing much higher in Standard Process



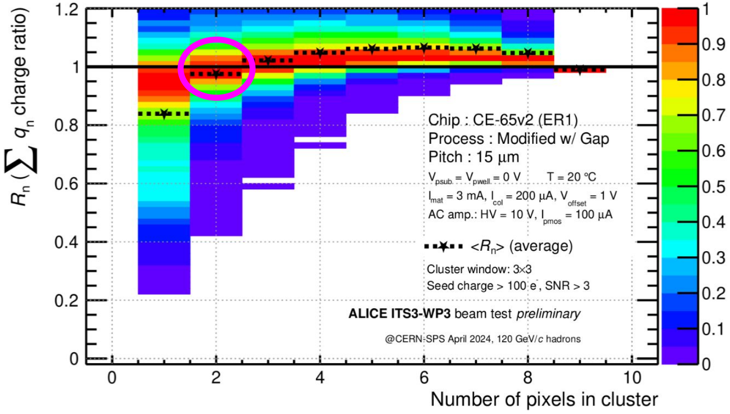


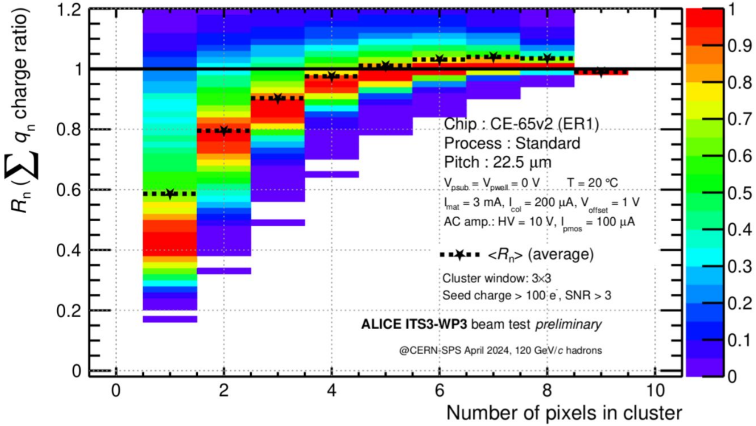


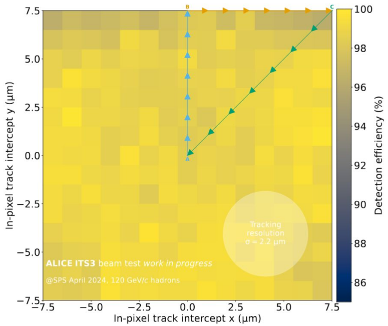


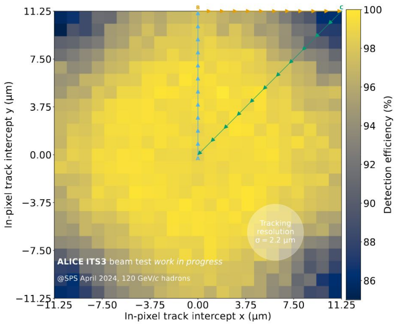
- ➔ Modified with Gap variant carries virtually all charge in the first two pixels of a cluster
- ➔ Standard variant splits charge across ~4+ pixels in a given cluster

Charge Sharing much higher in Standard Process









➔ **Modified with Gap** variant carries virtually all charge in the **first two pixels** of a cluster

➔ Standard variant splits charge across ~4+ pixels in a given cluster

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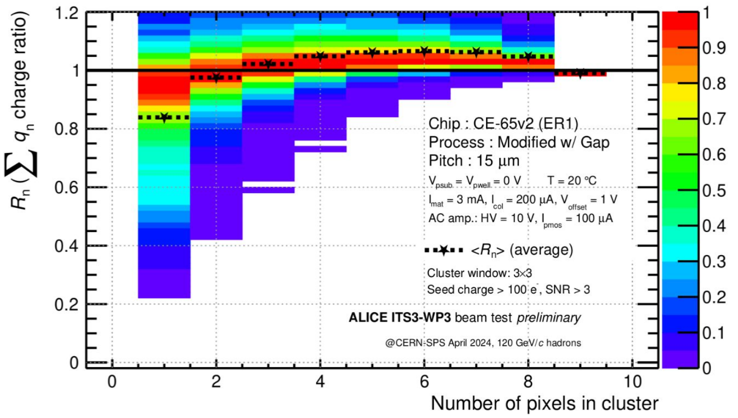

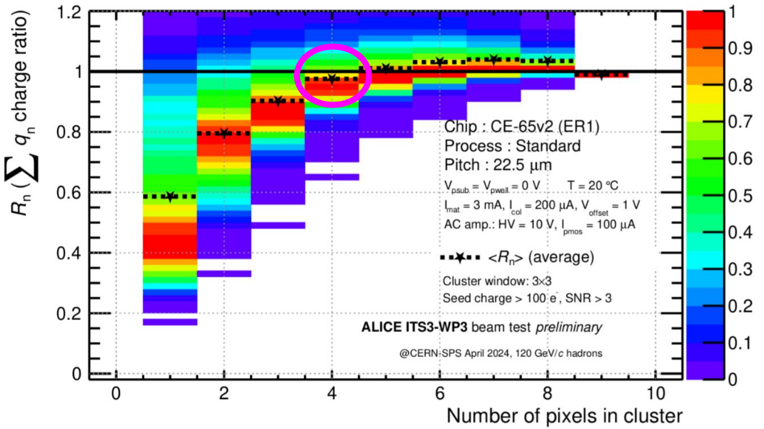

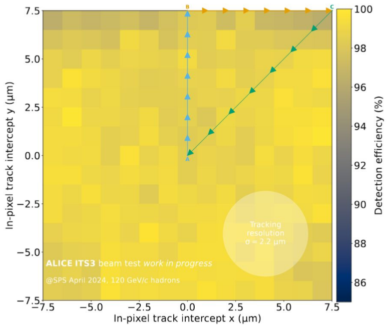

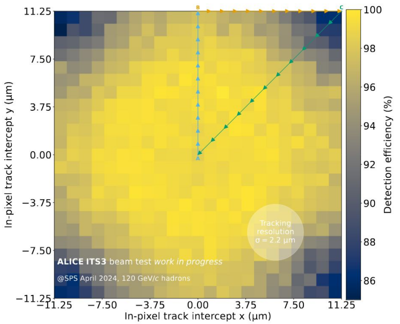

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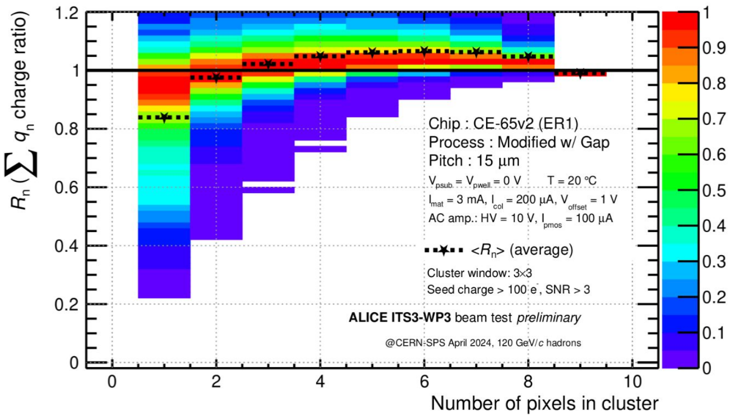

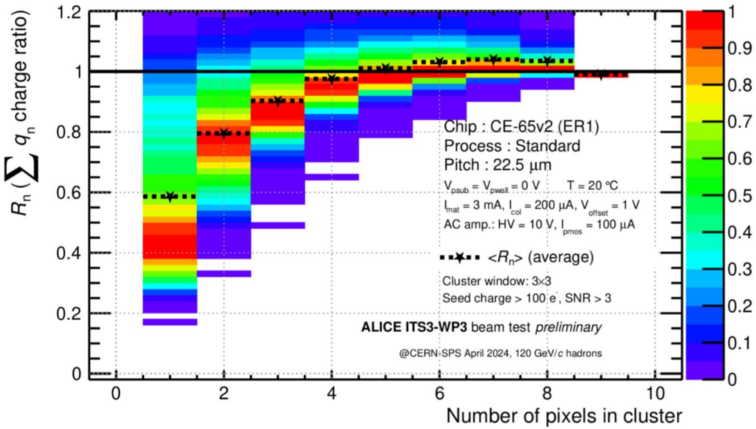

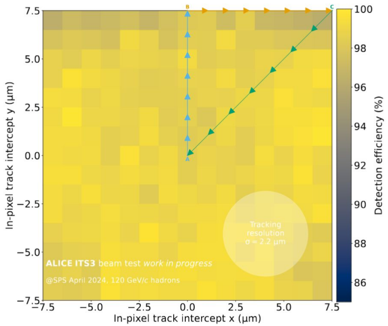

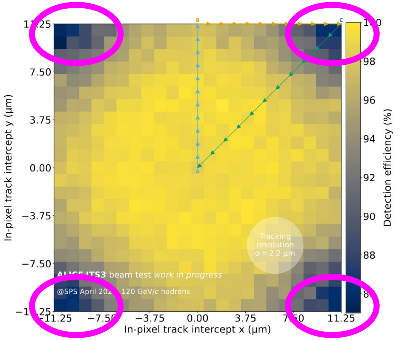

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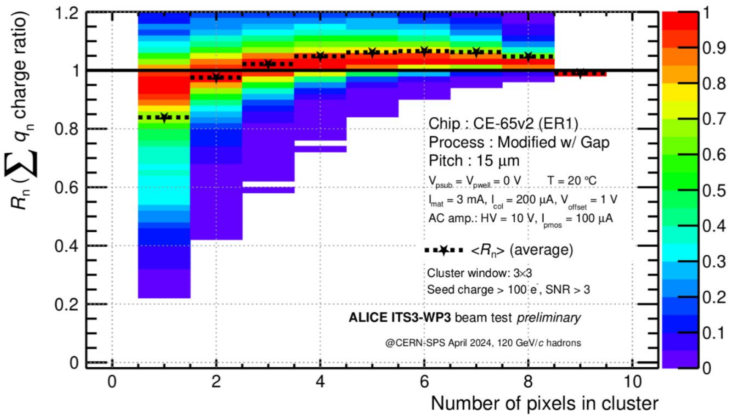
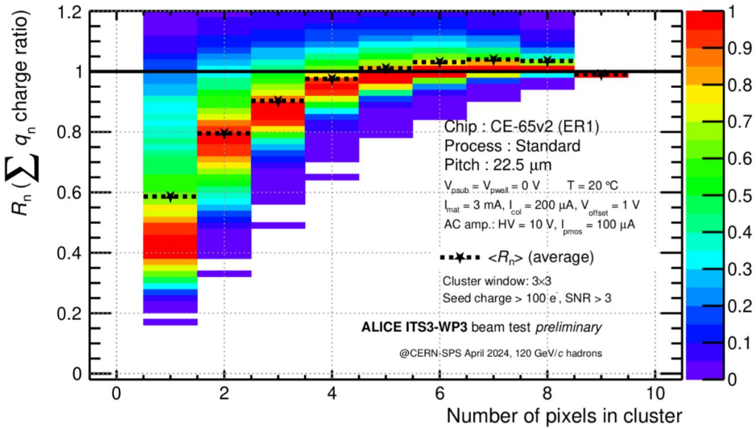
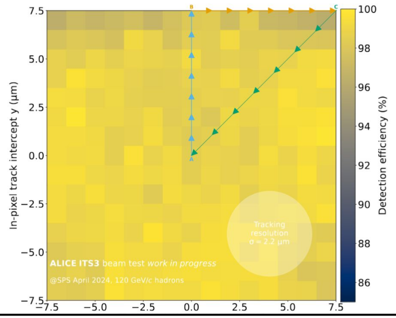
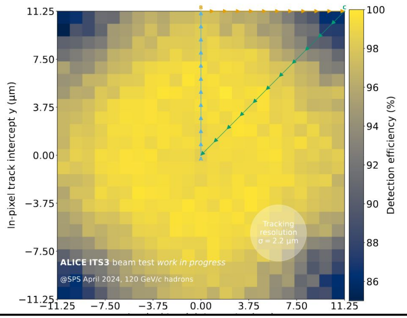




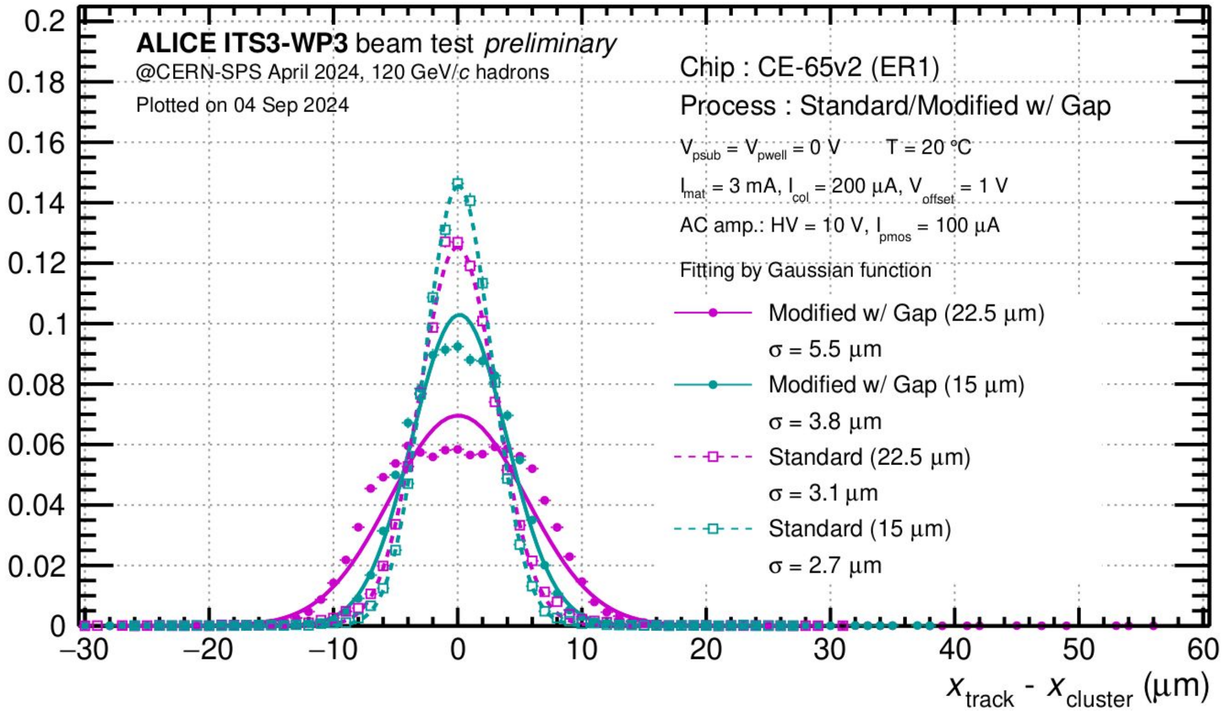




➔ But how much does the **position reconstruction** improve?

➔ **Standard variant** splits charge across ~**4+ pixels** in a given cluster

Standard Process outperforms Modified w/ Gap

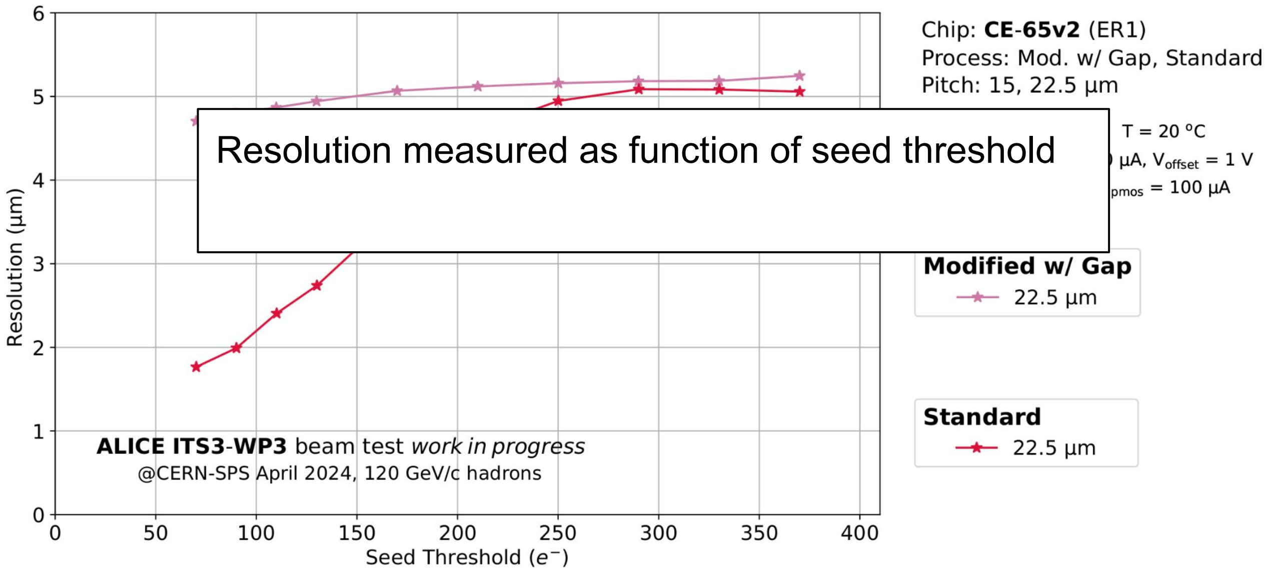


Window Method (100 e-)

➔ Residuals considerably **smaller for Standard** variants due to charge sharing

Standard process spatial resolution <3 µm, meeting FCC-ee goals

Cluster Method



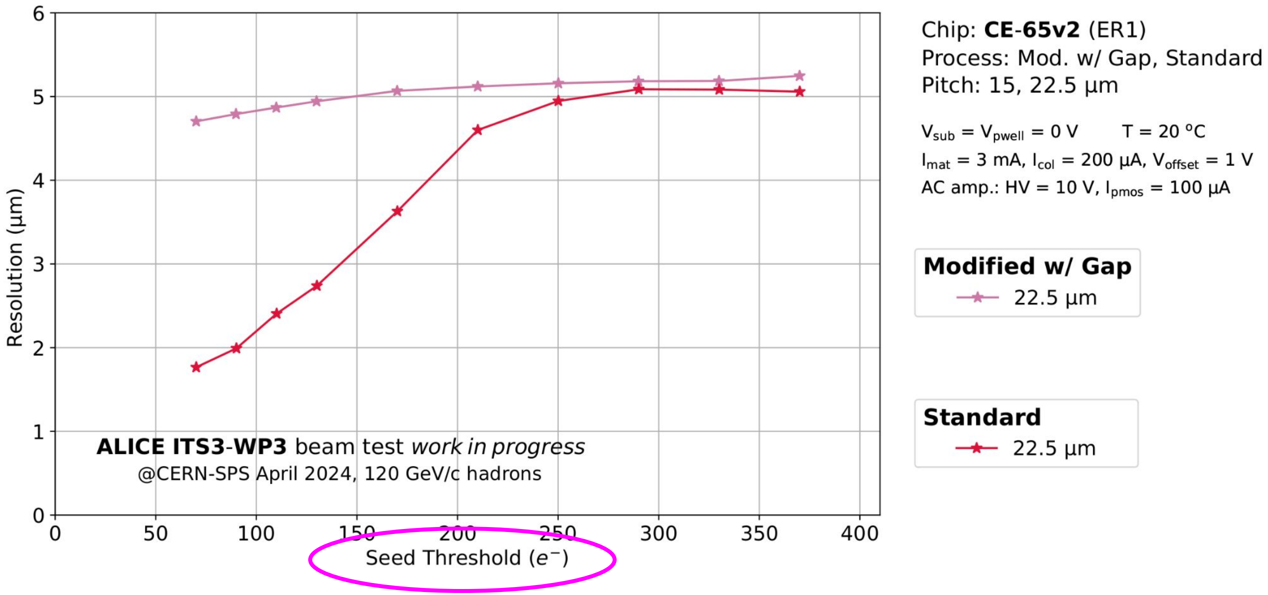
Resolution measured as function of seed threshold

➔ Standard process achieves excellent sub 3 µm resolution at low thresholds

➔ Modified w/ Gap variants achieve a worse resolution

Standard process spatial resolution <3 µm, meeting FCC-ee goals

Cluster Method

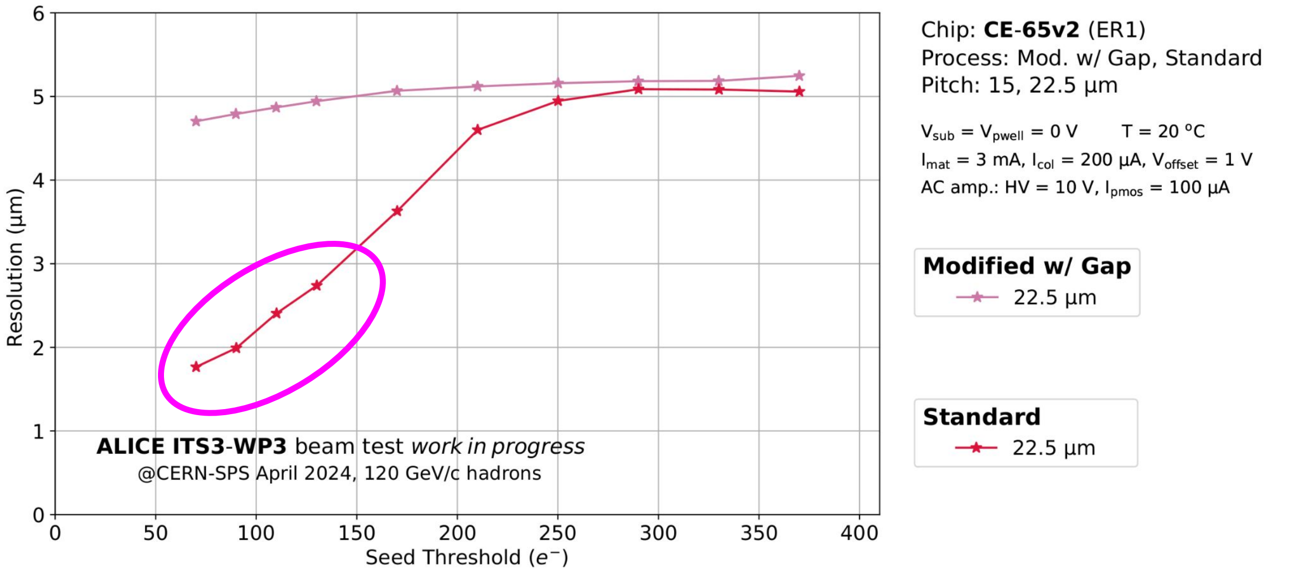


Require **at least** this signal charge

- ➔ Standard process achieves excellent sub 3 µm resolution at low thresholds
- ➔ Modified w/ Gap variants achieve a worse resolution

Standard process spatial resolution <3 µm, meeting FCC-ee goals

Cluster Method



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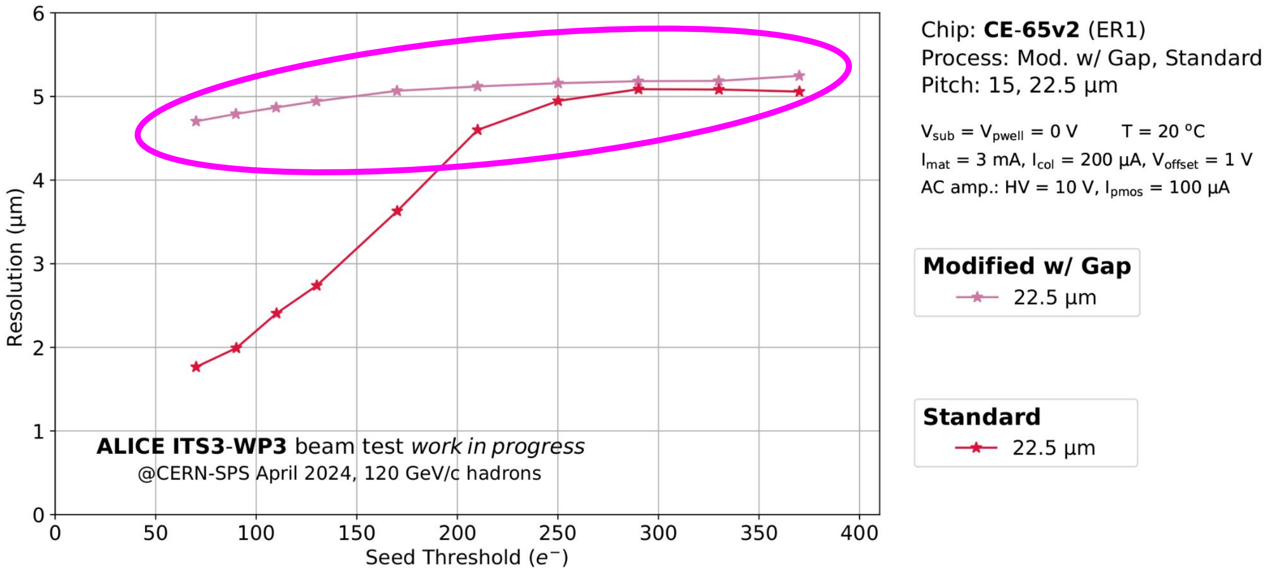
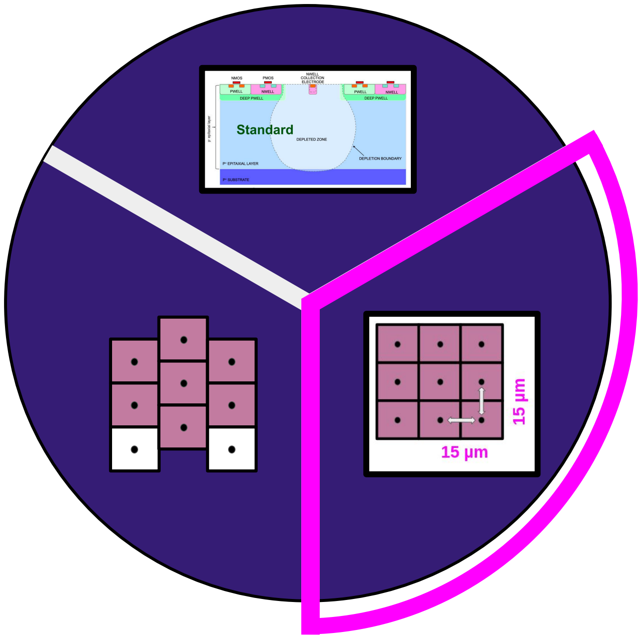


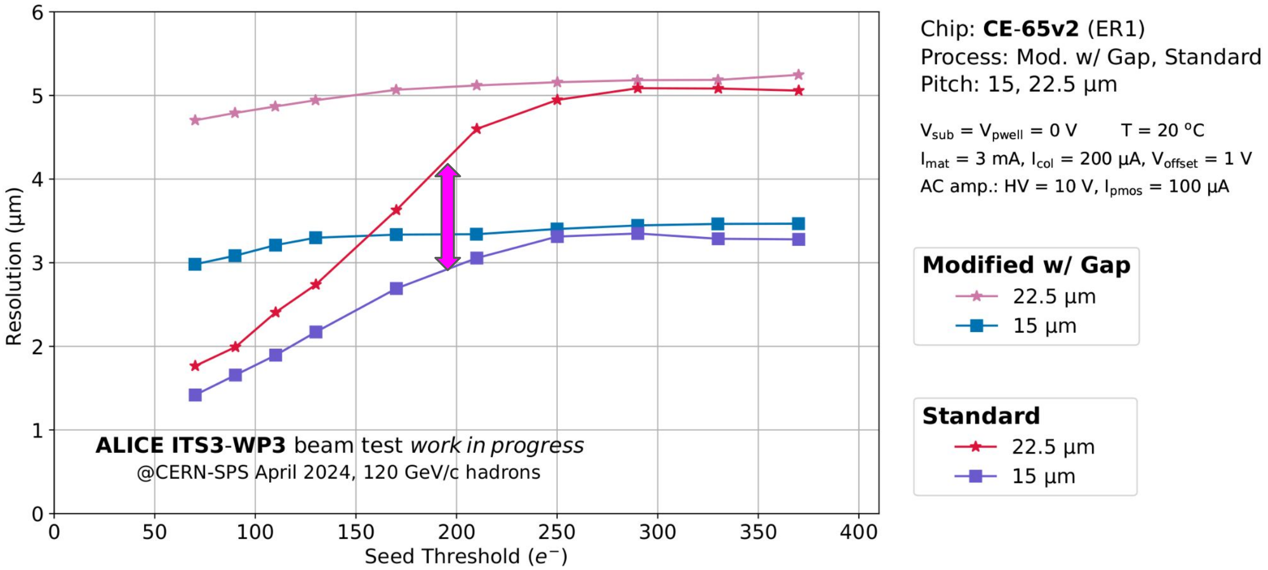
➔ **Standard process** achieves excellent **sub 3 µm resolution** at low thresholds

➔ **Modified w/ Gap** variants achieve a **worse resolution**

Design Axis: Pitch



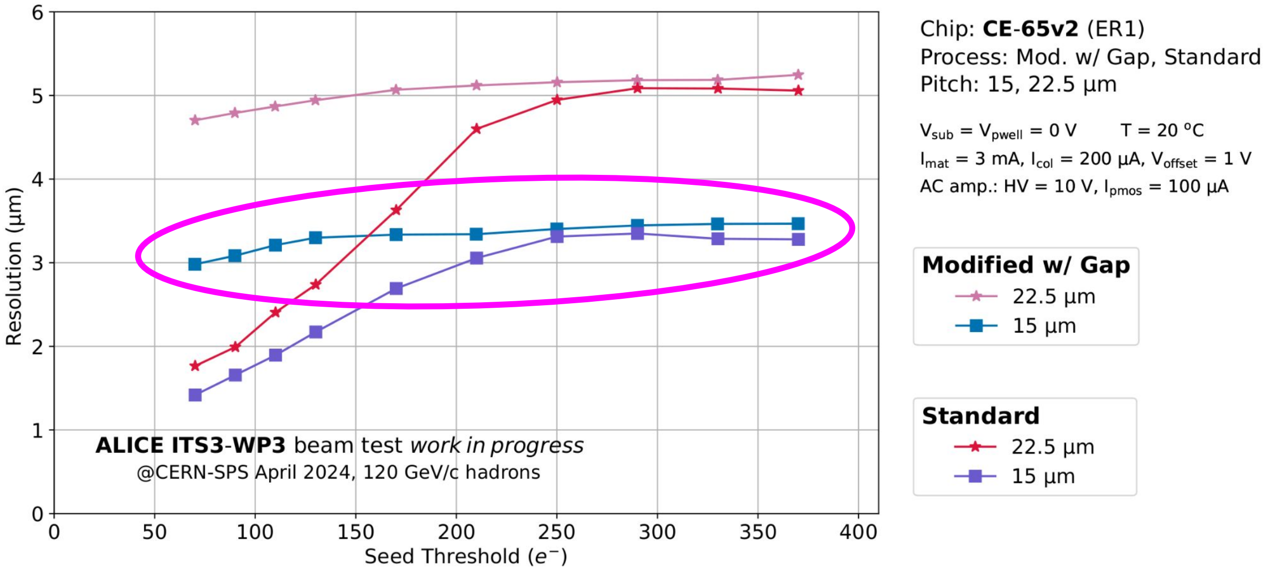
Modified with Gap + small pitch ≈ 3 µm spatial resolution



Cluster Method

- ➔ **Small-pitch** (15 µm) **Standard process** chip further **improves** in resolution
  - ◆ Effect smaller at low thresholds
- ➔ Small-pitch (15 µm) Modified with Gap chip now just above 3 µm
  - ◆ Across all thresholds

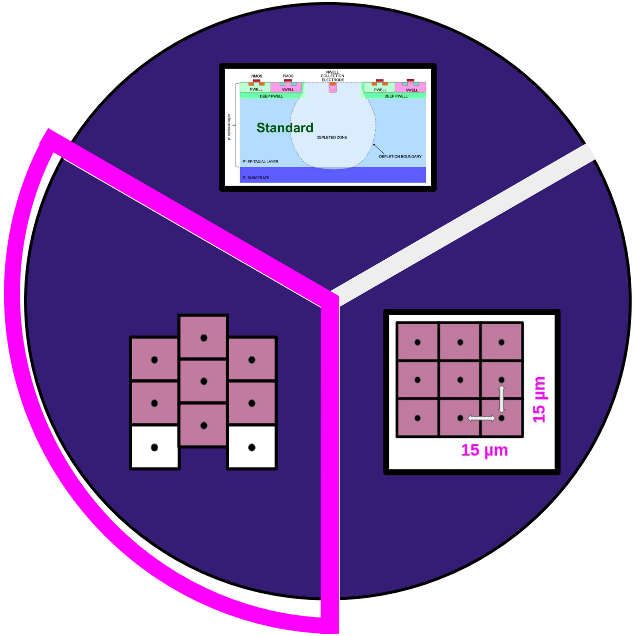
Modified with Gap + small pitch ≈ 3 µm spatial resolution



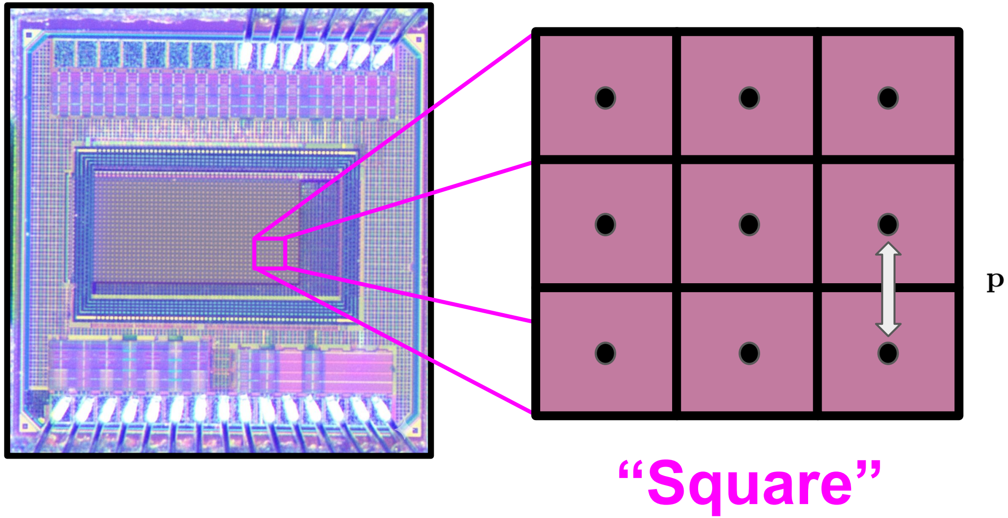
Cluster Method

- ➔ **Small-pitch** (15 µm) **Standard process** chip further **improves** in resolution
  - ◆ Effect smaller at low thresholds
- ➔ **Small-pitch** (15 µm) **Modified with Gap** chip now just above **3 µm**
  - ◆ Across all thresholds

Design Axis: Matrix Geometry



Matrix Geometry: Square vs Staggered



- ➔ Arrangement of **matrix** typically in **rectangle** of individual pixels
  - ◆ Baseline design
- ➔ CE-65v2 chip additionally implements “staggered” matrix design

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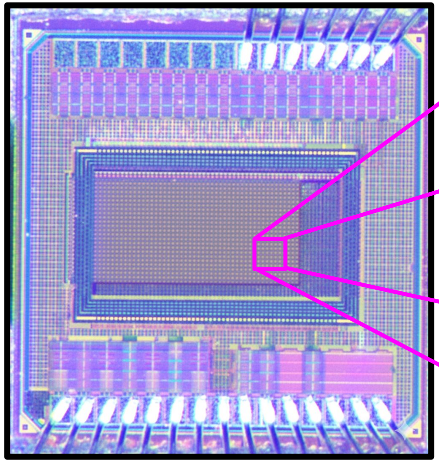

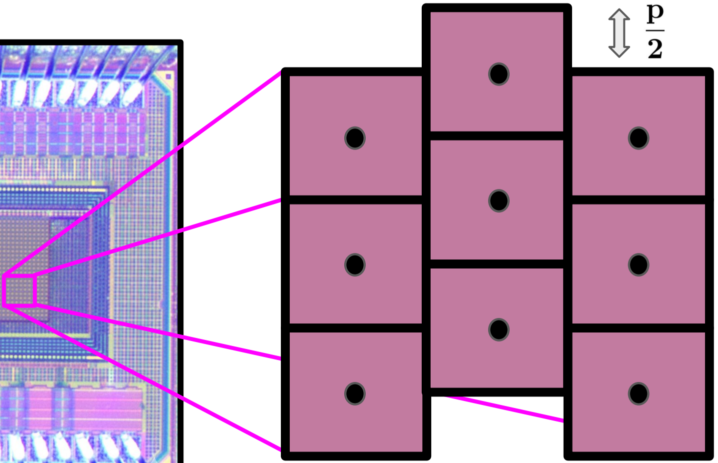

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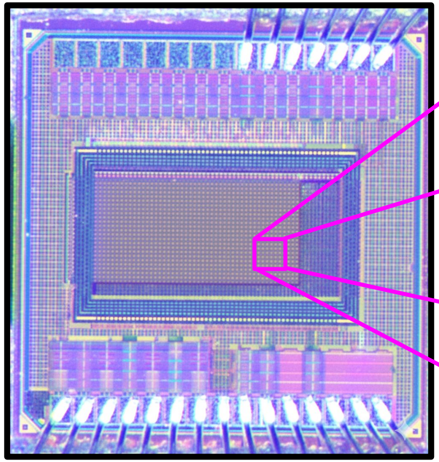

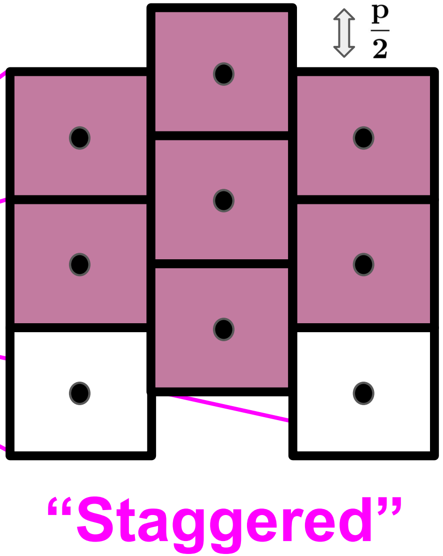

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  - ◆ 8 -> 6
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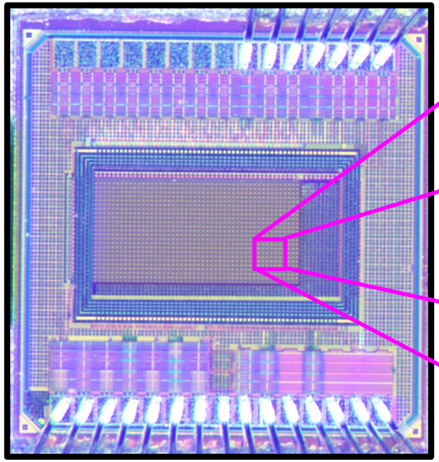

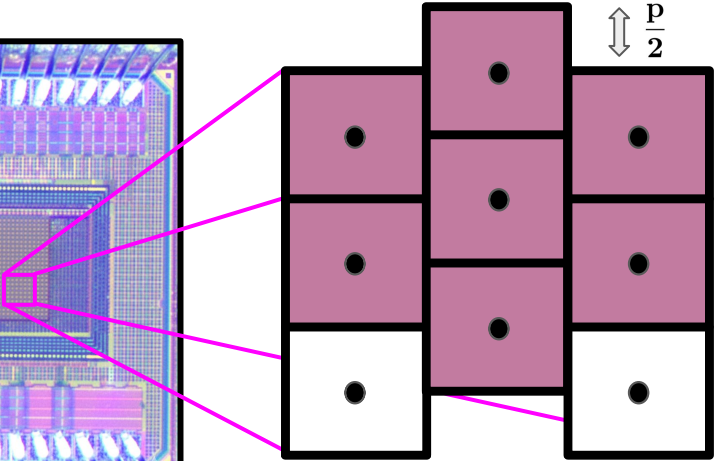

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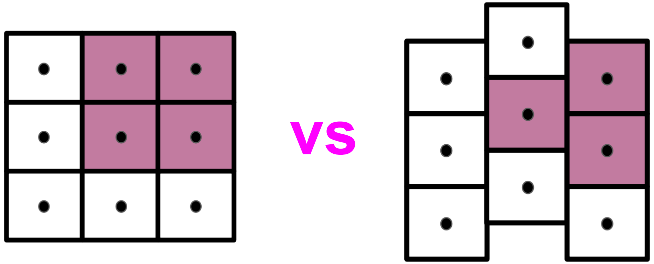

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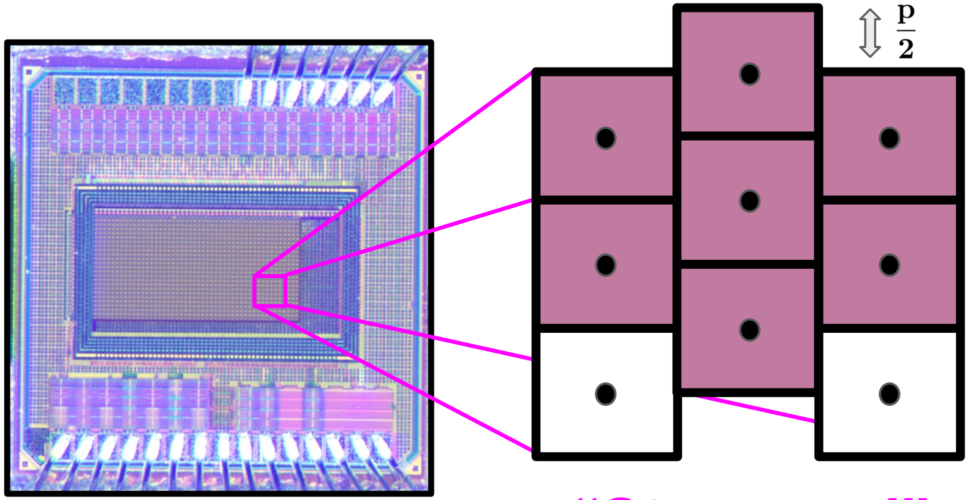

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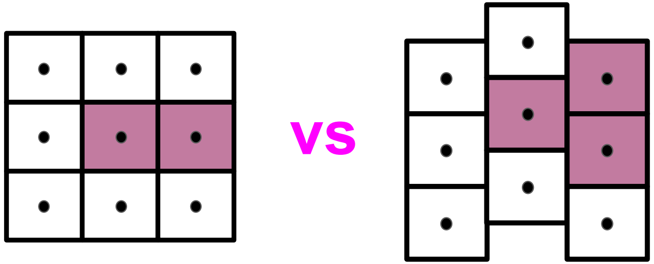
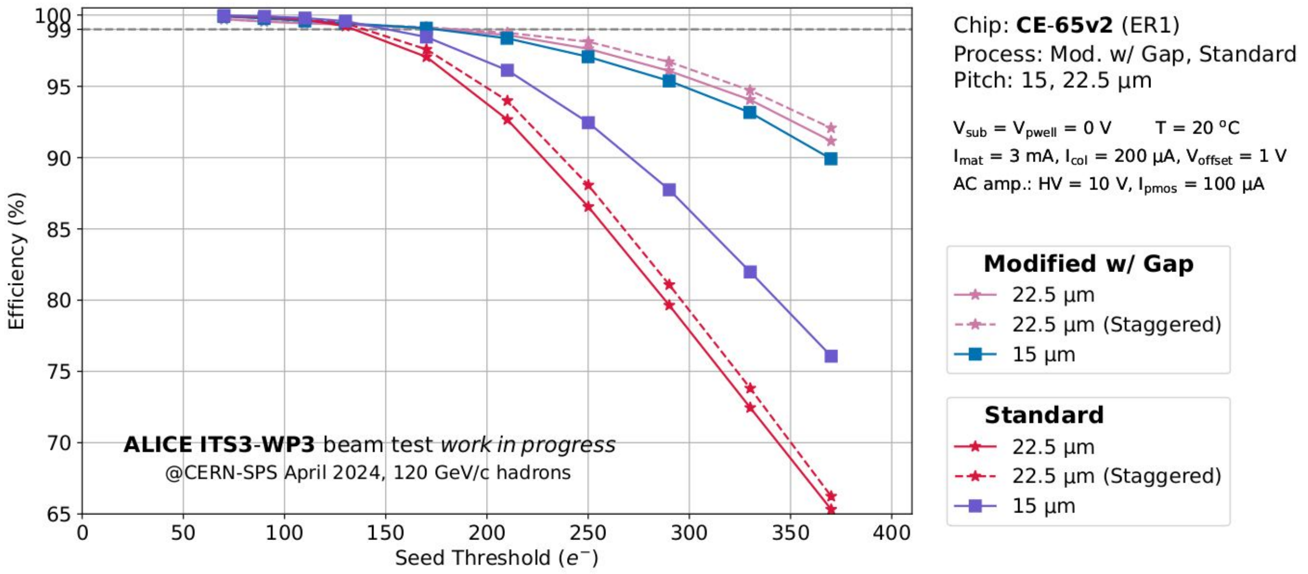


Staggered Matrix little effect on Hit-detection Efficiency



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➔ Both the **Standard** process and **Modified with Gap** process chips only **marginally benefit** from Staggered arrangement

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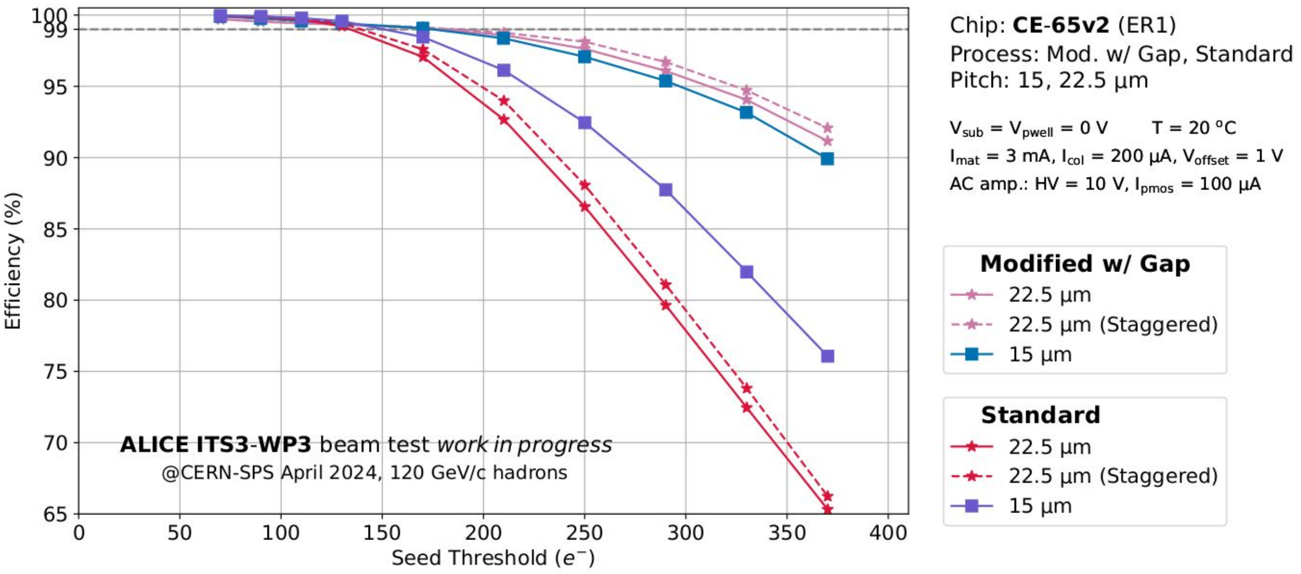

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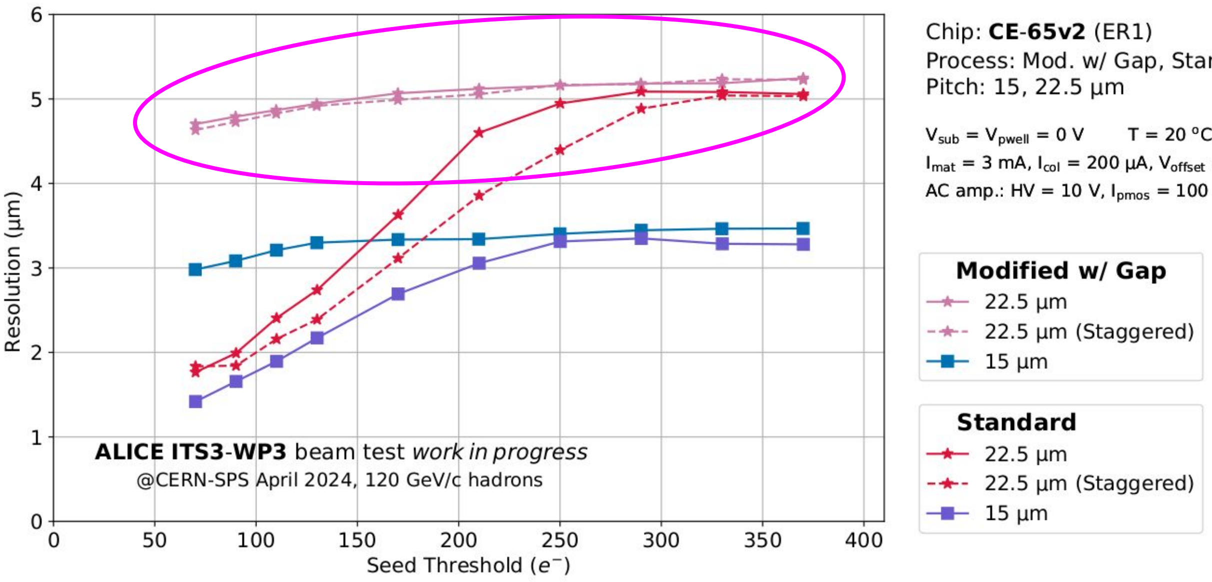
But what about the **spatial resolution**?

Staggered Matrix improves spatial resolution



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➔ Virtually **no effect** on Modified w/ Gap variants

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- Improvement largest at intermediate thresholds
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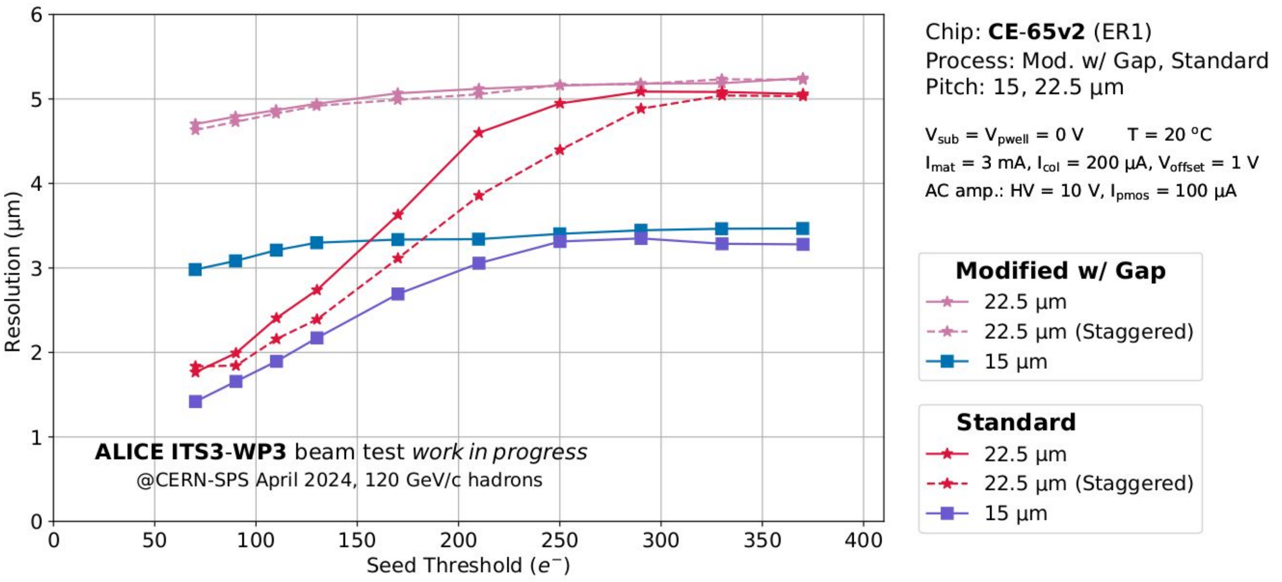

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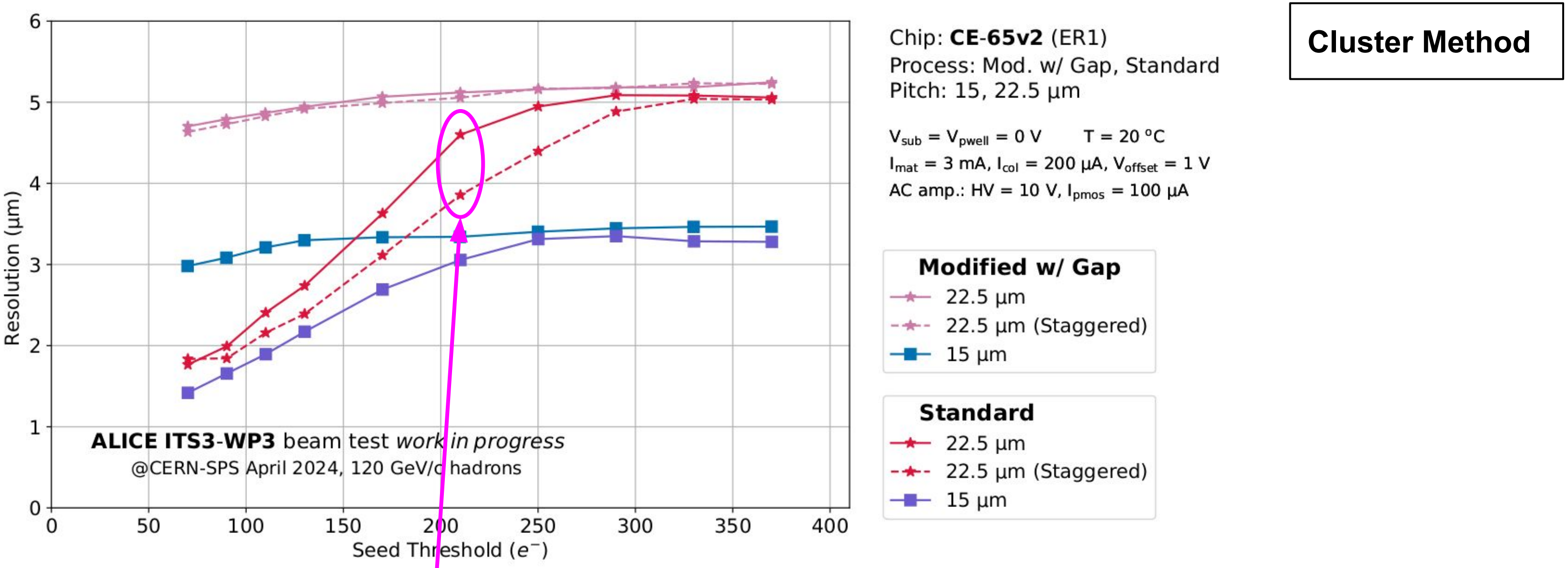

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Conclusion

Summary and Outlook

- ➔ CE-65v1 and CE-65v2 variants exhibit low-noise across different pixel pitches and process modifications
  - ◆ Majority of pixels in **15-25 e ENC** range
- ➔ Gain calibration performed using Fe-55 source
  - ◆ **AC-coupled** preamplifier allows tuning of charge sharing, near-**full depletion** of sensitive volume
  - ◆ Gain uniformity at the O(4%) level
- ➔ **Excellent resolution** was obtained in large-matrix **65 nm CMOS test structures** at SPS testbeam
  - ◆ **Sub 3 µm** spatial resolution for Standard process chips
  - ◆ 15 µm Modified with Gap process just above 3 µm
  - ◆ **Staggered** arrangement shows **16% improvement** at 210 e threshold
- ➔ Further testbeam **analysis** of DESY + SPS data **ongoing**
  - ◆ Additional “Modified”/Blanket chips
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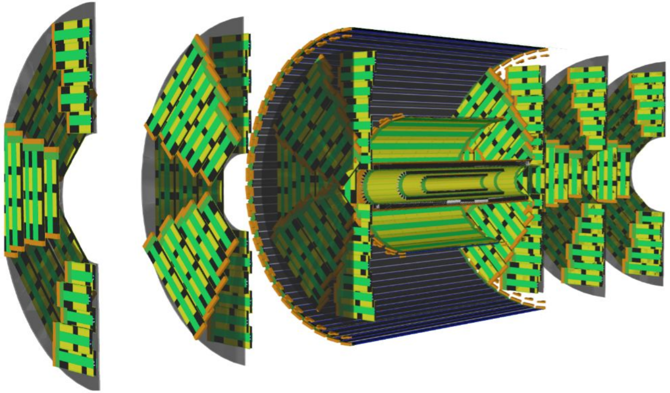
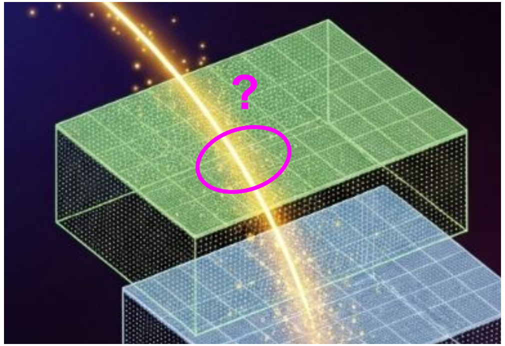
Promising avenues: **small-pitch** (<15 µm) **Modified w/ Gap** and **large-pitch** (>20 µm) **Standard** process

Backup

Vertexing at the FCC-ee

- Vertexing performance at future lepton colliders will crucially depend on
  - **Spatial resolution** of sensors (<3 μm)
  - Material budget of sensors, support structures, and cooling
- Radiation environment much milder than in proton-proton collisions
  - $O(10^{13})$ 1 MeV n_{eq} cm^{-2}
- Monolithic Active Pixel Sensors have emerged as enabling technology





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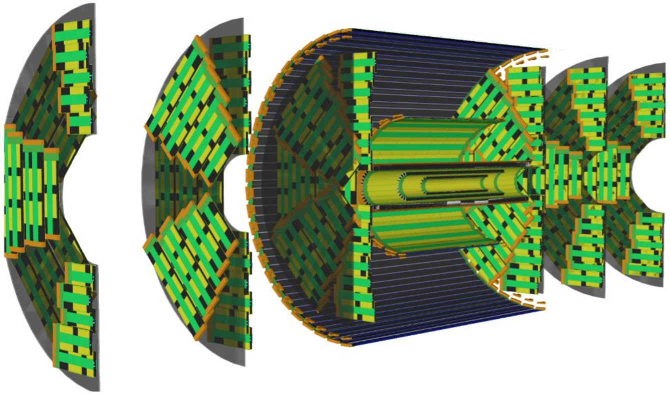

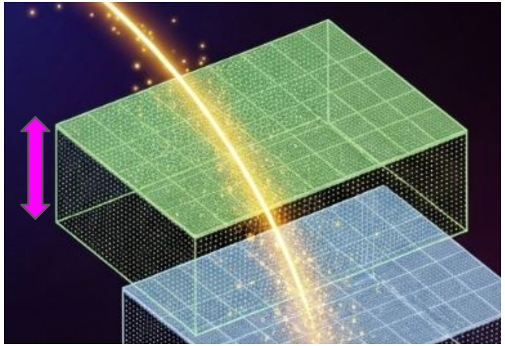

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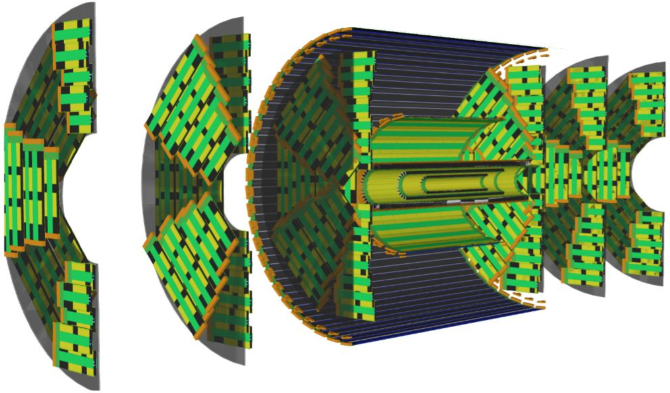
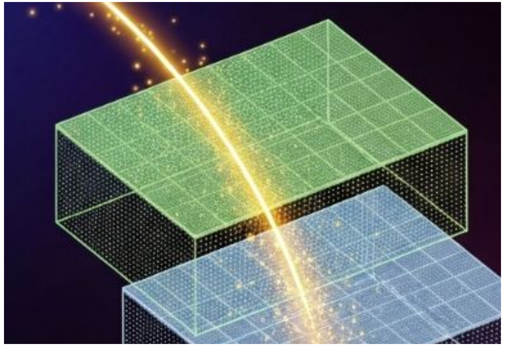
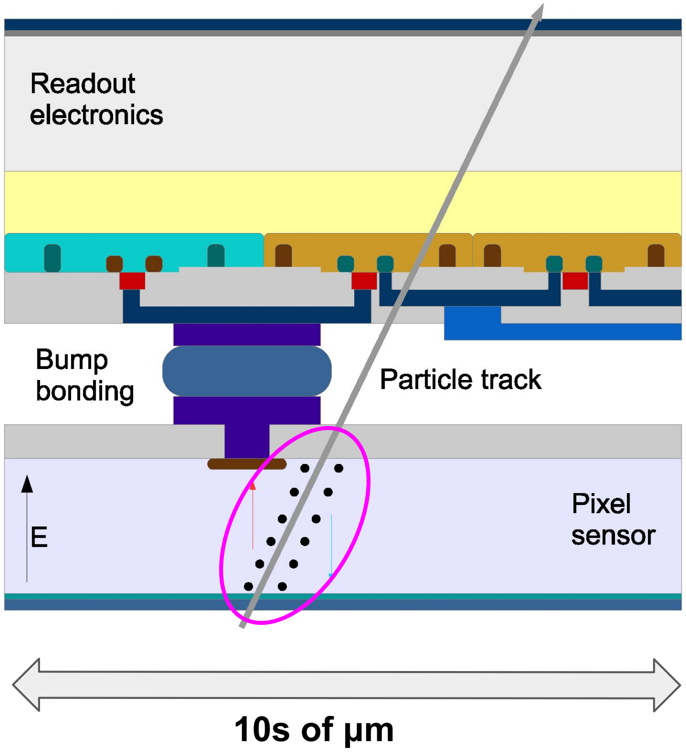




Semiconductor Detectors



- ➔ Function by measuring **charge** deposited by **particles** traversing silicon
  - ◆ Low energy (~ 3.6 eV) required to create an **“electron-hole pair”**
- ➔ Signal = small current
  - ◆ Sophisticated signal processing chain in order to become practically usable
  - ◆ Typically charge collection and signal processing occur on separate chips
- ➔ Can be miniaturised
  - ◆ 10’s of µm
  - ◆ Allows precise track reconstruction

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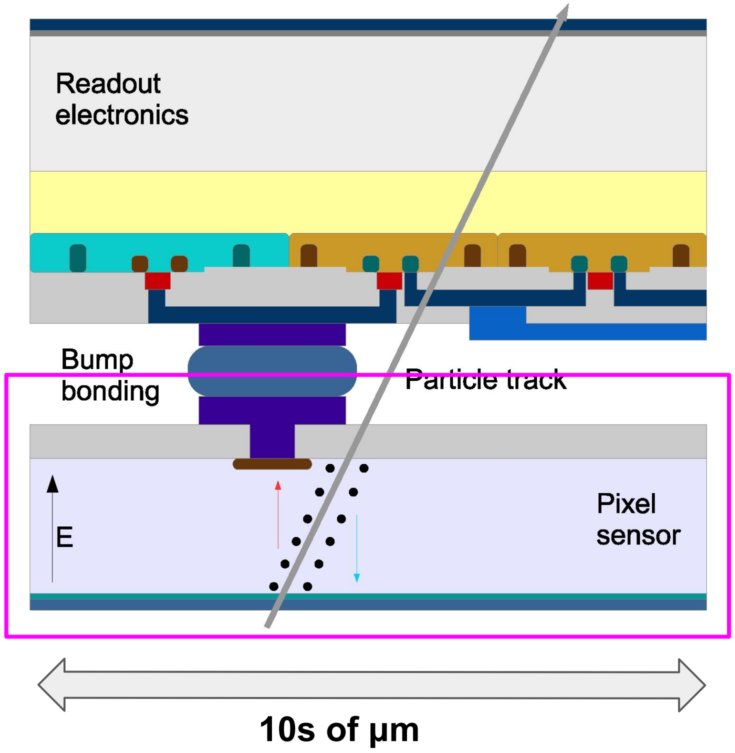

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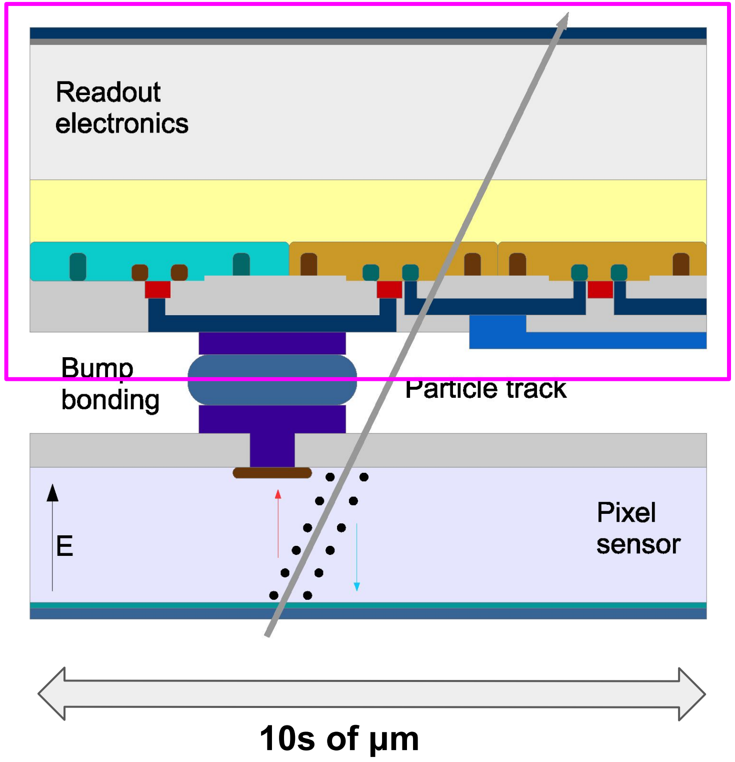

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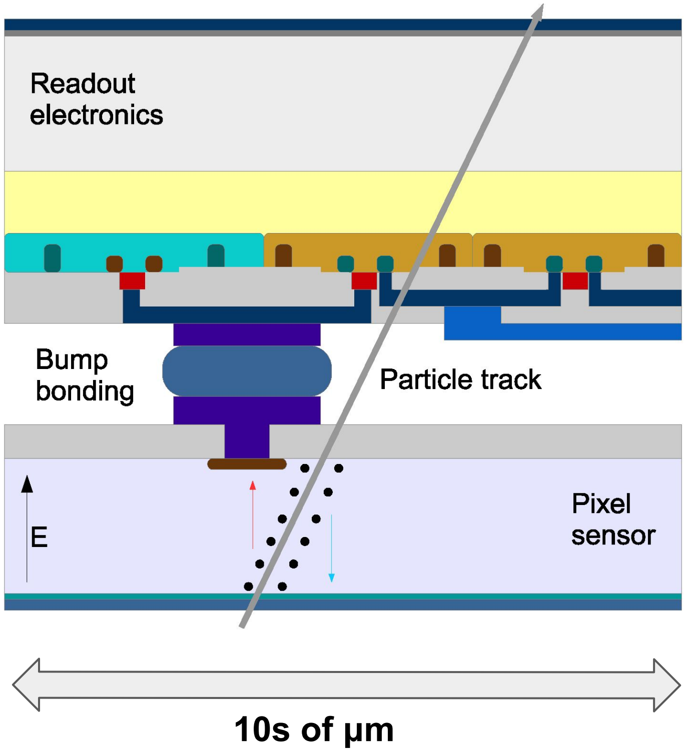

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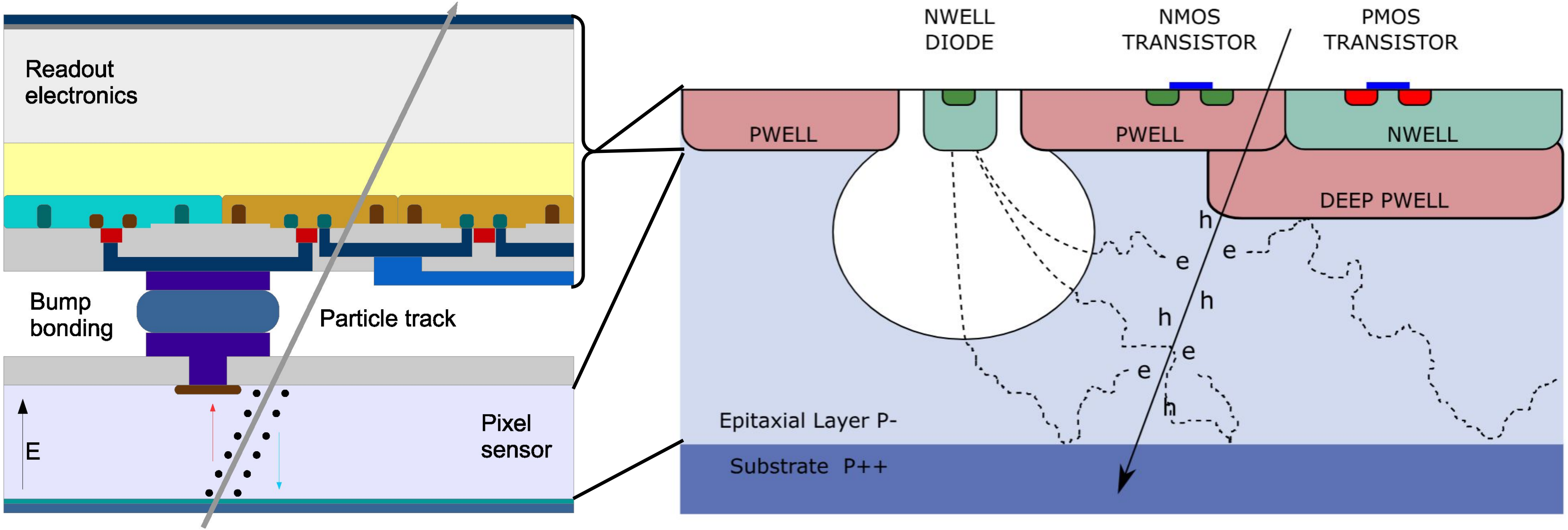
Monolithic Active Pixel Sensors

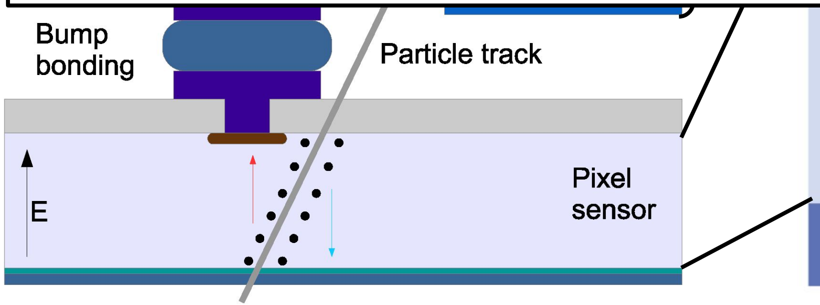


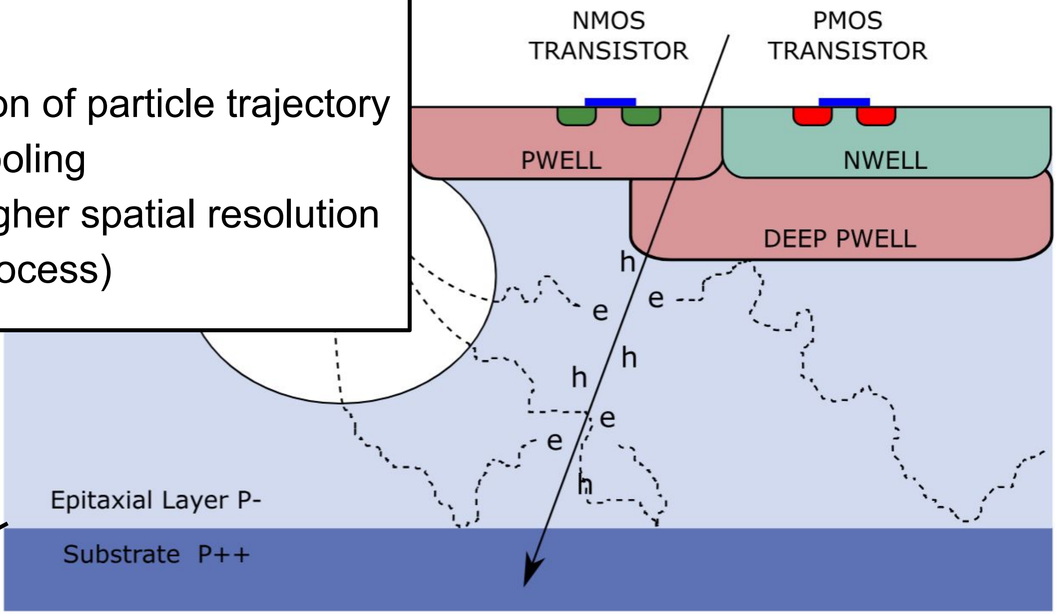
➔ Monolithic Active Pixel Sensors combine the sensor and readout chip onto same piece of silicon!

Monolithic Active Pixel Sensors

Advantages

- ➔ Lower sensor thickness = less deflection of particle trajectory
- ➔ Reduced power consumption = less cooling
- ➔ Smaller width (pixel pitch ~20 μm) = higher spatial resolution
- ➔ Cheaper (can often use commercial process)





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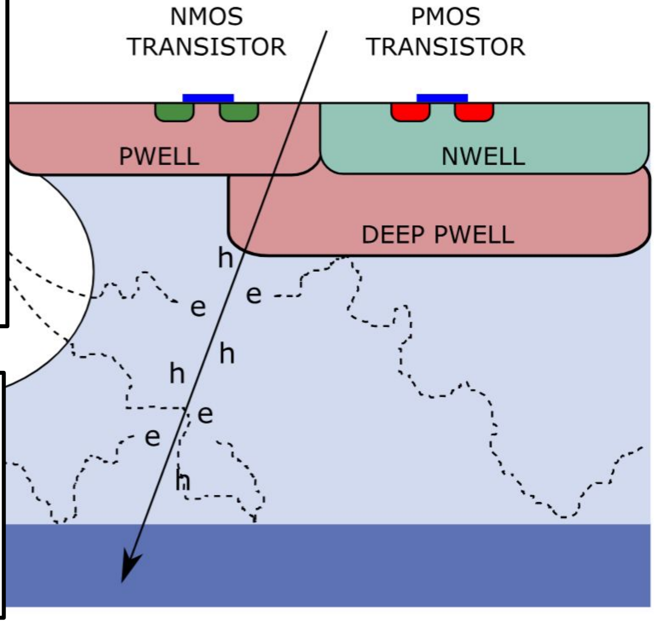

Disadvantages

- ➔ Less radiation hardness
- ➔ Slower readout and timing

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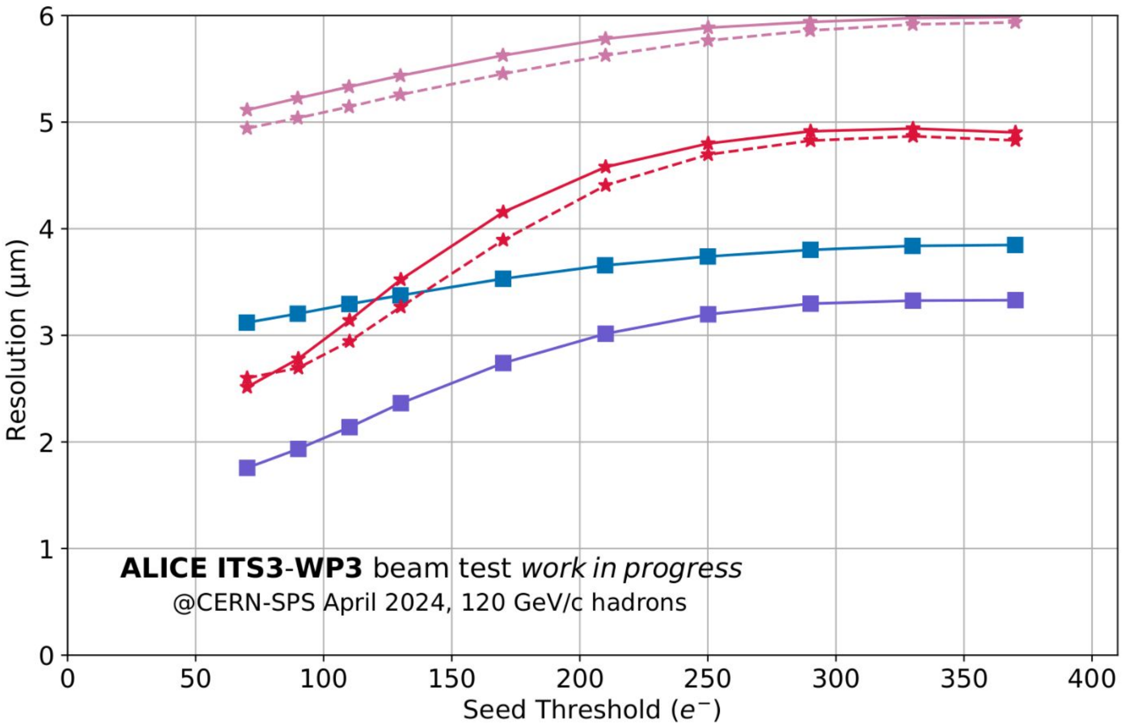
Spatial resolution degrades with RMS

Cluster Method

+ **RMS**



Chip: **CE-65v2** (ER1)
Process: Mod. w/ Gap, Standard
Pitch: 15, 22.5 µm

$V_{sub} = V_{pwell} = 0$ V T = 20 °C
$I_{mat} = 3$ mA, $I_{col} = 200$ µA, $V_{offset} = 1$ V
AC amp.: HV = 10 V, $I_{pmos} = 100$ µA

Modified w/ Gap
- 22.5 µm
- 22.5 µm (Staggered)
- 15 µm

Standard
- 22.5 µm
- 22.5 µm (Staggered)
- 15 µm