


# OCTOPUS:

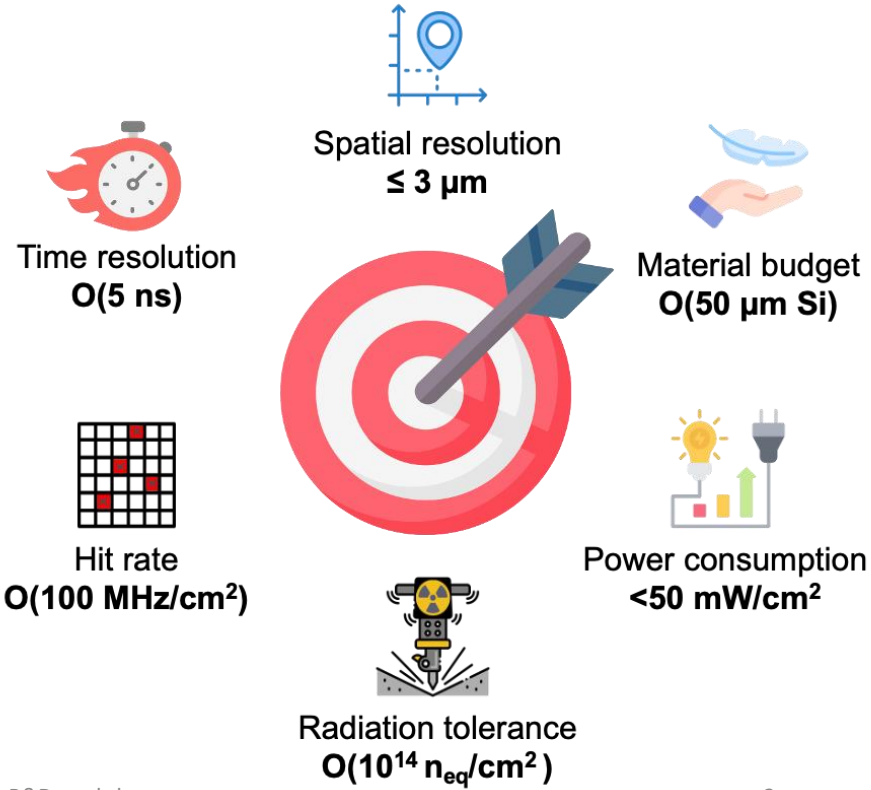
## R&D program towards a vertex detector for the future $e^+e^-$ collider

Serhiy Senyukov (IPHC-CNRS) on behalf of the OCTOPUS project

# OCTOPUS:

## Optimized CMOS Technology for Precision Ultra-thin Silicon

- **Project:** simulate, produce and test MAPS prototypes
- **Target:** reticle-size demonstrator sensor for future lepton collider vertex detectors
- **Requirements:** based on 2021 ECFA detector roadmap
- **Performed in:** DRD3 WG1
- **CMOS process:** TPSCo 65 nm via DRD7.6a
- [https://octopus.web.cern.ch/](https://octopus.web.cern.ch/)



# Intermediate project target:

## New sensor for beam telescopes


Time resolution
~~O(5 ns)~~
**O(100 ns)**

Hit rate
**O(100 MHz/cm²)**

Spatial resolution
**≤ 3 µm**

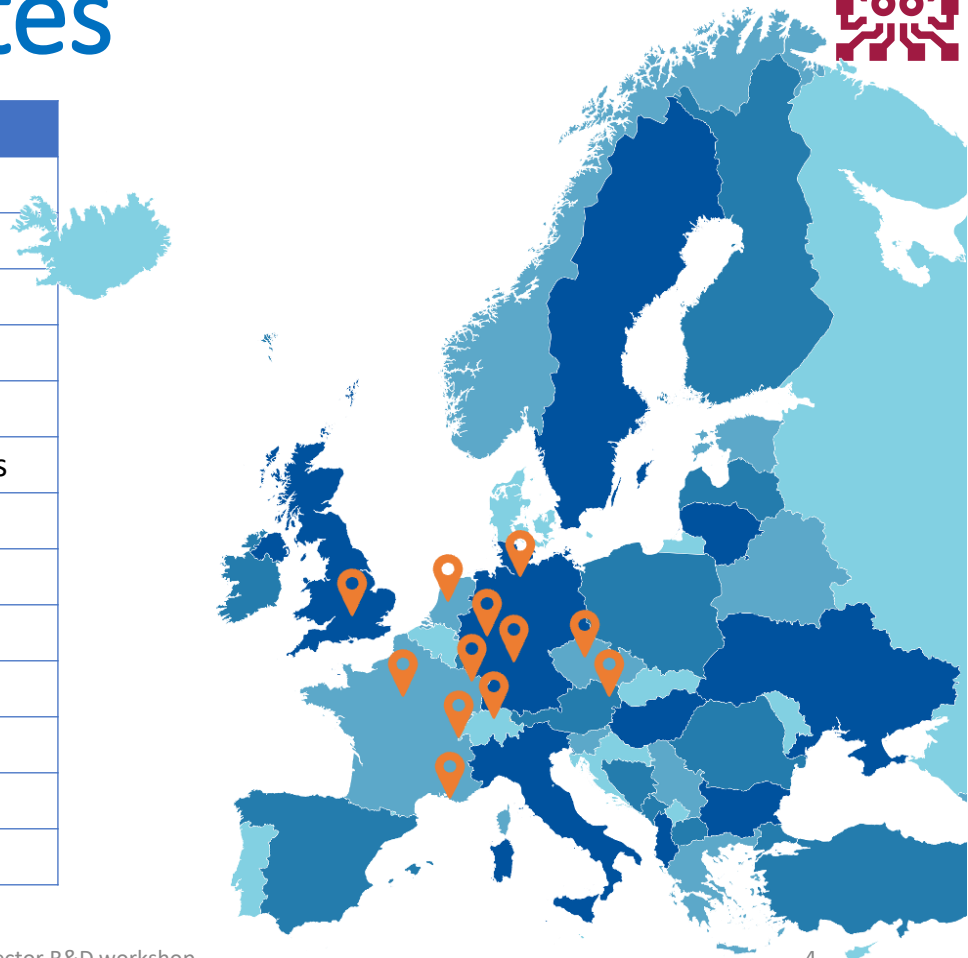
Material budget
**O(50 µm Si)**

Power consumption
~~<50 mW/cm²~~
**<500 mW/cm²**

Radiation tolerance
~~O($10^{14}$ $n_{eq}$/cm²)~~
**not explicitly required**

# 14 member institutes

| Institute | Main areas of contribution |
|---|---|
| APC Paris | Simulations, testing |
| University of Bonn | ASIC design, testing |
| CPPM Marseille | ASIC design |
| NIKHEF | Testing, DAQ |
| CERN | Testing, DAQ, ASIC design support |
| DESY | ASIC design, testing, DAQ, simulations |
| ETH Zurich | ASIC design, testing |
| CTU Prague | ASIC design, DAQ, testing |
| GSI Darmstadt | Simulations, testing |
| MBI Vienna | DAQ, testing, ASIC design |
| IPHC Strasbourg | ASIC design, testing |
| University of Oxford | Powering, integration, testing |
| University of Zurich | Testing, DAQ, simulations |



# 4 working groups

**OCTOPUS project**
S. Spannagel, D. Dannheim

| | | | | |
|---|---|---|---|---|
| **WP1: Simulations**<br>A. Ilg, A. Velyka | **WP2: ASIC design**<br>F. Guezzi, L. Huth, S. Senyukov | **WP3: Data Acquisition**<br>Y. Otarid | **WP4: Testing and characterization**<br>F. King, M. Franks | **System Demonstator (DRD8)** |
| **Task 1:**<br>Sensor optimization / TCAD | **Task1:** Sensor and pixel front-end design | **Activity 1:** Caribou 2 development | **Task 1:** Summary of current 65 nm demonstrator results | **Activity 1:** Concept, design of mechanics & cooling |
| **Activity 1:**<br>Allpix$^2$ development | **Task 2:** Matrix architecture & readout design | **Task 1:** Chipboard design for prototypes | **Task 2:** Lab characterization, FE optimization, calibration | **Activity 2:** Design & Construction of beam telescope |
| **Task 2:**<br>Detecor performance / Allpix$^2$ | **Task 3:** Periphery, DACs & slow control | **Task 2:** FW and SW integraton of prototypes | **Task 3:** Testbeam caracterization, simulation comparison | **Activity 3:** Prototype construction |
| **Activity 2:**<br>Physics performance / Geometry optimization | **Task 3:** Trancievers & readout design | **Task 3:** Chip / board assembly, bonding & logistics | **Activity 1:** Sensor irradiation & testing | |
| | **Activity 1:** Submission coordination & DRD7 liason | | | |

# WP1: Sensor optimization

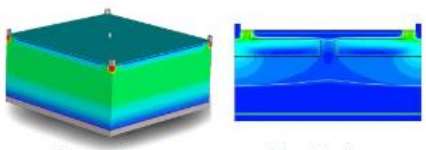
**Tech-independent simulation framework:**

- TCAD – sensor simulation
- Allpix squared – particle interaction, signal propagation

**Aim: 3 µm resolution with full efficiency**

- Large parameter space:
  - Process variants
  - Pitch
- Trade-off between:
  - Charge sharing
  - Efficiency
  - Timing
- Existing TPSCo 65 test results used to benchmark simulations

Sentaurus TCAD SYNOPSYS® Silicon to Software™



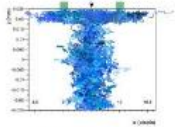
Generic doping profile

Realistic electric field

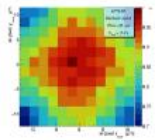
Weighting potential

ap² allpix squared

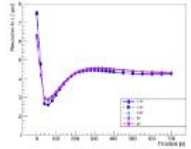
Particle interaction



Induced Signal



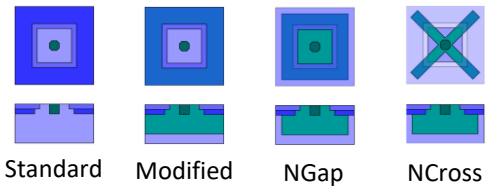
Efficiency

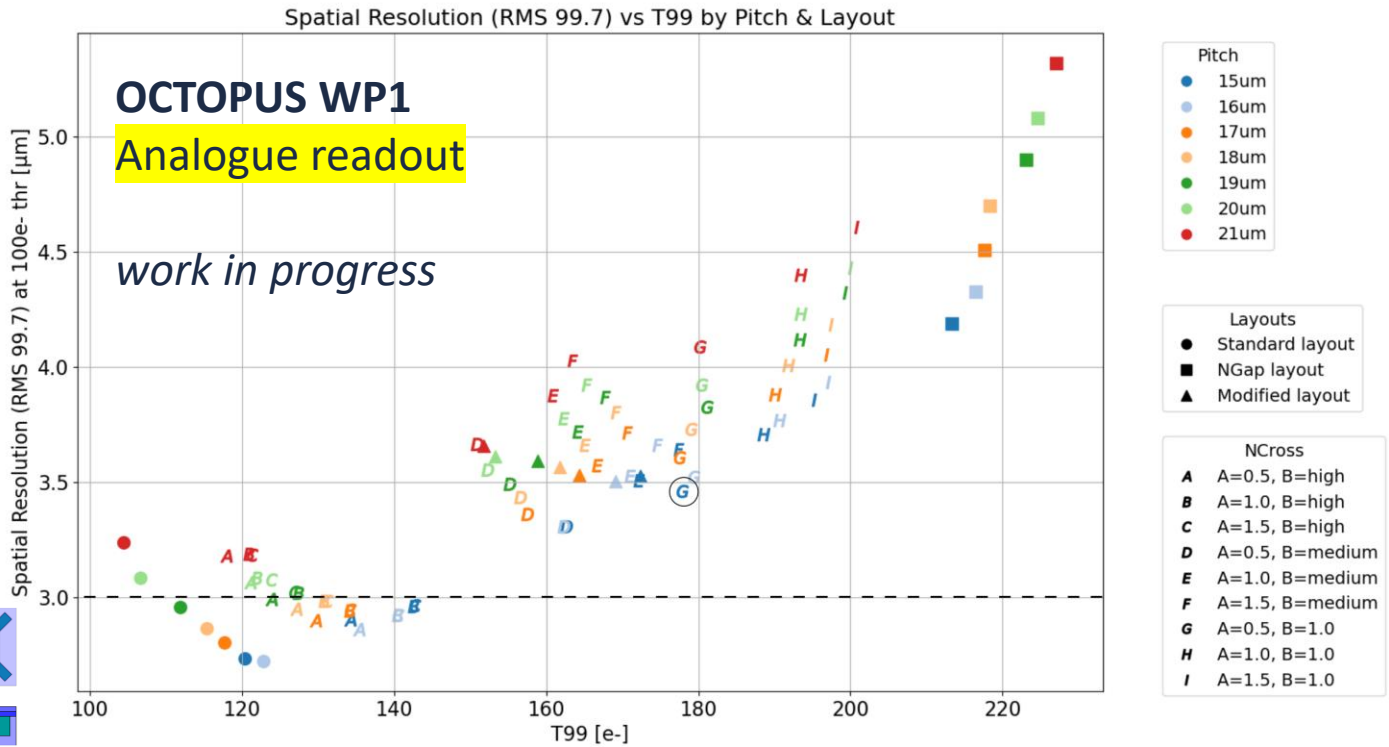


Spatial resolution

# WP1: Novel layout - NCross

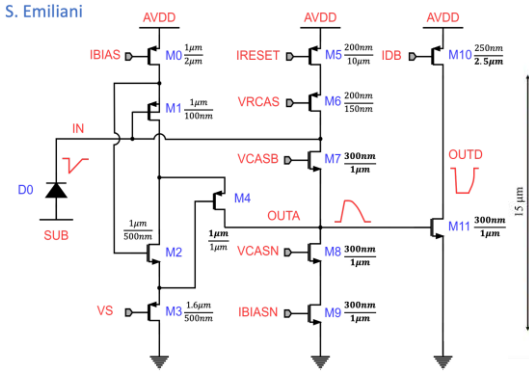
- **Novel cross shaped layout (Ncross) provides 3 µm resolution at 18-20 µm pitch**
- New layout may be implemented in the next TPSCo 65 nm submissions (2026-2027)

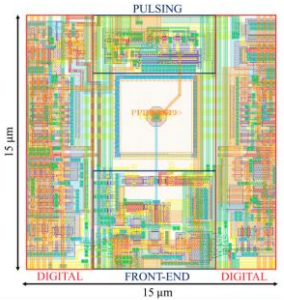


# WP2: Pixel front-end

- MOSAIX (ALICE ITS3) frontend as a starting point of development
  - Previous versions proven in silicon (DPTS/MOSS)
  - Compact footprint
  - Significant time walk at low power
- Time stamp for rising and falling edge needed for:
  - Time walk correction
  - Charge interpolation for spatial resolution
- Alternative front-ends are under consideration (e.g. CSA from H2M)

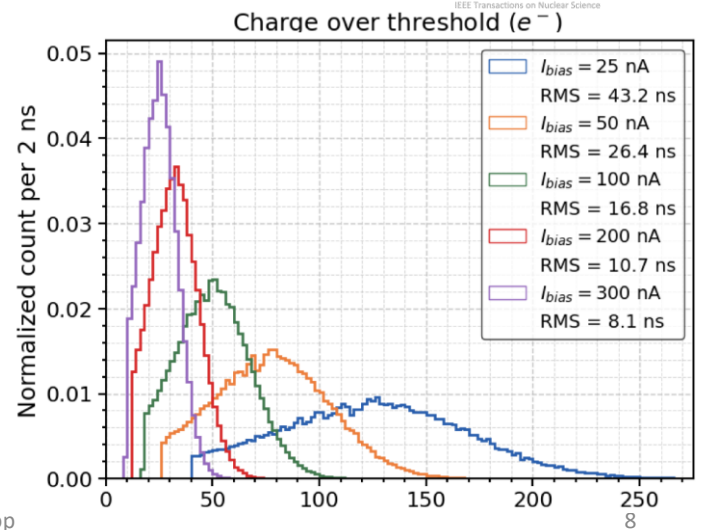



DPTS Pixel: 15 µm x 15 µm

F.Piro, A Compact Front-End Circuit for a Monolithic Sensor in a 65-nm CMOS Imaging Technology, 09.09.2023, IEEE Transactions on Nuclear Science

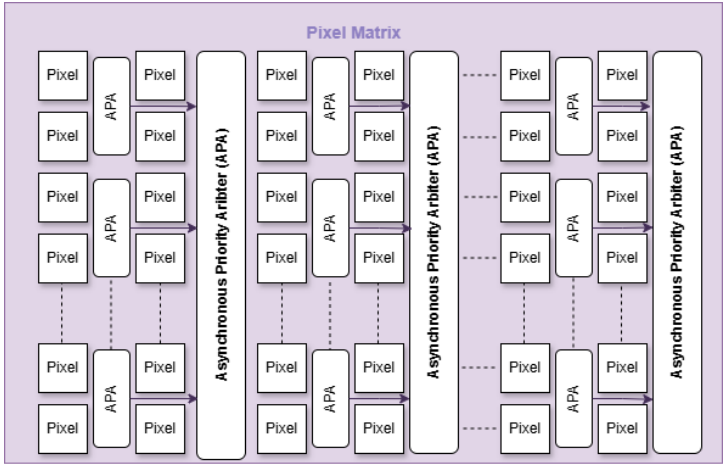
https://indico.cern.ch/event/1461789/

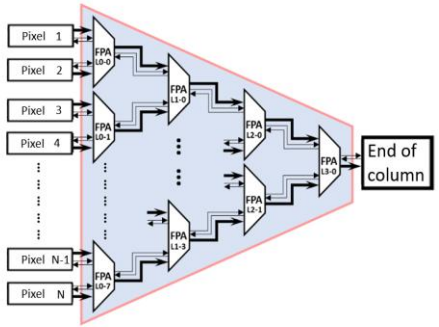


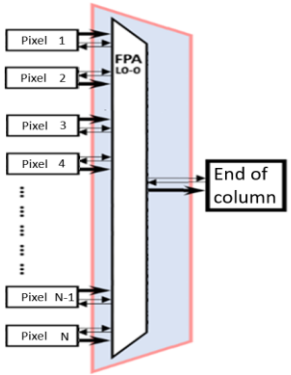
# WP2: Matrix readout

## APA – Asynchronous Priority Arbiter

- Pixels are grouped in double columns
- Hits are propagated via APA tree to the periphery asynchronously (no clock)
- Time ordering of hits is preserved
- Expected time resolution: 5 ns
- Evaluating the best tree topology in-between
  - Many 2:1 (better bandwidth)
  - One N:1 (Less area)
- SPARC chip (ER2) to be tested in 2026 to verify the performance of the architecture

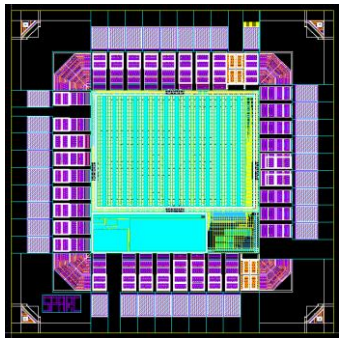


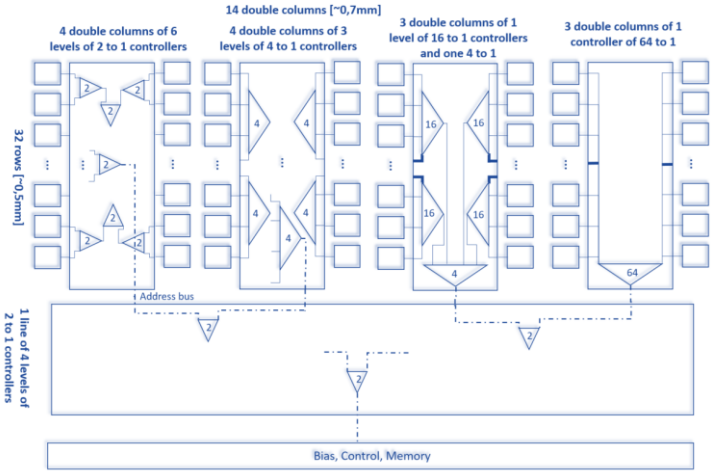



# SPARC: first prototype of asynchronous readout

- Pixel matrix: 32 × 28
- Pixel pitch: 24 × 16 µm$^2$
- Pixel front-end: DPTS-like (CERN)
- FPA tree types: 2:1, 4:1, 16:1, 64:1
- Power dissipation: 5 mW/cm$^2$
- Mean readout time: 6.3 ns
- Designed by: IPHC, IRFU
- Submission: summer 2025 (ER2)
- Test system in preparation for 2026

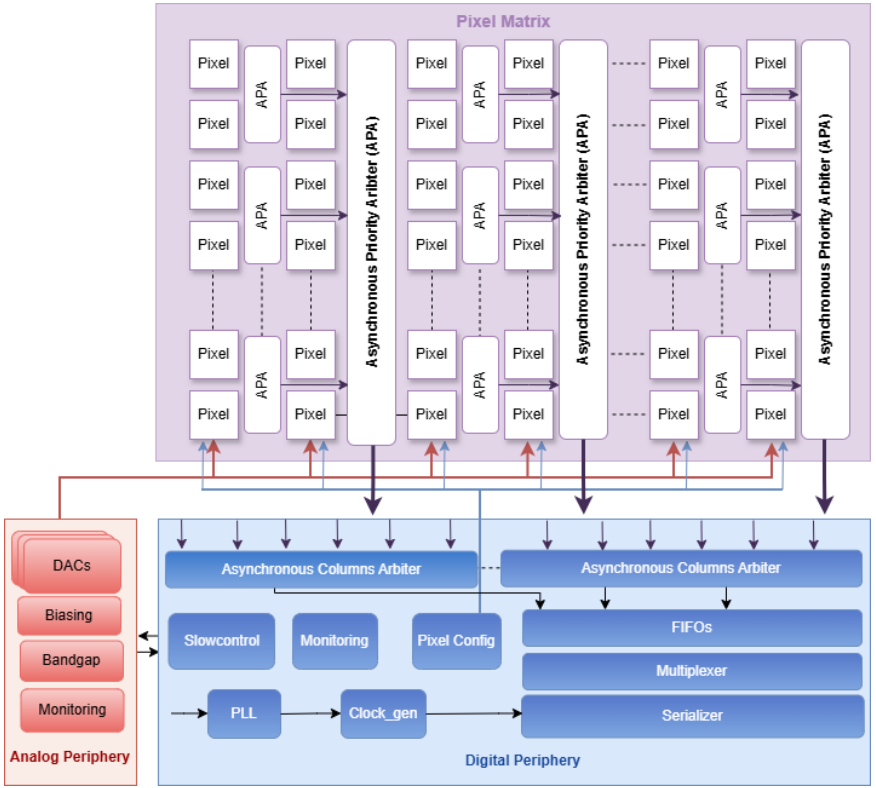


1.5×1.5 mm$^2$



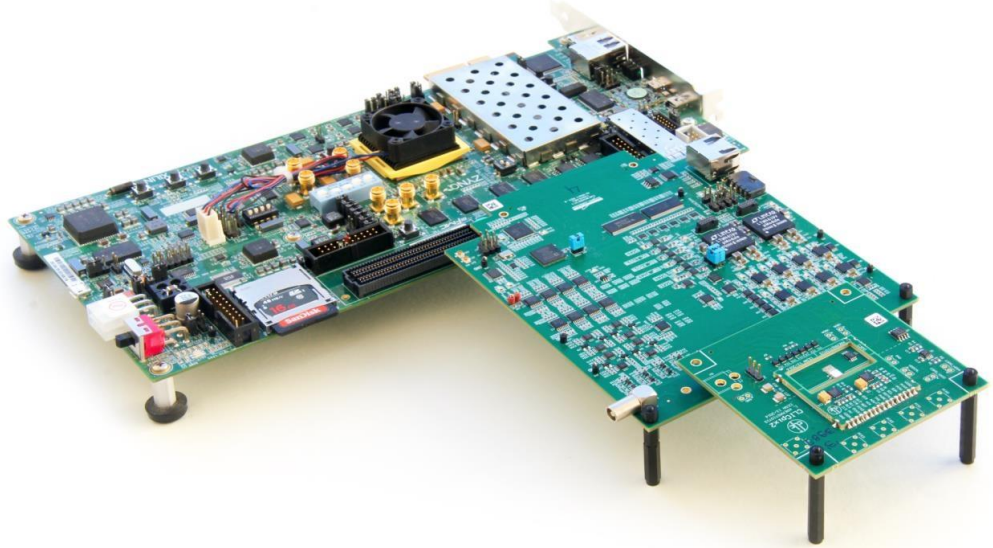
# WP2: Chip periphery and layout

- Time stamping for ToA and ToT via TDC in the end-of-column
- 4 level event buffer
- Various options for column merging are studied with simulations
- Serialization and data packaging by in-chip lpGBT logic
- Expected output data rate: 10 Gb/s per $cm^2$



# WP3: DAQ for OCTOPUS

- **Caribou** – open modular DAQ platform for testing silicon pixel detectors. Already used for various projects:
  - H2M, ATLASpix, APTS, DPTS, etc.
- **Hardware components:**
  - SoC board (3000 €)
    - Embedded CPU runs DAQ
  - CaR board (800 €)
    - Power supply
    - Data and control links
  - Chip board (100 €)
- First use in OCTOPUS
  - Test of SPARC chip (from 2026)



# WP4: Test and characterization

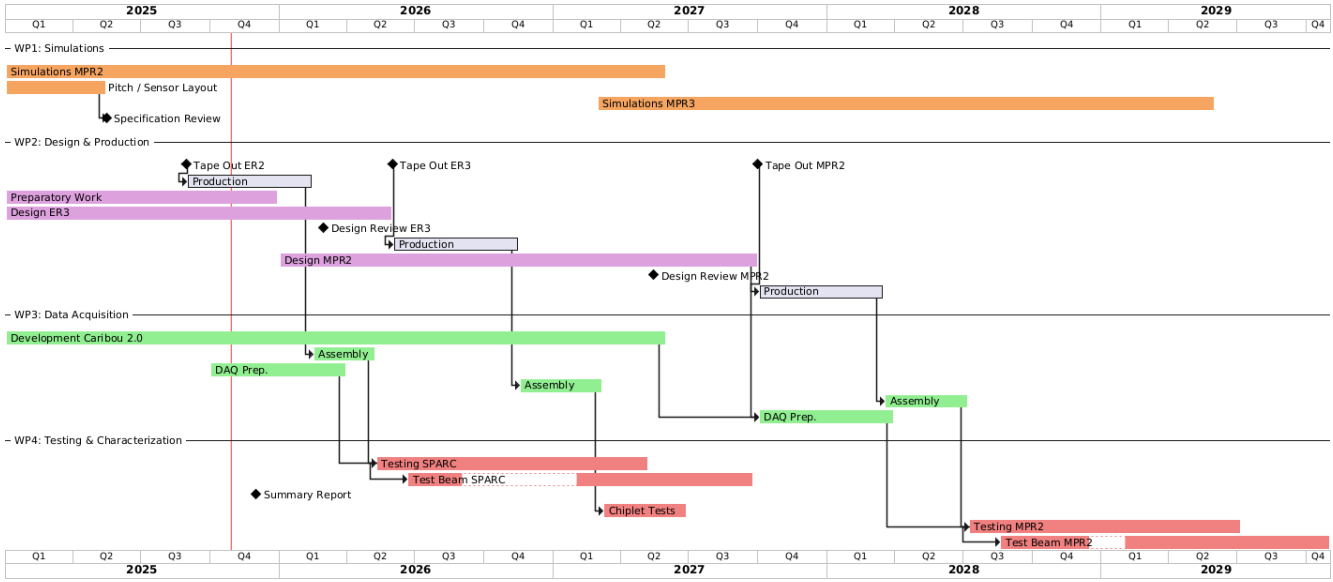
- **2025:** Finalizing summary report of current results of TPSCo 65 nm prototypes. Publication submission by the end of the year
- **2026:** SPARC characterization
  - Lab test in several institutes with Caribou DAQ
  - 2-3 weeks of the test beam in summer (CERN and DESY)
- **>2026:** Possible characterization of Ncross layout with APTS chips of ER2-respin or ER3.
  - Discussion ongoing with DRD7.6a on possible submissions

# Project timeline

Project schedule largely depends on the TPSCo 65 nm submissions organized by DRD 7.6a

Current targets:

- ER3 (2026) - several “chiplets” (1.5×1.5 $mm^2$) to test individual blocks
- MPR2 (2027) – full column prototype (2 × 1 $cm^2$)



# Summary and outlook

- OCTOPUS project aims to build a MAPS prototype for the vertex detector for future lepton collider
  - Spatial resolution: 3 µm
  - Time resolution: 5 ns
  - Power consumption: < 50 mW/cm$^2$
  - Hit rate: 100 MHz/cm$^2$
- Targeting ER3 and MPR2 submission in 2026/27 for the first prototypes in TPSCo 65 nm process
- Preparation for testing async readout using SPARC chip in 2026

# Thank you!