Fermilab

October 30, 2025

Status and plans for sensor developments at Fermilab

Artur Apresyan

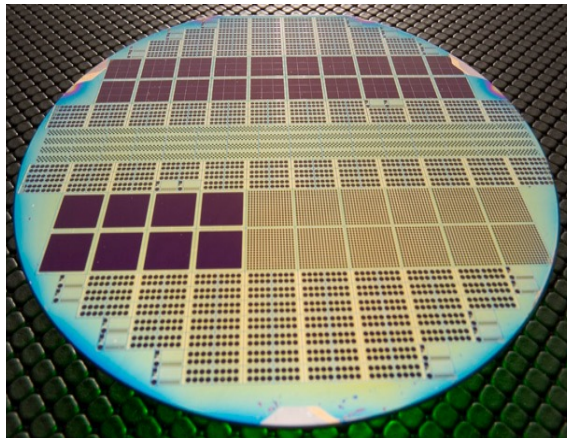
FCC-ee vertex detector R&D workshop

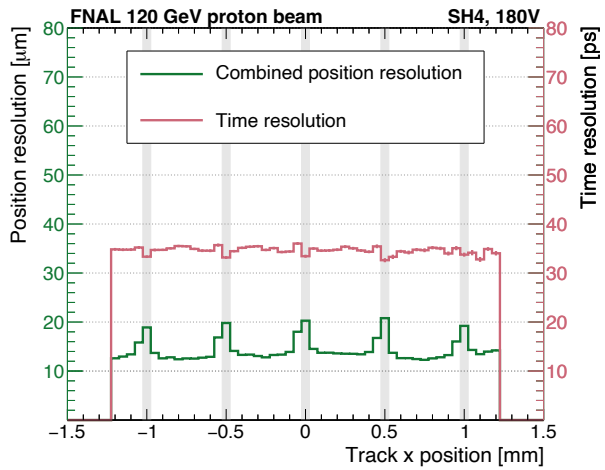
U.S. DEPARTMENT of ENERGY

Fermi National Accelerator Laboratory is managed by FermiForward for the U.S. Department of Energy Office of Science

Projects at Fermilab

- Build on technologies developed at the lab for Tevatron, LHC, HL-LHC, EIC, and others
  - Unique resource of strong instrumentation groups
  - Expertise in physics simulations and tracking reconstruction
- Fermilab is actively engaged in R&D on sensor designs towards FCC
  - Sensor design, simulation studies, collaborations with vendors
  - Collaborative efforts with US and international universities





AC-coupled LGADs

- **Improve 4D-trackers to achieve 100% fill factor, and high position resolution**
- An evolution of DC-LGADs
  - Excellent time resolution achieved across full sensor surface
  - Charge sharing enables excellent position resolution without fine pixelation

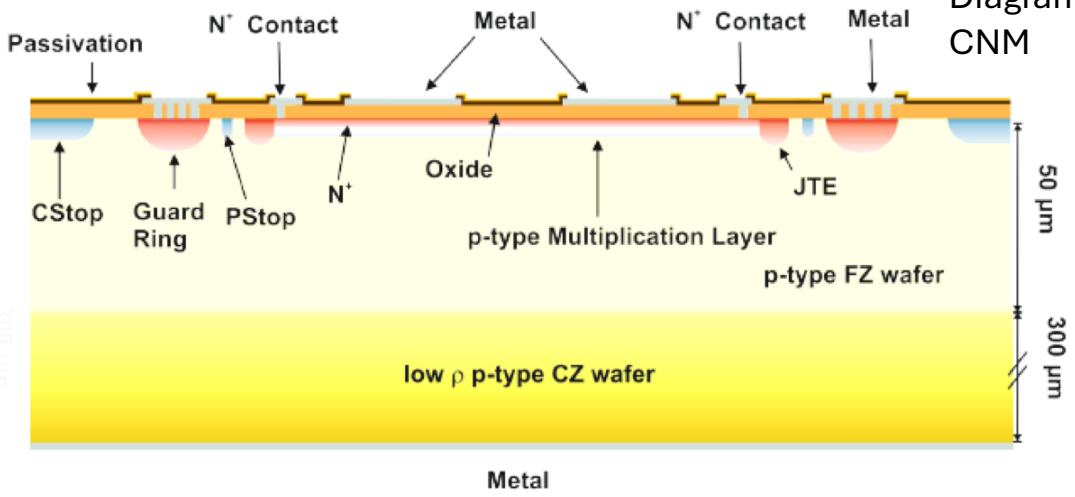
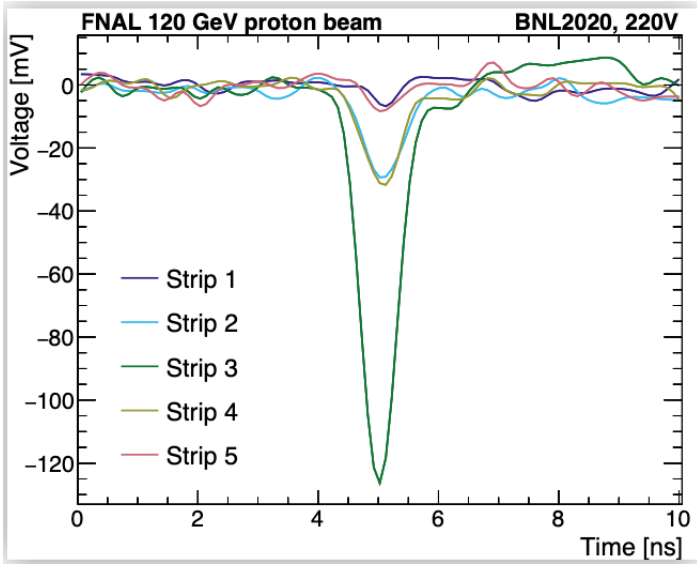


Diagram credit: CNM

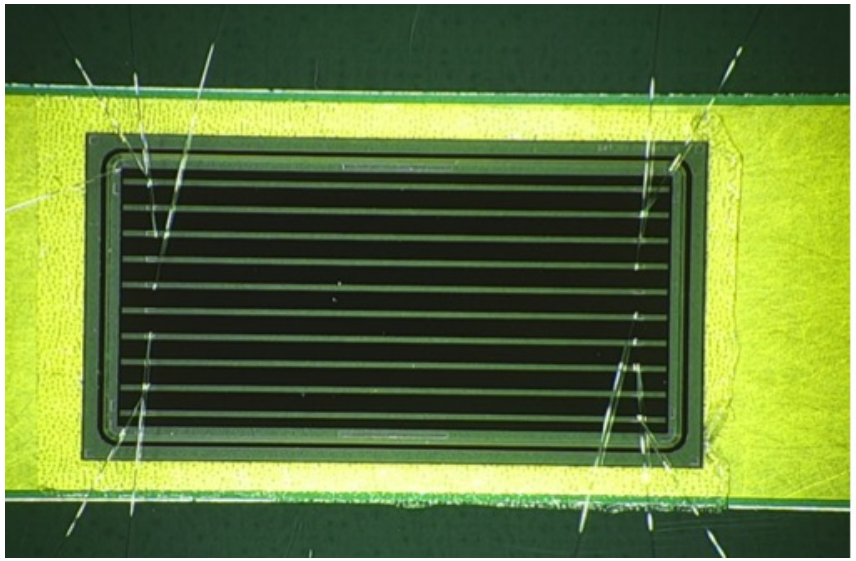
AC-LGAD



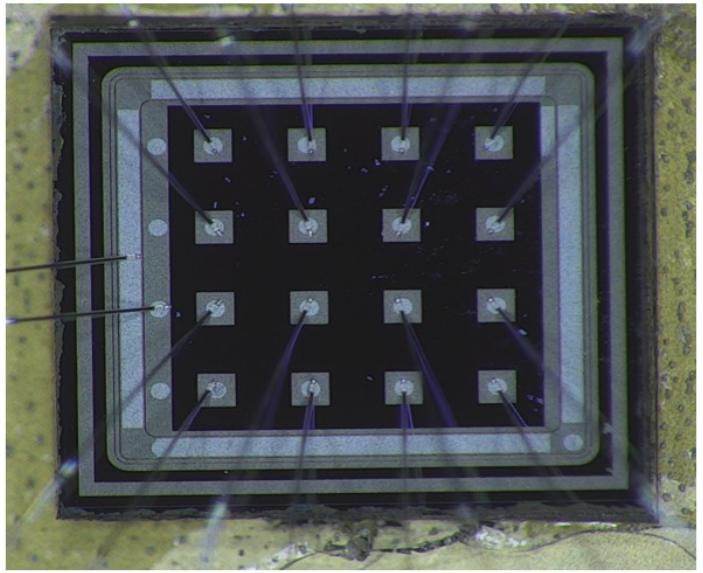
Signal sharing allows for improved position resolution

Sensor optimization for strip AC-LGADs

- Several rounds manufactured over the last few years
  - R&D from developments for HL-LHC, synergies between HEP and NP
  - Optimize position resolution, timing resolution, fill-factor, …
- Extensive characterization and design studies



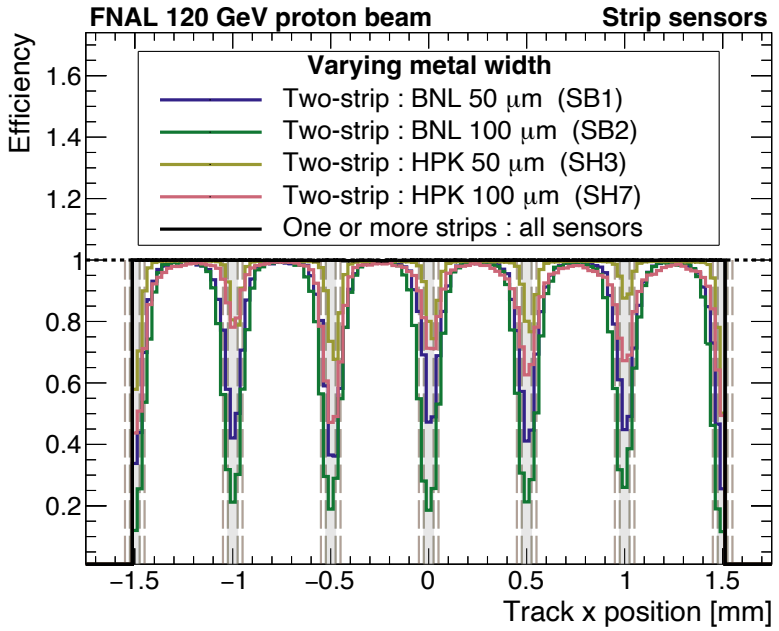
Photographs of some of the HPK AC-LGAD strip devices tested in this campaign



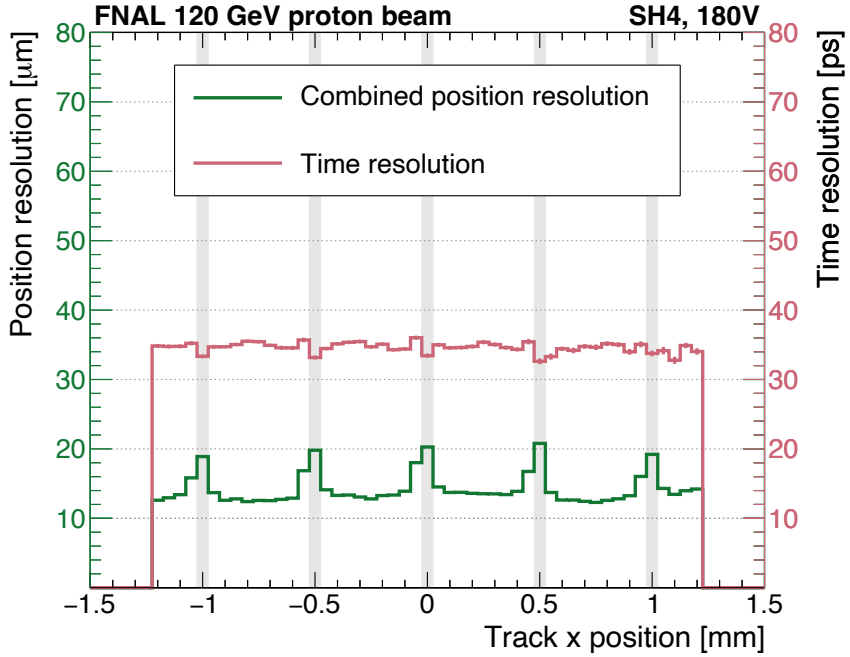
Photographs of the BNL AC-LGAD pixel devices tested in this campaign

Sensor optimization for strip AC-LGADs

- Position reconstruction
  - Achieve 15-20 µm resolution in 10mm strips, 500 µm pitch
- Exacellent time resolution
  - Achieve 30-35 ps for 10 mm strips



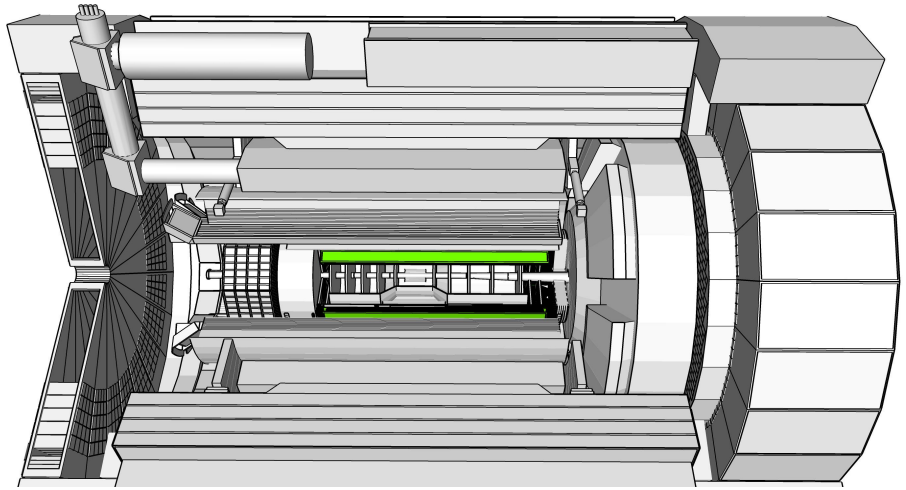
Detection efficiency across surface



Position and Time resolutions across surface

ePIC barrel TOF

- The ePIC detector is a multipurpose collider detector for EIC
- Need particle ID down to low energies and across all rapidities
  - Strip sensors in the barrel: **first time strips LGADs** will be used
  - Very similar to the idea of Silicon Wrapper with precision timing



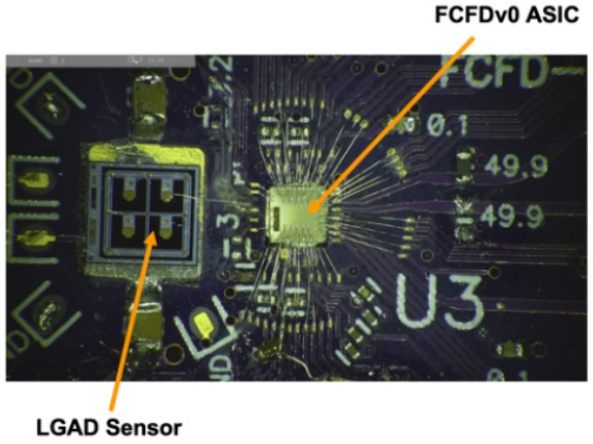
	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10	0.5*10	2.4M	30 ps	30 μm in $r \cdot \varphi$	0.01 X0
Forward TOF	2	0.5*0.5	8.8M	25 ps	30 μm in x and y	0.05 X0
B0 tracker	0.07	0.5*0.5	0.28M	30 ps	20 μm in x and y	0.01 X0
RPs/OMD	0.14/0.08	0.5*0.5	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

Requirements on timing and spatial resolutions and material budget are still being evaluated and are subject to change as the design matures, and we will continue to explore common designs for these detectors where possible to reduce cost and risk.

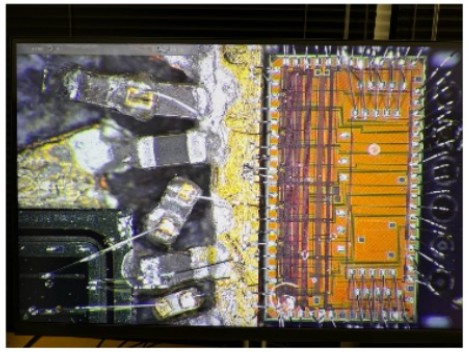
Fermilab Constant Fraction Discriminator Chip (FCFD)

- A readout chip for AC-LGAD sensors based on CFD
  - Developed in TSMC 65 nm technology node
  - **All current** ASICs need time-walk correction: each pixel timing needs to be corrected offline : continuous monitoring and corrections needed
  - CFD: **No need for time-walk** correction : directly get time-measurement
- Can be used for many types of precision timing detectors

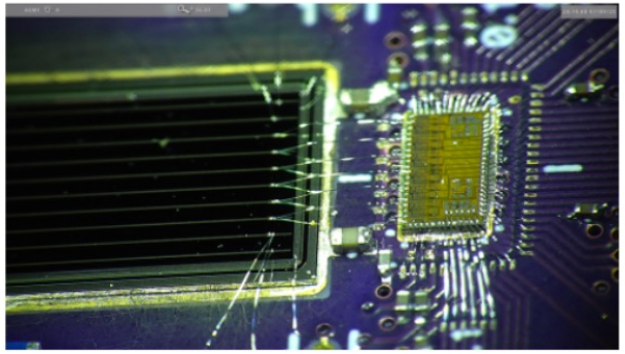
FCFD0



FCFD1



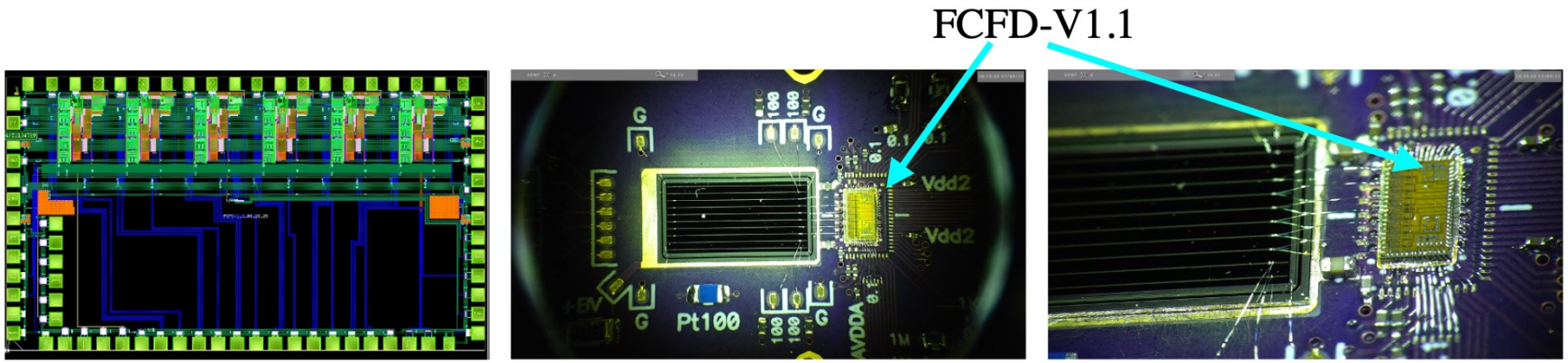
FCFD1.1



CPAD 2023: https://indico.slac.stanford.edu/event/8288/contributions/7544/
* CPAD 2024: https://indico.phy.ornl.gov/event/510/contributions/2148/

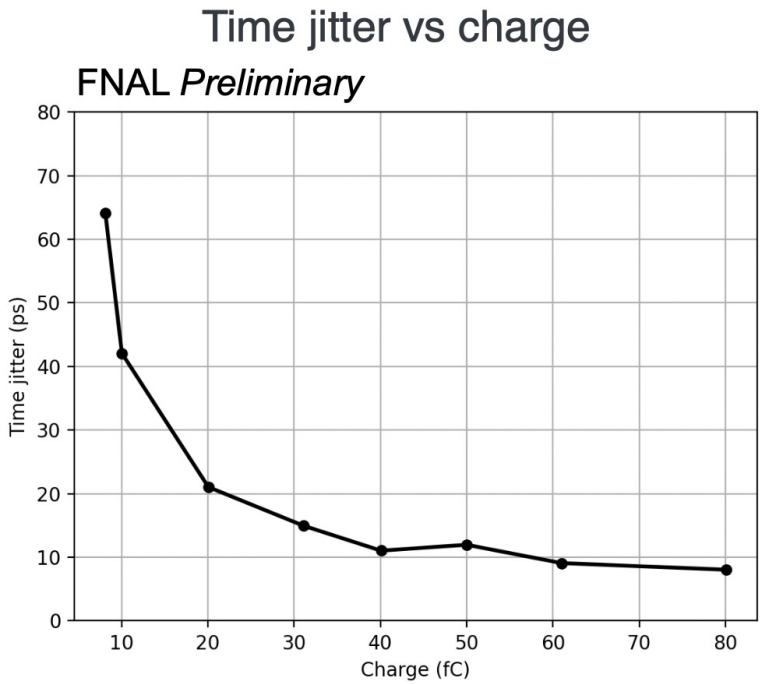
FCFD-V1.1 — latest version

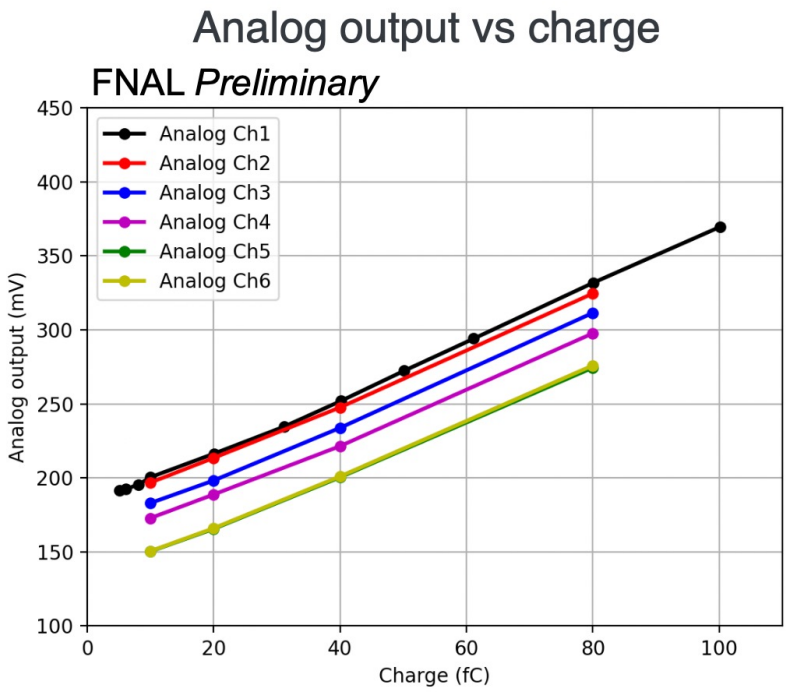
- **Design specs:**
  - Hamamatsu 1 cm long strips, 50 µm thick sensor
  - 500 µm pitch, 50 µm wide metal strips
  - Sheet resistance 1600 Ω/square
  - Dynamic range: 10 - 70 fC; signal MPV : 25 fC
  - Jitter at MPV : around 20 ps
- Chip **submitted on Feb 19, 2025,** received in Fermilab in **June 2025**.
- Wire-bonded to a HPK 1-cm strip sensors, 500um pitch, 50um metal electrode



FCFD - Laboratory measurements

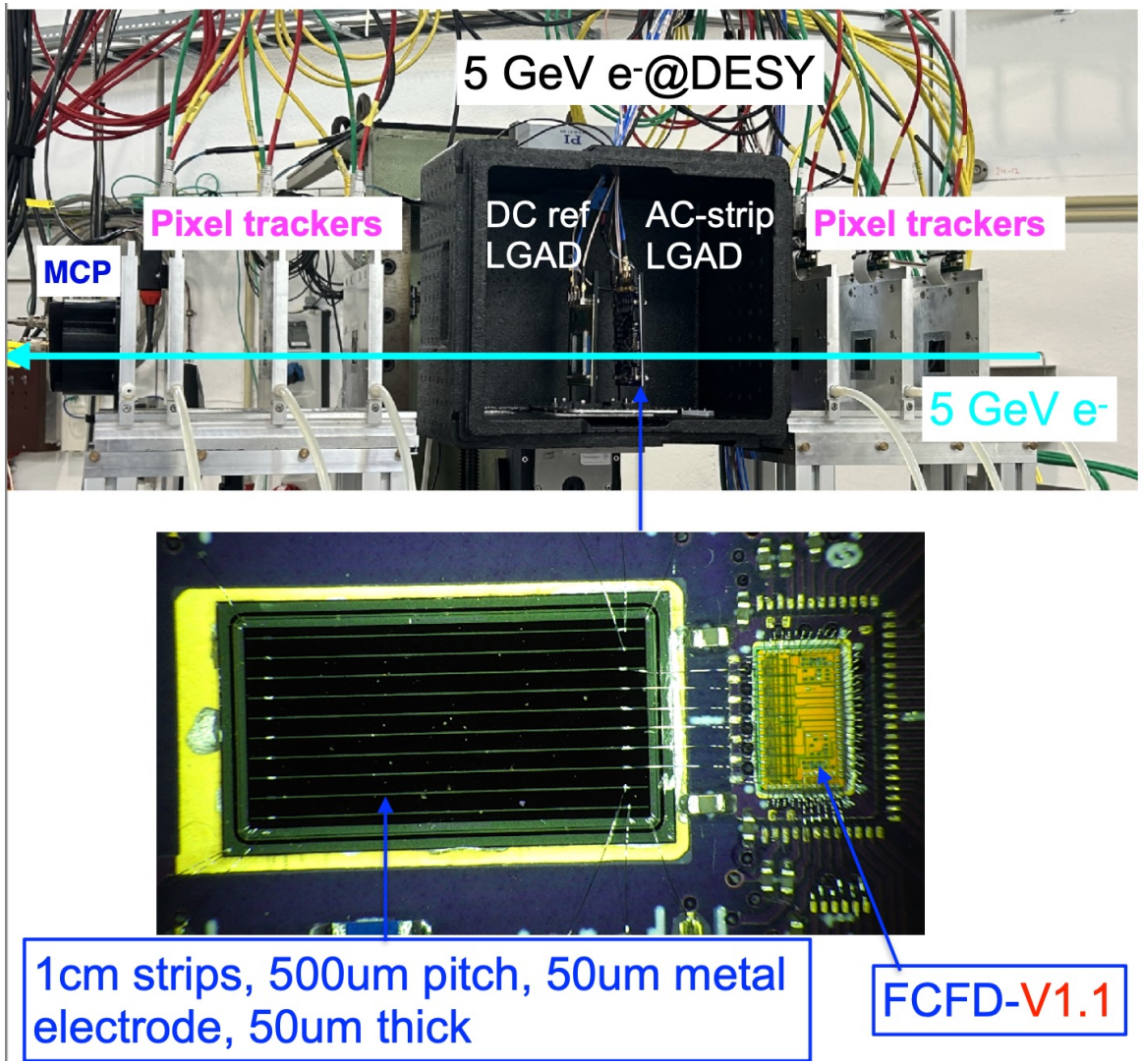
- Charge injection measurements:
  - Jitter measurements consistent with simulation and specs
  - Amplitude measurements: all channels behave as expected, linear in the range





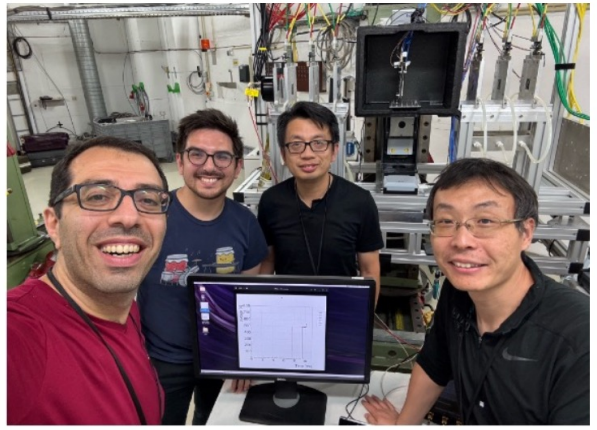
FCFD test beams in 2025

2 test beams in summer 2025 at DESY (5GeV e-) and CERN (120GeV p)



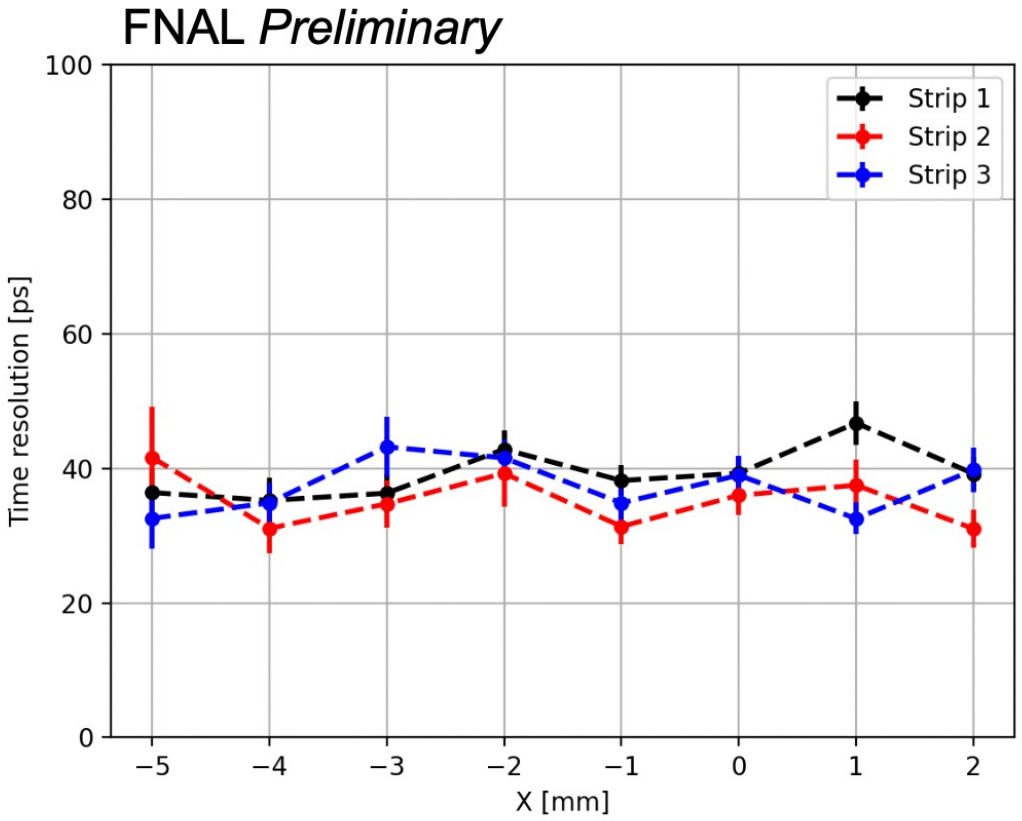
- Tracking with ~5 µm resolution
- Time reference detector with ~ 10 ps resolution (MCP)
- DAQ: high bandwidth, high ADC resolution 8-channel scope

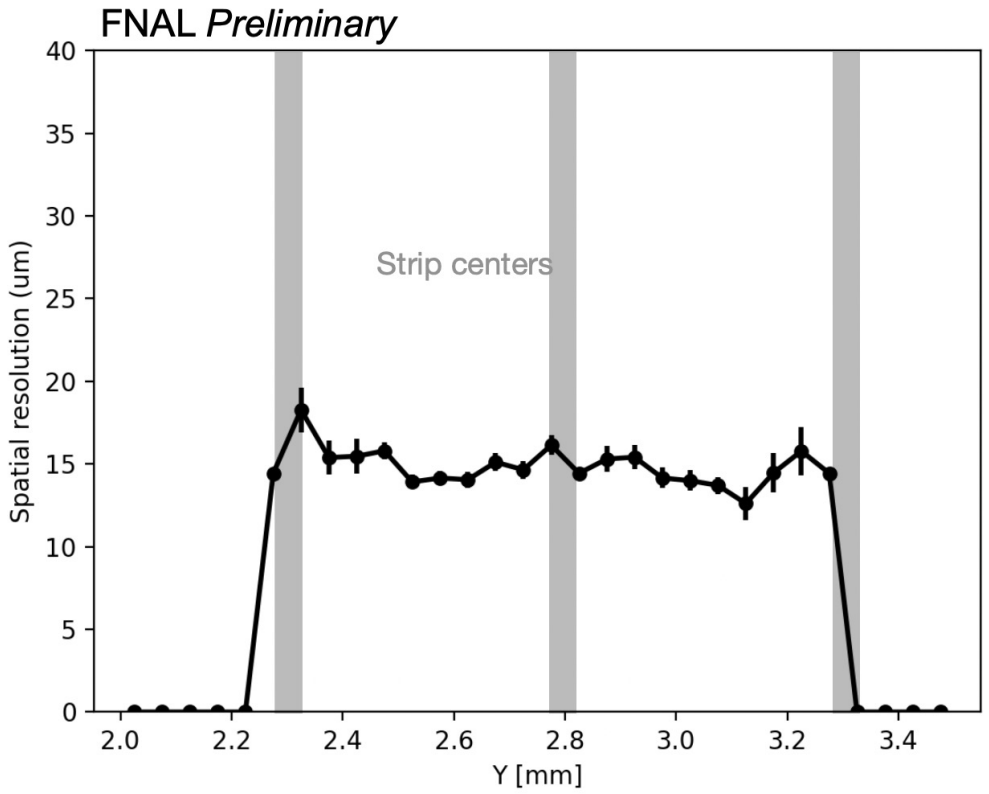
crew@DESY (July, 2025)



FCFD - Results from the beam tests

- Demonstrated performance in beams, meeting specifications:
  - ~40 ps time resolution over the entire sensor area
  - 15 μm spatial resolution



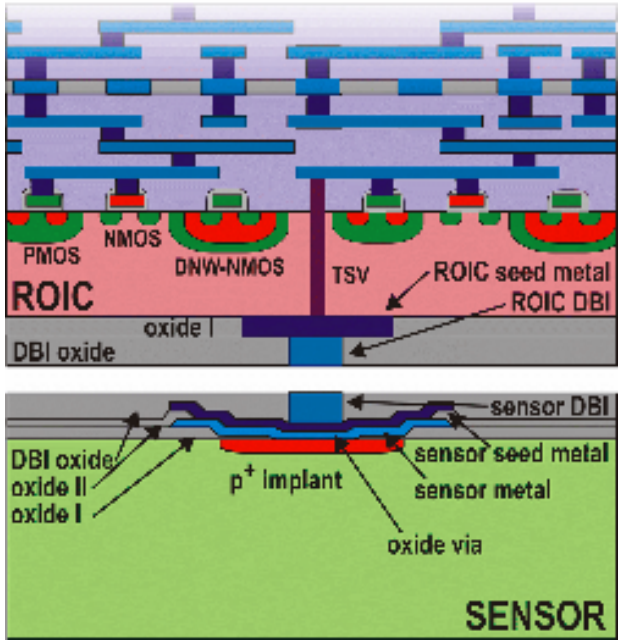


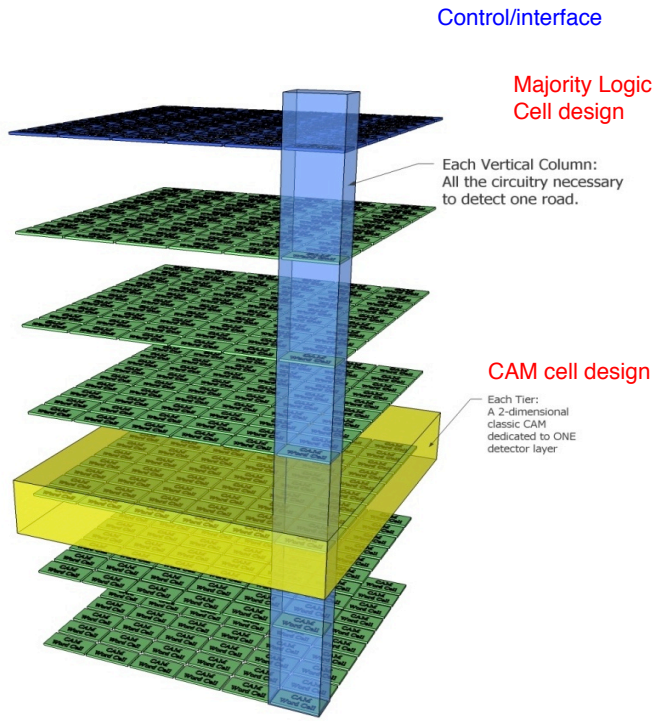
3D-integrated pixel detectors

- Low-power, highly granular detectors in (***x***, *t*)
  - Adoption of 3D-integration has been cost-prohibitive in academia

- Supported by DOE “Accelerated Innovation in Emerging Technologies”
  - Joint development effort of SLAC, FNAL and LLNL
  - Partner with industry leaders to implement new technologies
  - Design goal: position resolution ~5 μm, timing ~ 5-10 ps

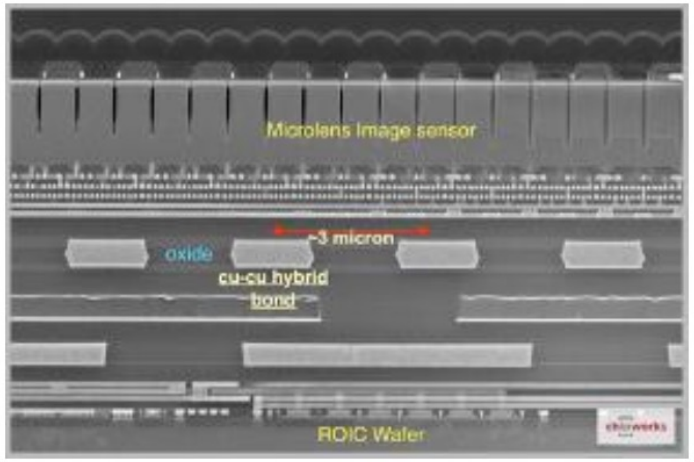
- Can be a candidate for vertex detectors





3D project

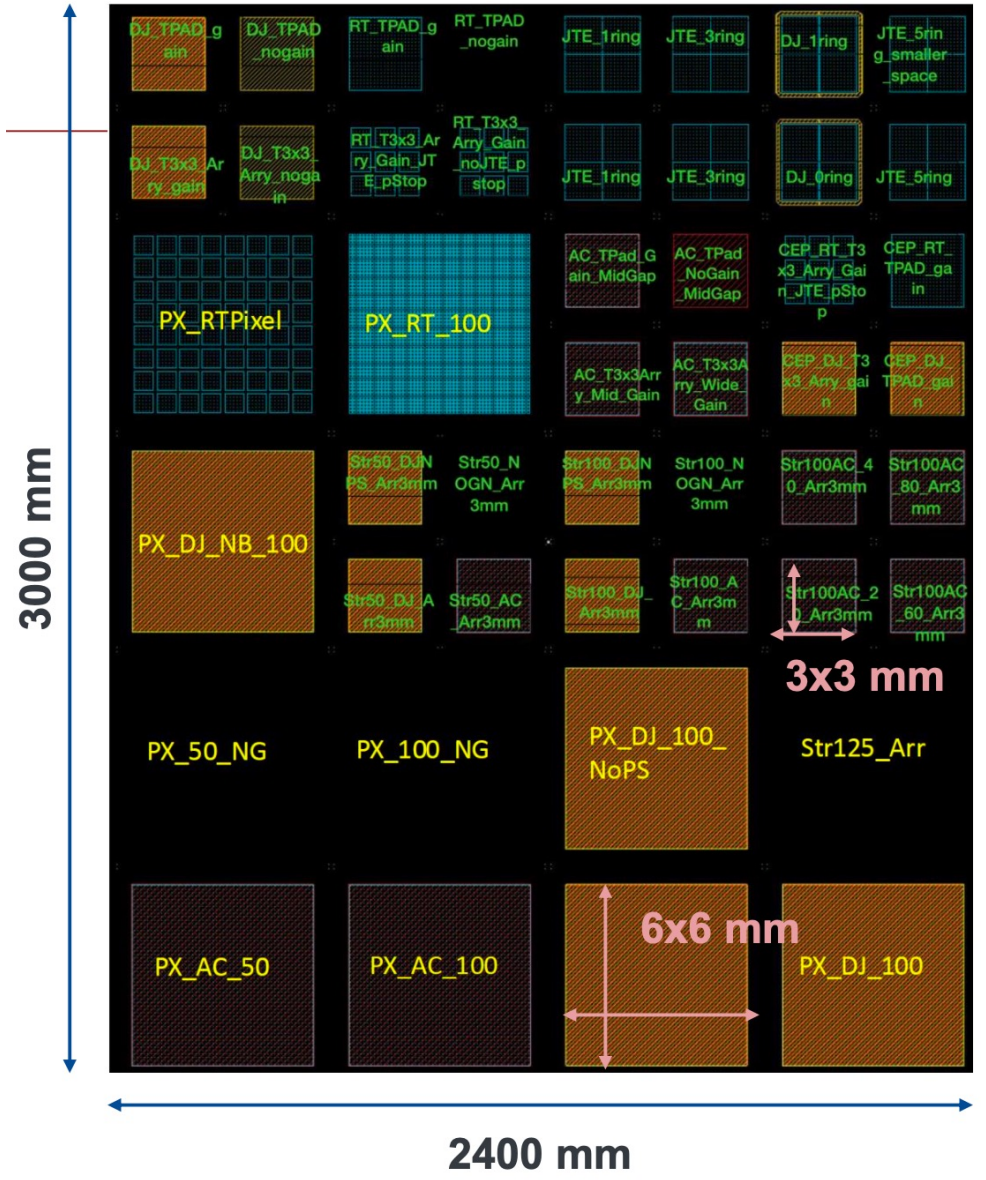
- The research program consists of three main thrusts towards developing the proposed detector:
  - **Thrust 1:** *Design and manufacture Low-Gain Avalanche Diodes (LGADs) devices compatible with **12" foundry processes : NEVER DONE BEFORE***
  - **Thrust 2:** *Design application specific integrated circuit (ASIC) techniques to meet various application needs for granularity, precision timing, and power**: 28 nm design***
  - **Thrust 3:** *Enable a new generation of particle detectors that utilize **3D-integration**: **BECOMING STANDARD IN INDUSTRY***



Section of the Sony Exmor camera chip showing the hybrid bond interface

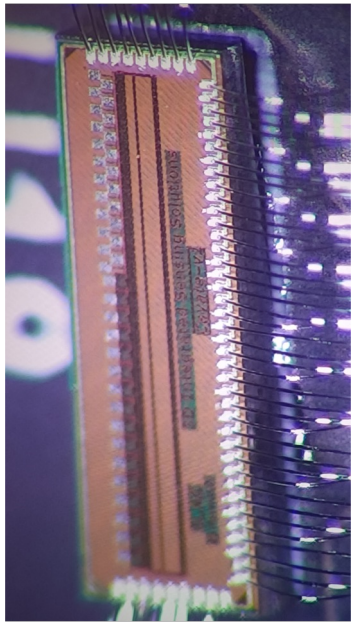
3D project : sensor development

- Development in partnership with Tower Semiconductor
  - Wafer run: 12” in 65nm process
  - **First LGAD process on 12” wafers**
- Optimize doses, energies, edge termination strategies
  - Standard CMOS process forces constraints on detector design
  - E.g. define active regions to exclude STI, metal density and spacing, angles restricted to 45° and 90°, etc…

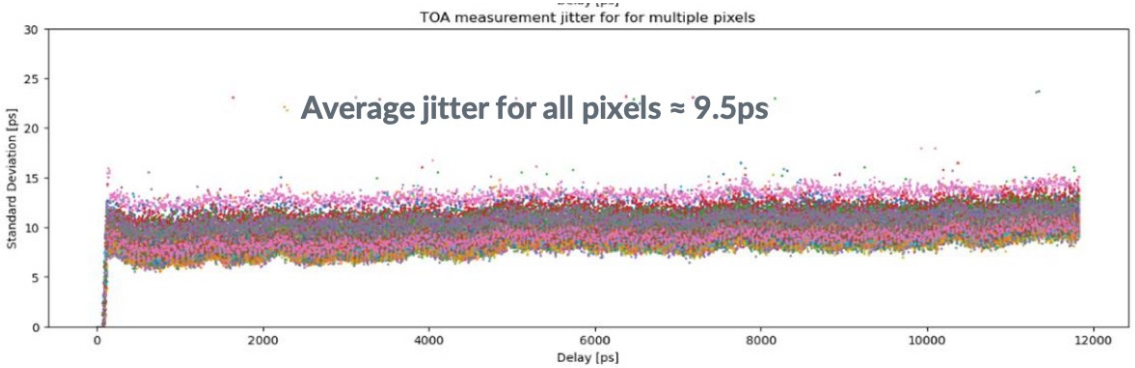


3D project: readout ASIC

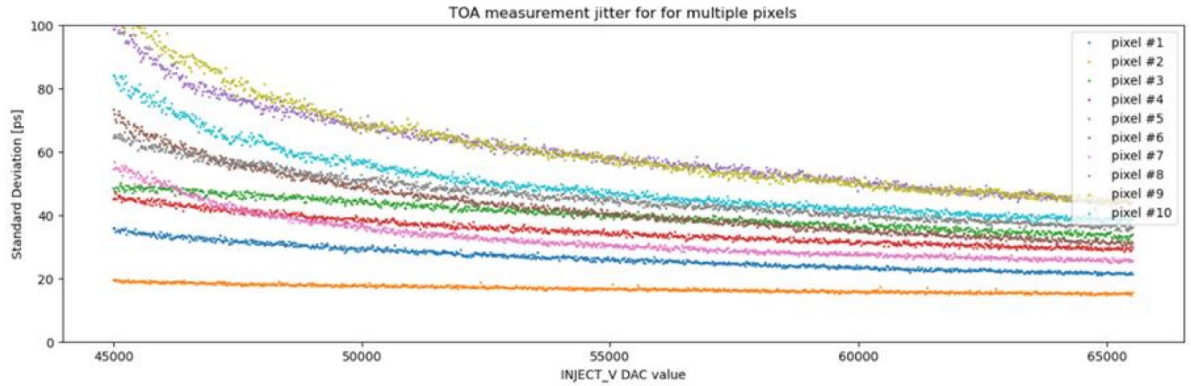
- First 28nm readout ASIC prototype (1x3 mm^2)
  - Variants of 50μm and 100μm size pixels
- Test main ingredients for full chip integration
  - TDC prototype demonstrated full system jitter around 10 ps
  - Analog frontend demonstrated to achieve 20 ps jitter



First readout ASIC prototype, TSMC 28 nm



Performance of the TDC



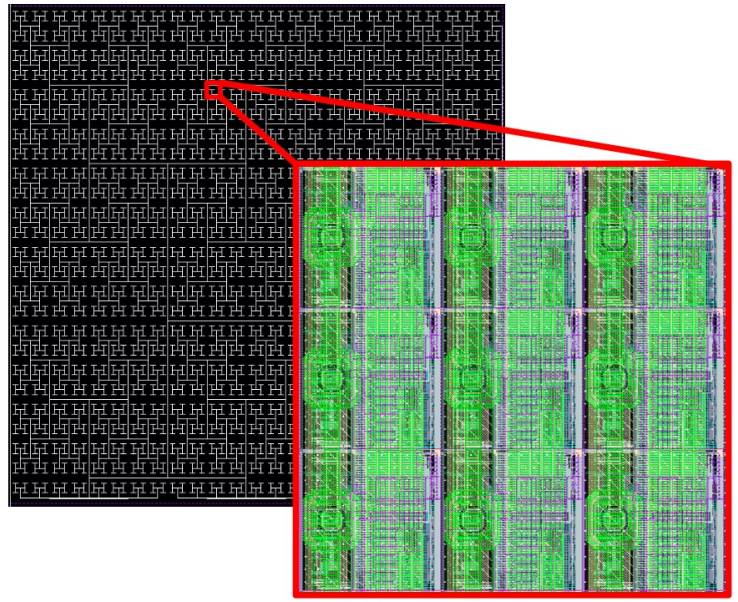
Performance of the Analog FE

3D project: readout ASIC 2nd prototype

- 2nd prototype in 28nm submitted in September 2025
  - THRIGLAV: THRee-d InteGrated LgAd driVer
- (5x6 mm^2) with 100x100 array of 50μm pitch pixels
  - Optimization of pixel blocks based on feedback from MPW1
  - Digital control and readout logic design, fast IO driver.
  - At the end of 2nd year, we anticipate first demonstration of 28nm readout chip bump-bonded to the prototype LGAD array with high-precision timing performance.
- For the next project phase, we would proceed to wafer-to-wafer bonding of 12” LGAD and 12” 28nm ASIC wafers.

THRIGLAV v1

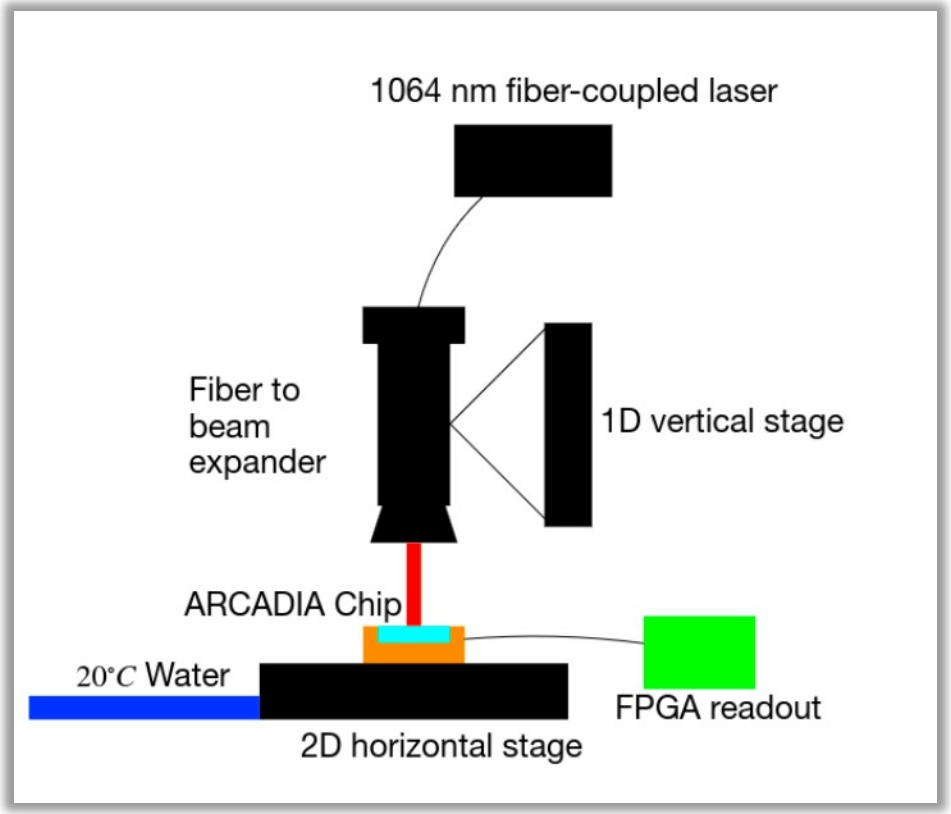
SLAC Fermilab



Layout of the pixel matrix highlighting the clock distribution three with zoom on 3x3 pixel region

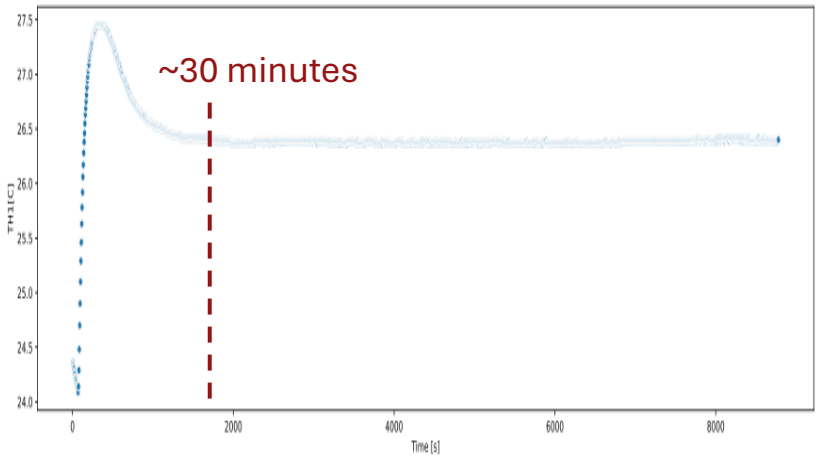
Measurements of ARCADIA

- New lab for silicon detector studies for future colliders
- Two stations for laser and beta-source studies:
  - Flexible setups for a variety of studies: oscilloscope or FPGA readout



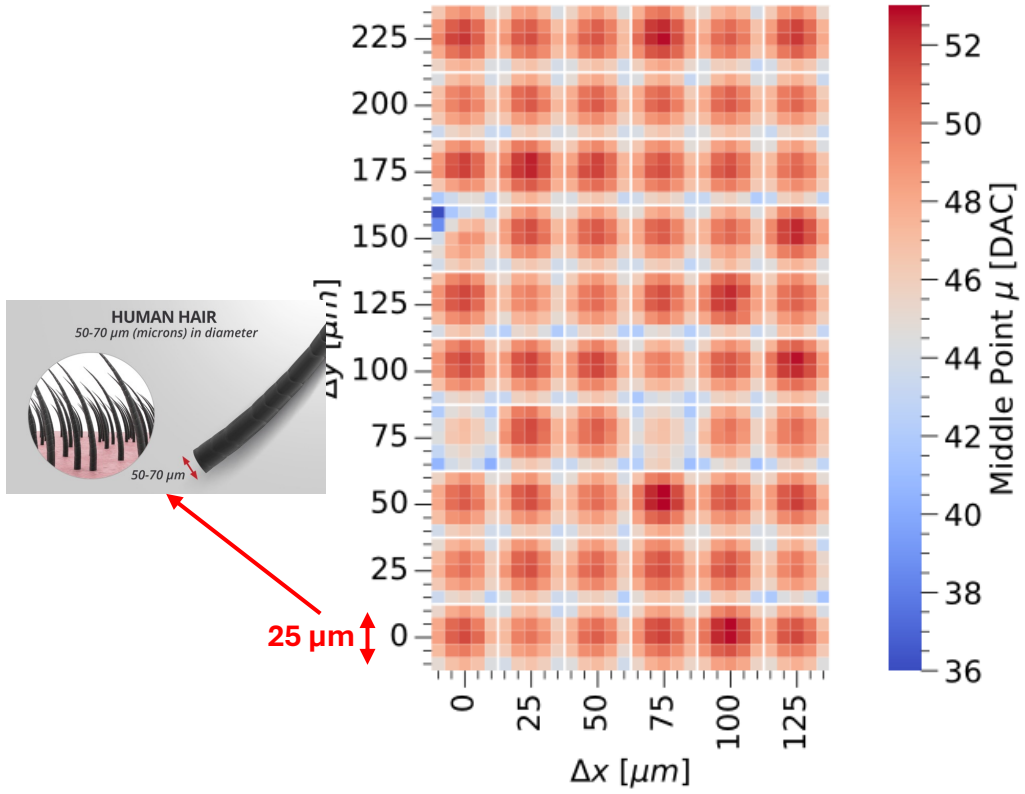
Measurements in the lab

- Laser calibration:
  - Tune the intensity to reproduce a MIP signal
    - Use beta-source and cosmic muons for calibration
  - Achieve beam-spot around 10 µm FWHM
    - Edge scanning and dedicated CCD camera
  - Calibrate the laser power to monitor for output power changes : fiber split for monitoring
- Automatized control of motion stages to perform µm scans
  - Calibrate stage movement to account for rotations when movin in 2D directions
  - Temperature control: measurements performed at room temperature



Measurements in the lab

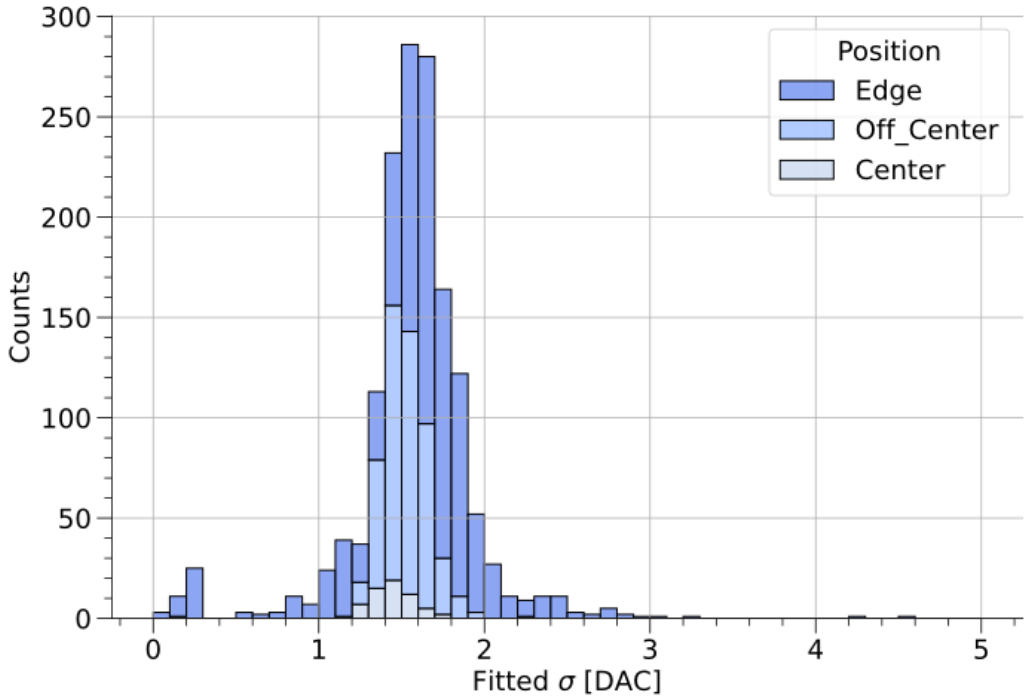
- An area of 6×10 pixels used to characterize cluster efficiency
  - Step size of 5μm is used across the scanning area
  - Total 25 scans per pixel.
  - Vary VCASN from 1 to 11, with steps of 2 to measure the efficiency.

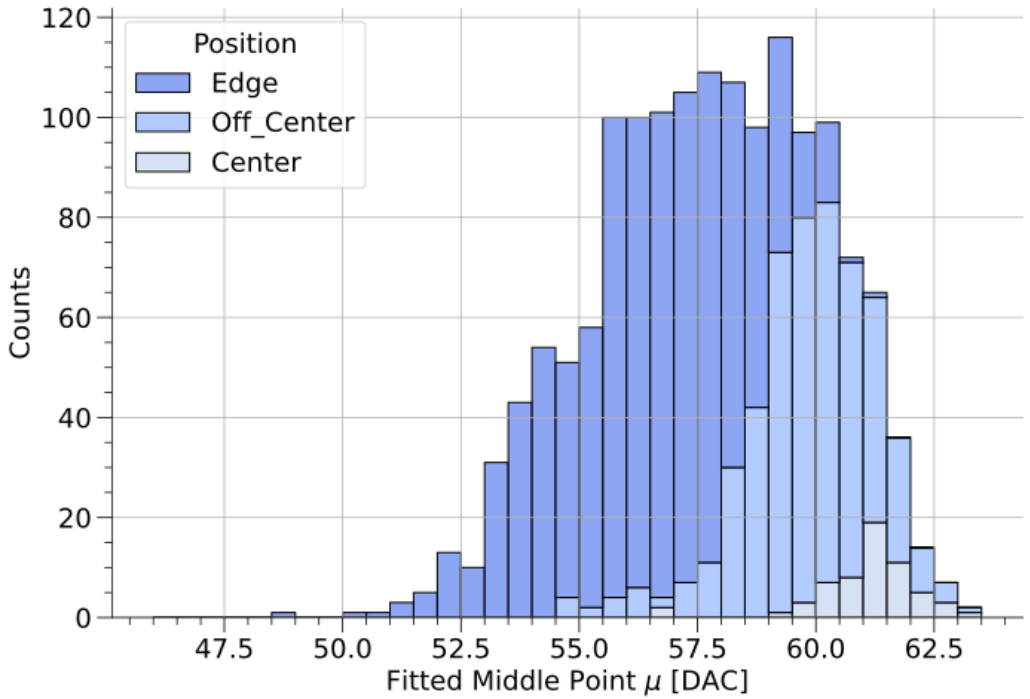


- Due to charge sharing, the value of μ is lower at pixel edges and higher at the center

Measurements in the lab

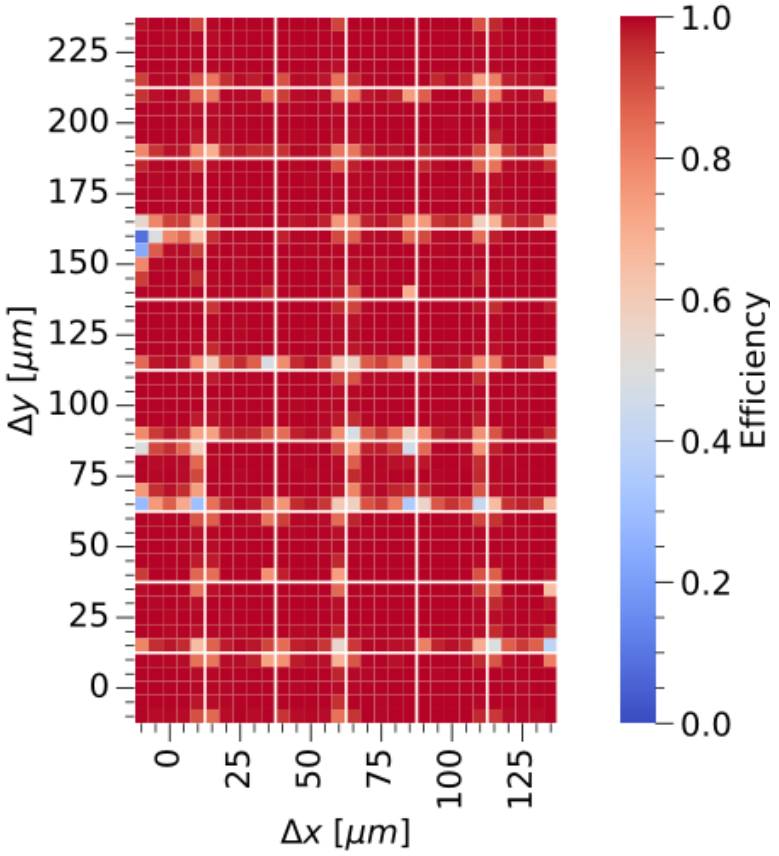
- Excellent readout performance and response to laser scans
  - Lower charge threshold, and higher noise further away from the pixel center.
  - This behavior is largely due due to charge sharing between pixels

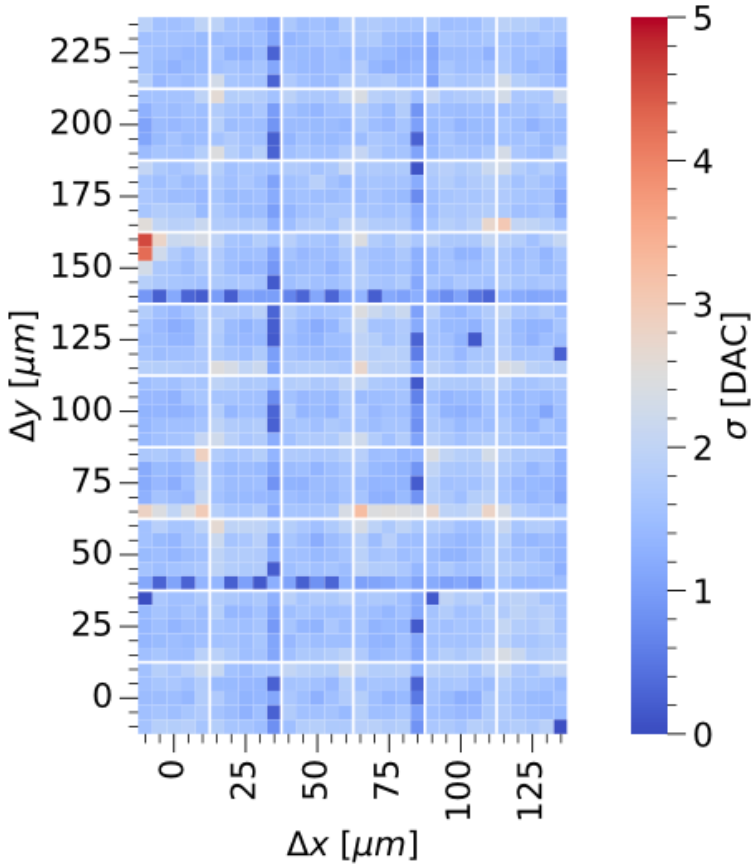




Measurements in the lab

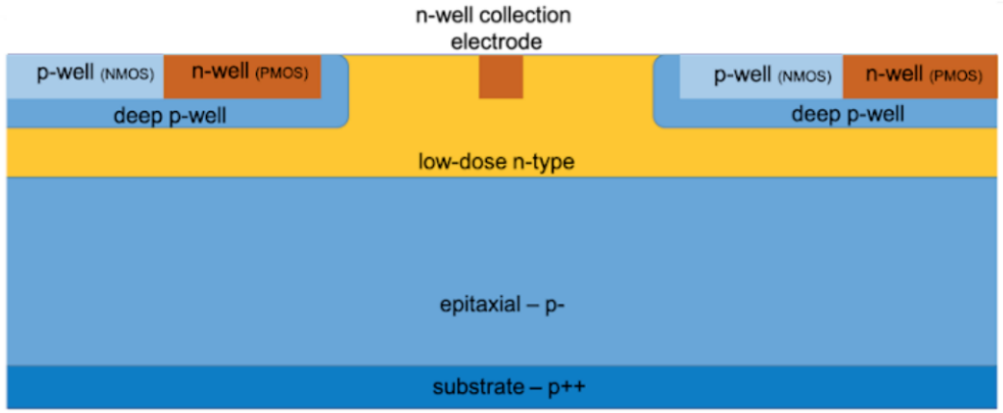
- Excellent uniformity of detection efficiency across the pixel area
- Noise is mostly uniform across detector surface



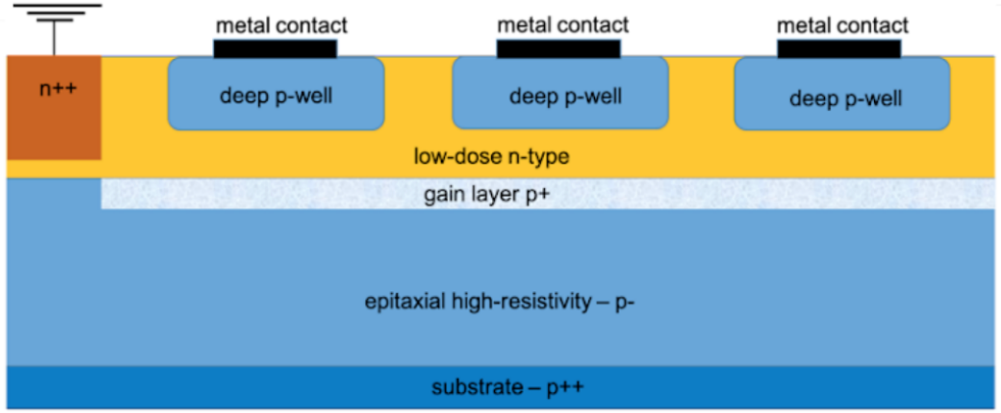


Developments with SkyWater

- Develop MAPS sensors in a commercial process that will provide fast timing (10 ps) and precise spatial resolution (5 μm)
  - Target application vertex detectors for future e^+e^- Higgs factories
- Electronics for signal processing are placed in dedicated p– and n-wells contained within a deep p-type well
  - Intrinsic gain will allow MAPS detectors to perform precise time measurements in addition to spatial measurements



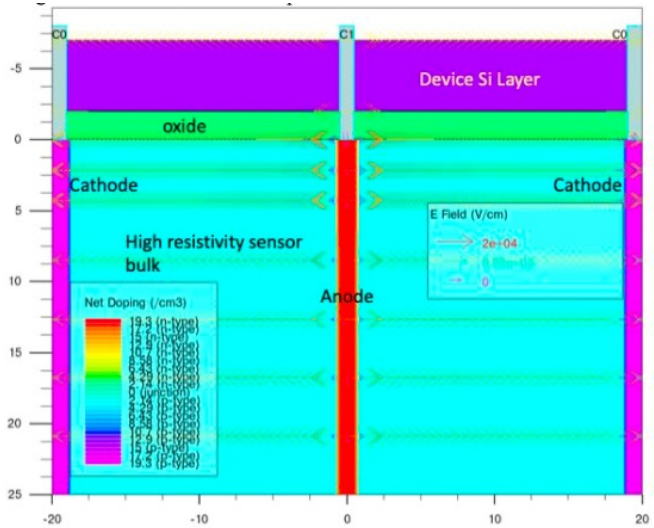
CMOS sensor



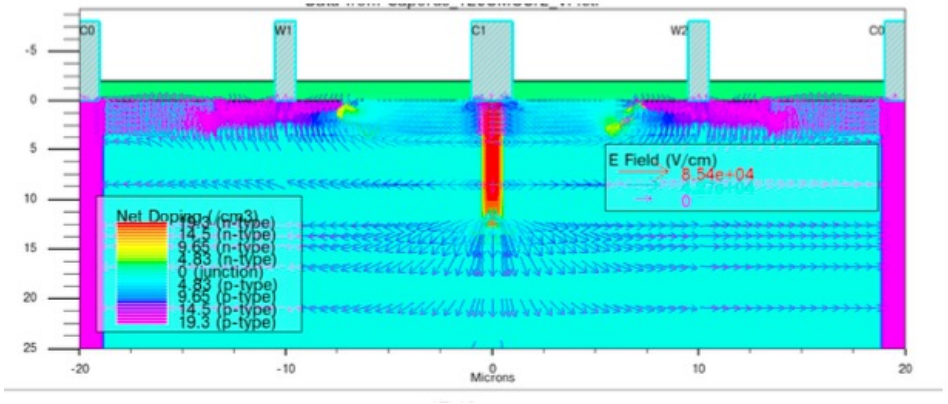
Monolithic AC-LGAD

Developments with SkyWater

- Exploring options: factorize charge generation, large signal to the front-end electronics
  - Integrate with directly coupled CMOS electronics in an SOI stack
- Deep trench electrode: low capacitance and good charge collection by drift
  - Simulation shows that the central anode provides efficient charge collection
- Collaboration with *Caporus technology* to investigate feasibility



"sketch" of a 3D sensor incorporated into an SOI stack with the CMOS in the top SOI layer



Electric field for a sensor with charge collected in a central anode. Electrodes W1 and W2 are connected to deep p well structures which contains the CMOS electronics

Summary

- Several ongoing projects at Fermilab with applications towards FCC-ee vertex detector
  - All projects are making steady progress
  - Developments with SkyWater are progressing
  - Signed an NDA with LFoundry to join the developments with ARCADIA

- Lots of developments in infrastructure and expertise in the recent years, benefiting from synergies with HL-LHC, HEP and NP