

Status and plans of the ARCADIA project and LFoundry 110 nm

Manuel Rolo (INFN)



Istituto Nazionale di Fisica Nucleare

FCC-ee vertex detector R&D workshop
Pisa, 30th October 2025

ARCADIA FD-MAPS CMOS Sensors



Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

INFN CSN5 Open Call for the development and production of high-efficiency deep-submicron monolithic CMOS sensors on a 110nm CIS technology

- Collaborative research between INFN and LFoundry (chip manufacturing fab in Avezzano)
- R&D in semiconductor sensor technology, IP-core design and ASICs, advanced DAQs
- Application to high-energy particle and astroparticle physics, and medical applications
- Development of very low-power architectures for frontier silicon tracker detectors with power densities below 10 mW/cm²
- Innovative monolithic CMOS sensors with gain layer (CMOS LGAD) for frontier photon and charged particle detectors with time-of-flight capabilities
- Enabling technology for the production of very thick (up to 700µm) fully-depleted CMOS sensors with excellent charge collection efficiency for gamma and X-ray imaging
- Follow-up funding (2 M€ dedicated to FD-MAPS design and production, 50% for silicon runs) from ASI “SpaceltUp!”, ERC AdG “Si3” and EIC Pathfinder Open “1MICRON” with SPW runs planned through 2026-2028



European Research Council
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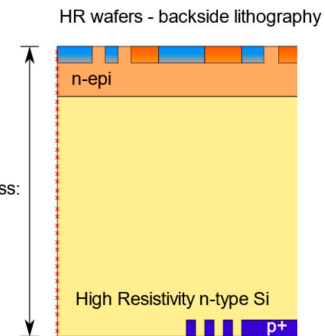
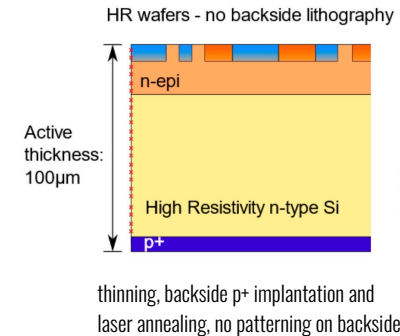
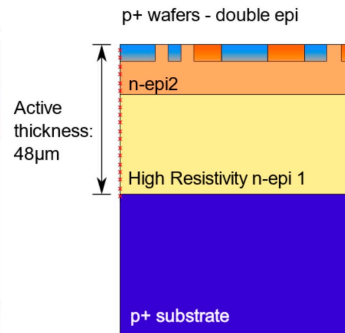
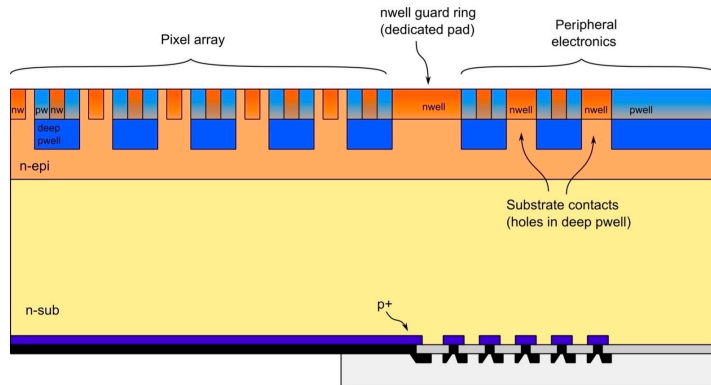
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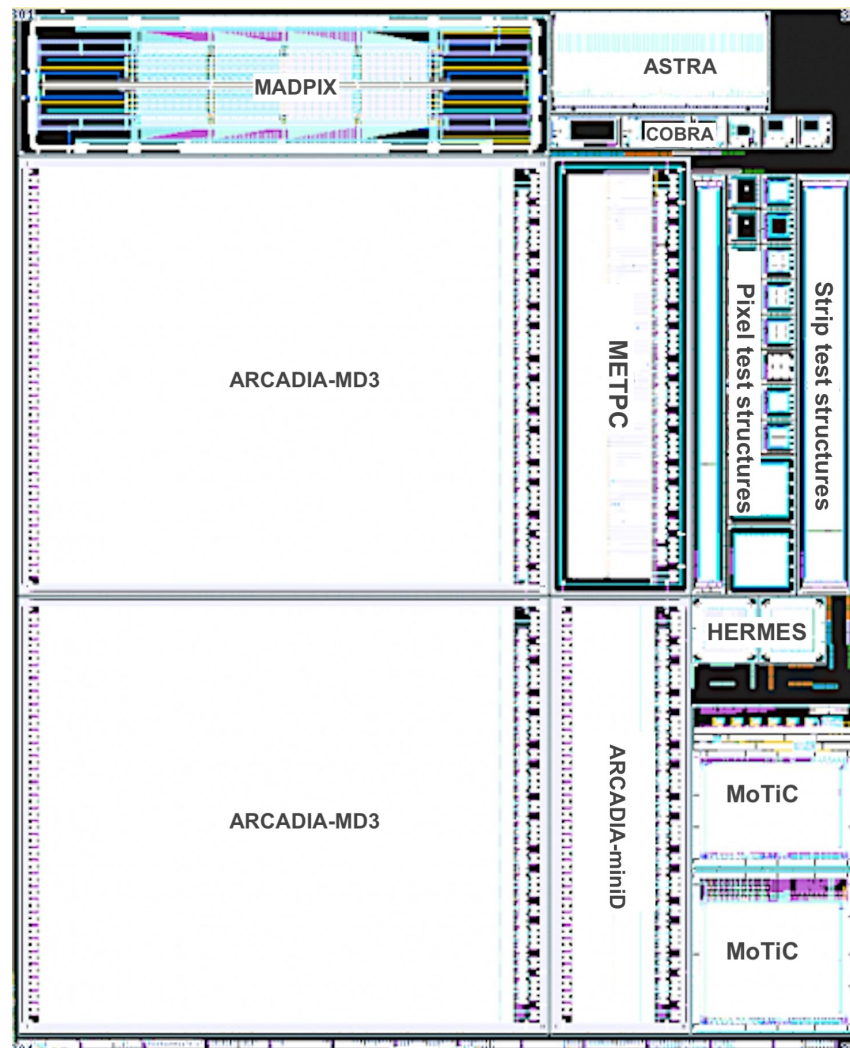
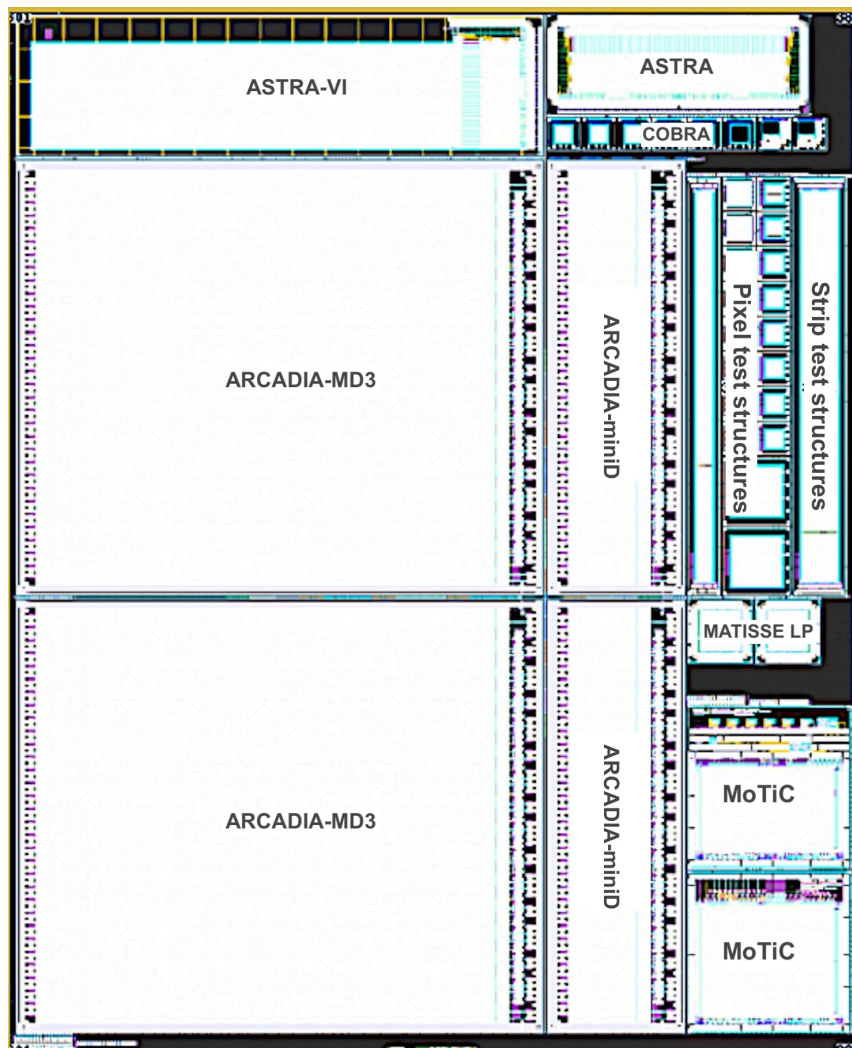


ARCADIA CMOS Sensor Technology



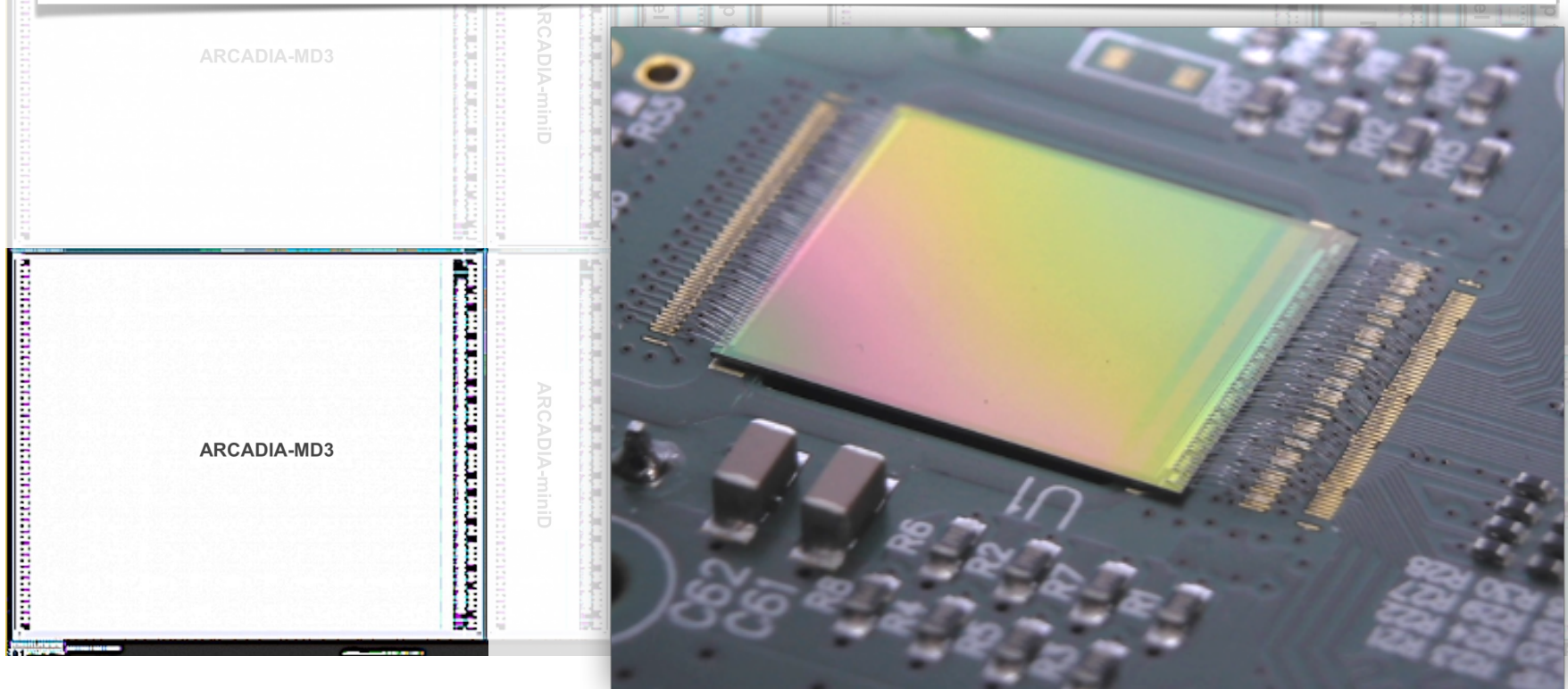
- ◆ **n-type high-resistivity** ($> 2\text{k}\Omega \cdot \text{cm}$) starting substrate, wafers with a typical final thickness ranging from 100 to 500 μm
- ◆ **n-type epitaxial layer** with increased doping concentration to control the potential beneath the deep p-well: moves the punch-through between the backside p+ electrode and the top p-type regions toward higher voltage values (improves process window)
- ◆ top side of the wafer processed with LFoundry's CMOS 110 nm node technology featuring **six metal layers** and 1.2 V NMOS/PMOS devices isolated with a deep p-well
- ◆ back of the wafer features a p-n junction realised with a p+ implantation and annealing
- ◆ **post-processing backside lithography** allows the creation of a multiple floating guard-ring termination structure around the sensor active area, avoiding early edge breakdown at the borders of the p+/n+ substrate junction - necessary for thicker sensors
- ◆ **thinner sensors** can avoid the BSI or use a **p+ starting substrate with the double epitaxial layer grown on top**

ARCADIA Technology demonstrators

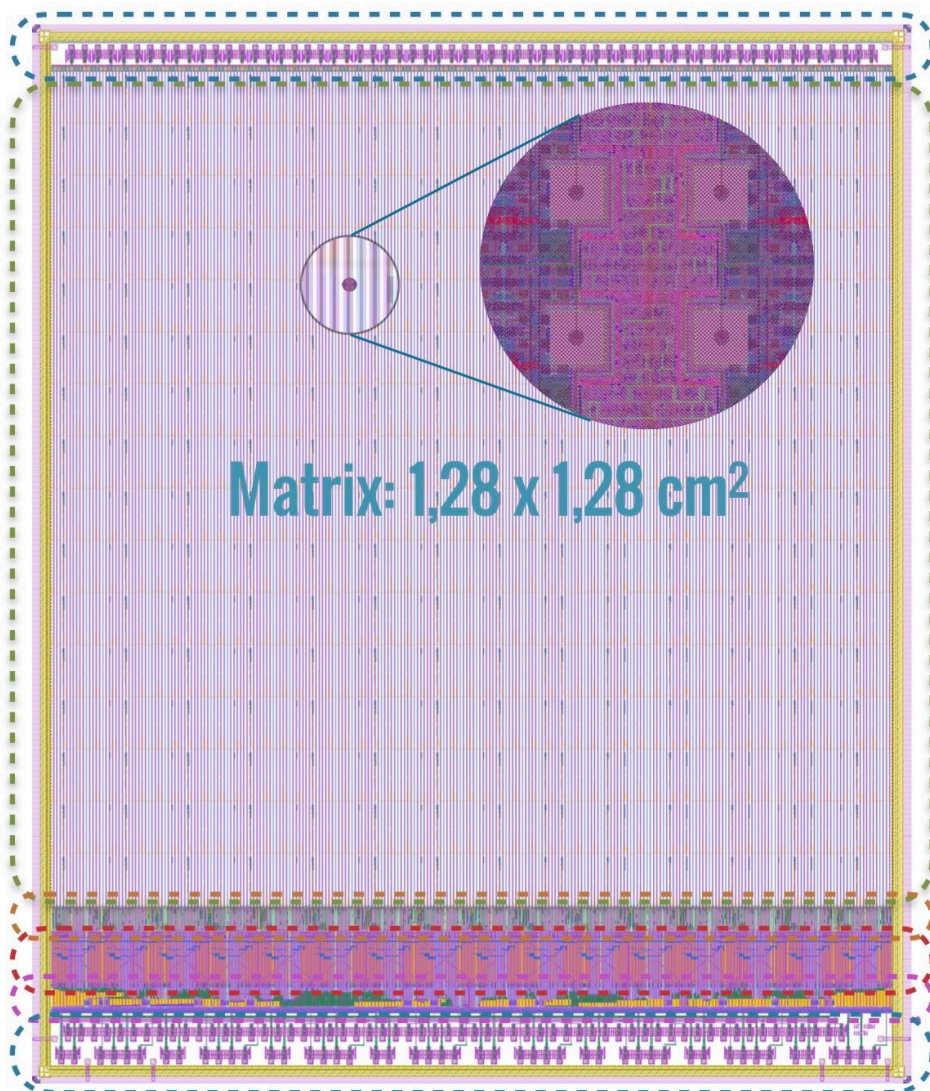


ARCADIA MD3 FD-MAPS Main Demonstrator

- ▶ system-ready fully depleted monolithic active pixel sensor demonstrator chip
- ▶ active area of 1.64 cm^2 on a matrix with 512×512 pixels featuring a *pitch of $25 \mu\text{m}$*
- ▶ data-driven binary readout allowing for a rate capability of 100 MHz/cm^2
- ▶ total power density of 17 mW/cm^2 (supporting event rates of $20\text{-}30 \text{ MHz/cm}^2$); for low-rate operation, power density below 10 mW/cm^2



ARCADIA MD3 FD-MAPS Chip Floorplan



Top Padframe

Auxiliary supply, IR Drop Measure

Matrix

512x512 pixels, Double Column arrangement

End of Sector (x16)

Reads and Configures 512x32 pixels

Sector Biasing (x16)

Generates I/V biases for 512x32 pixels

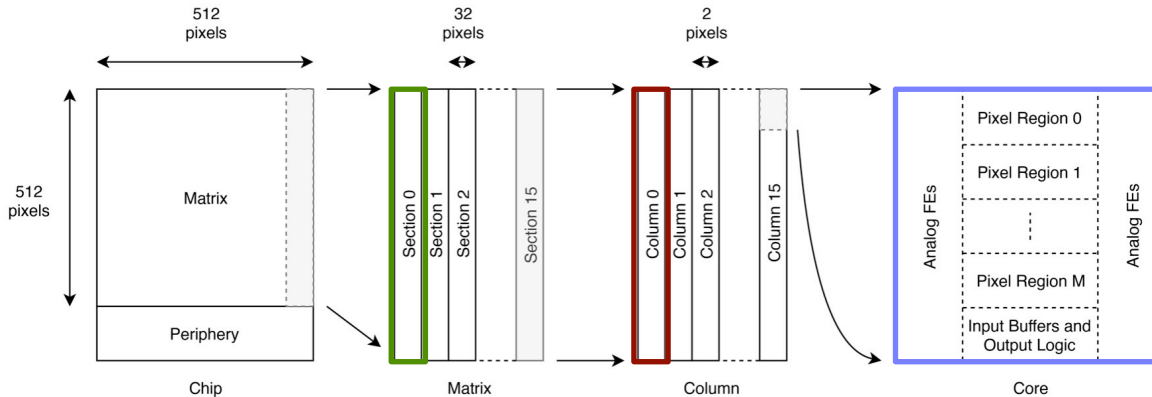
Periphery

SPI, Configuration, 8b10b enc, Serializers

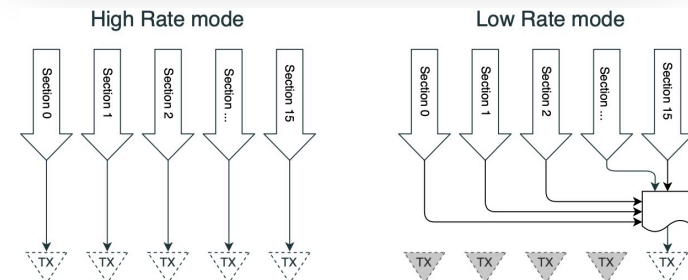
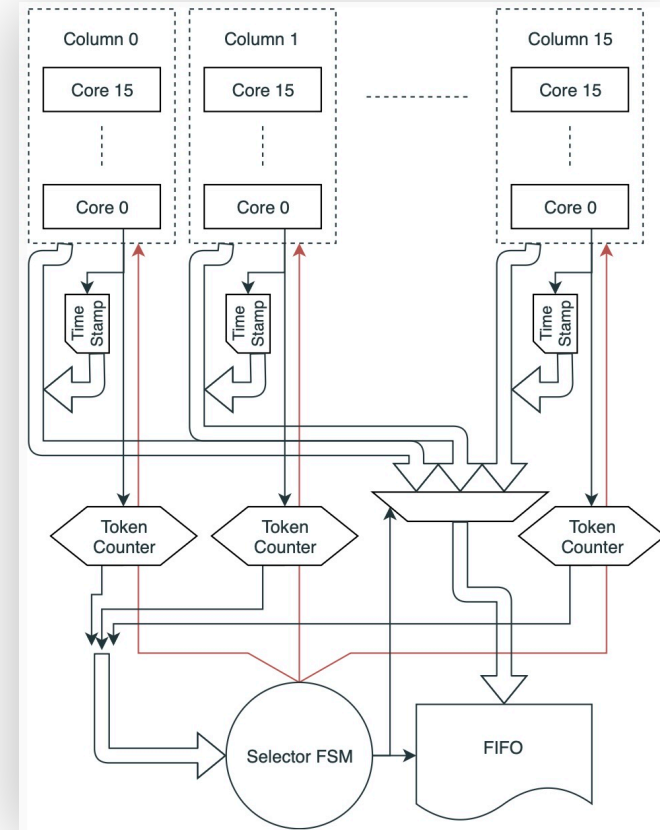
Bottom Padframe

Stacked Power and Signal pads

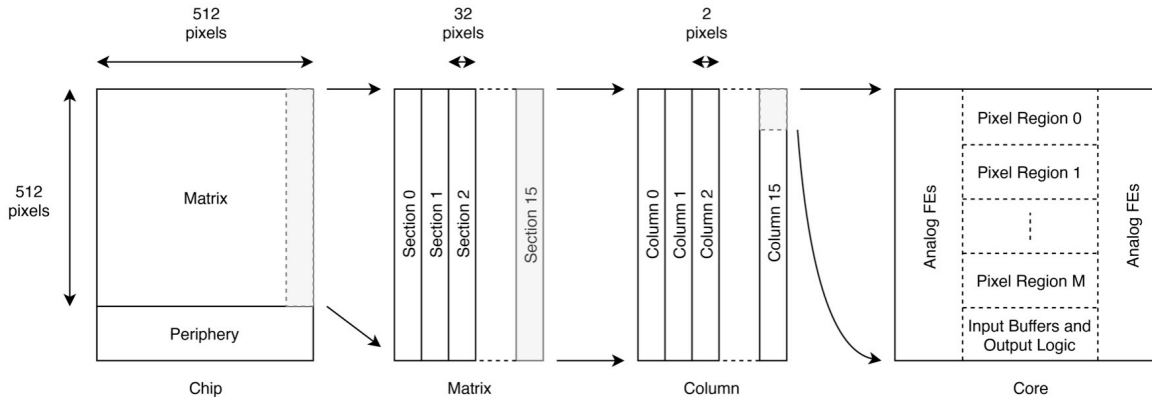
ARCADIA MD3 data readout



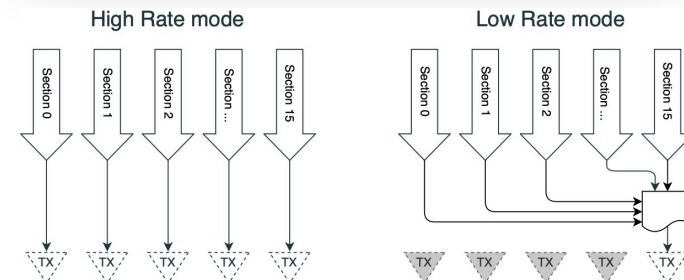
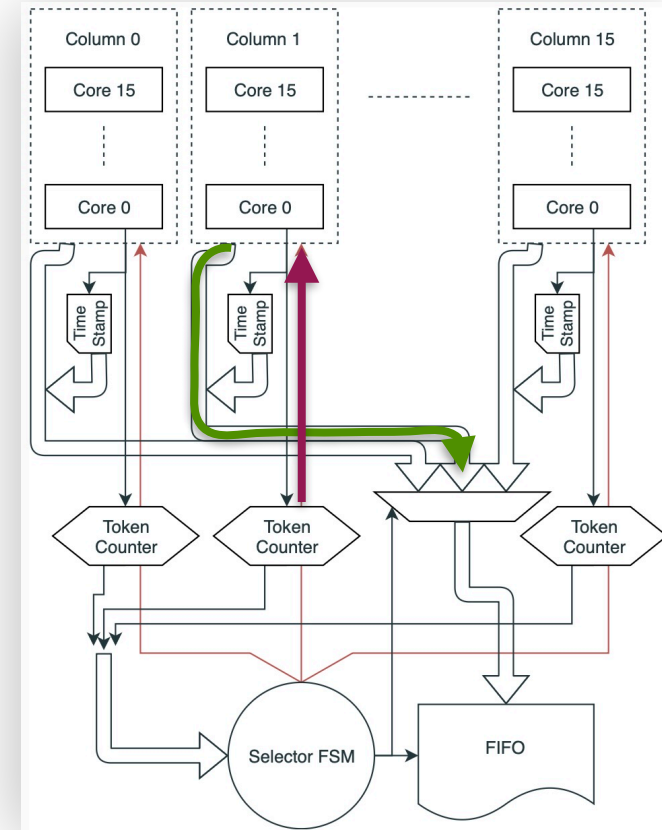
- The ARCADIA-MD3 active sensor matrix (512 x 512) is partitioned into **Sections** (32 x 512), each being composed of 16 **Core Columns** (2 x 512)
- The minimum synthesisable unit in the Matrix are the 16 **Cores** (2 x 32)
- priority-encoding based data readout, with the hitmap region (hardcoded during synthesis) and core (generated during readout) addresses being propagated to the section readout unit whenever the pixel receives the writing token
- The payload consisting of the Column data, Column address, and Timestamp is then sent to the output FIFO and will be (in High Rate Mode) independently read out and have a dedicated serialiser and c-LVDS data link.
- In Low Rate Mode, all data produced by the matrix is buffered from all the Section Readout Units into a central FIFO and conveyed into one data transceiver, all other being switched off (finite-state machines, encoders, serialisers and c-LVDS Tx links).



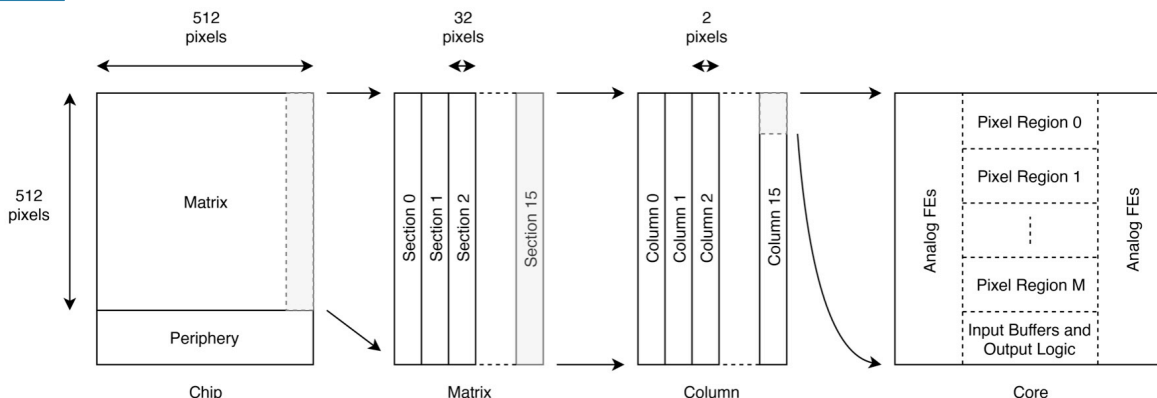
ARCADIA MD3 data readout



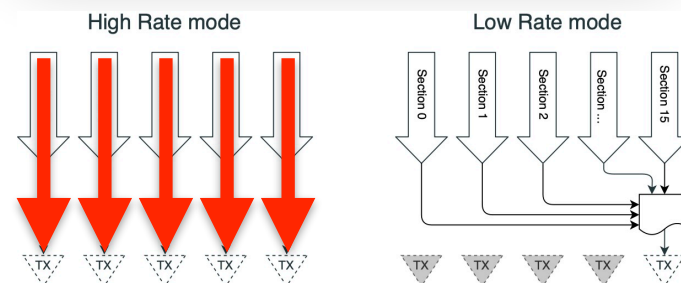
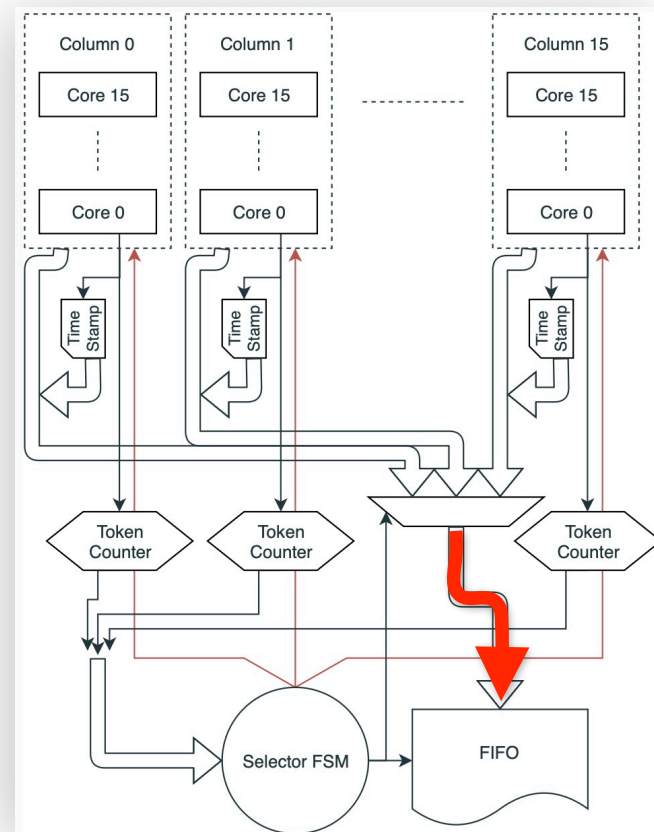
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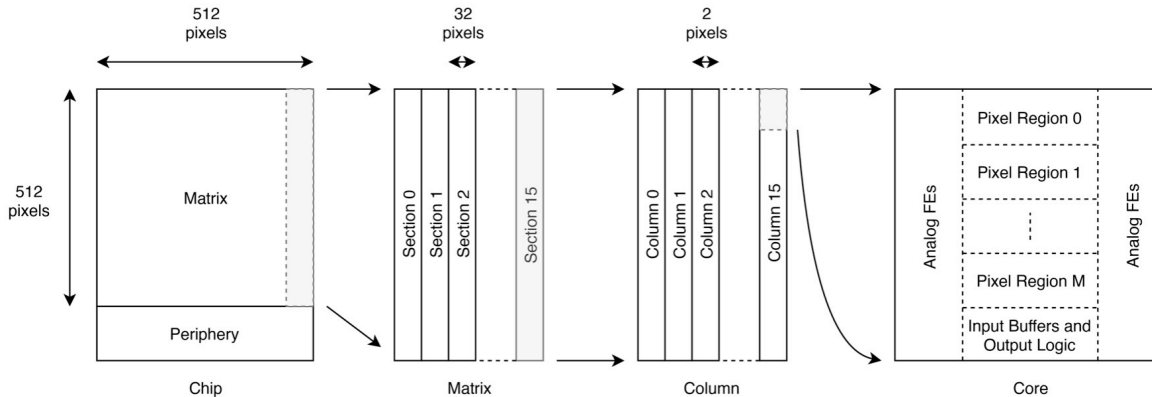
ARCADIA MD3 data readout



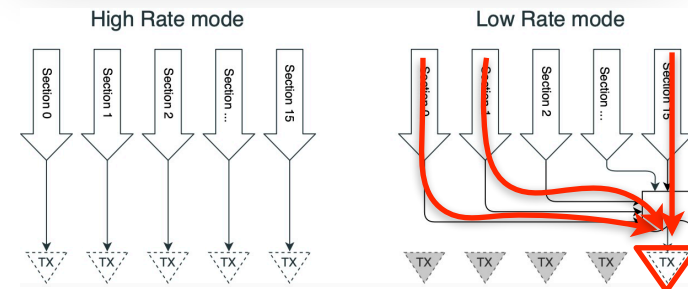
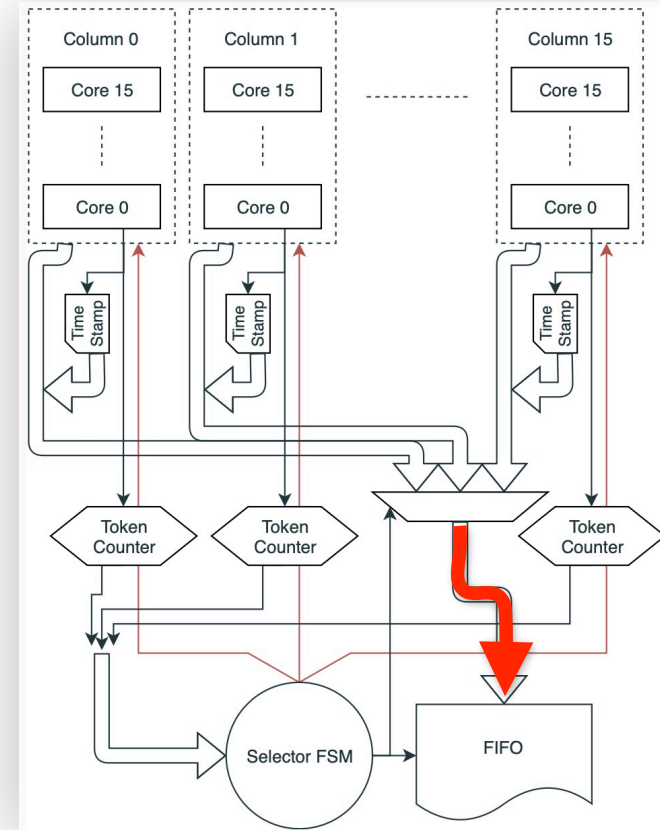
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ARCADIA MD3 data readout



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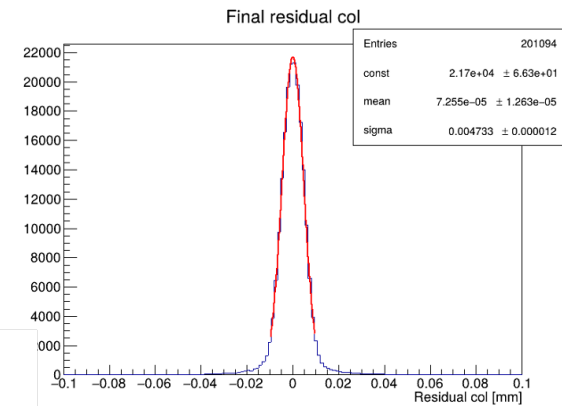


ARCADIA MD3 test-beam with 120 GeV protons

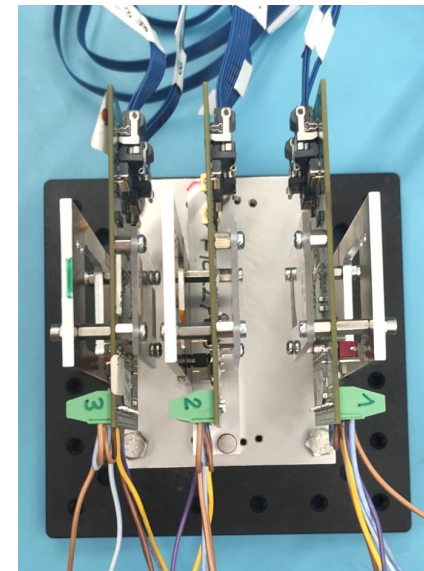
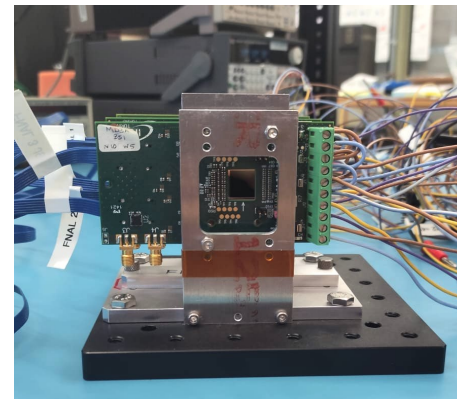
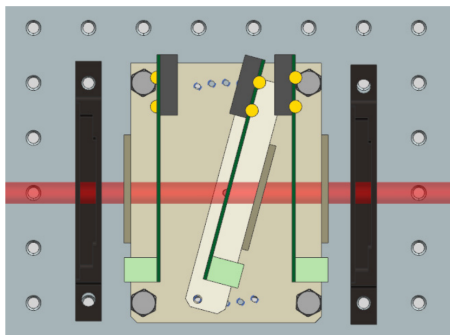
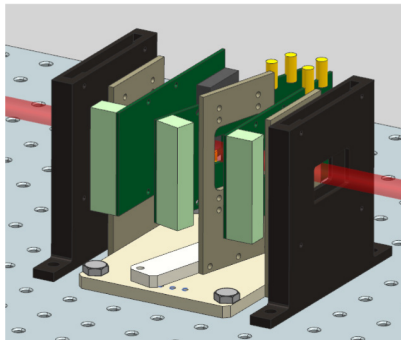
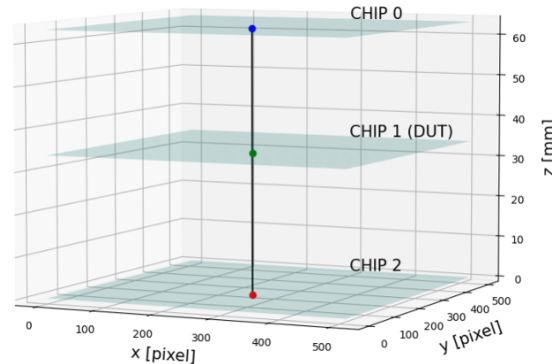
- Test beam at FNAL (120 GeV protons)
- mini-telescope with 3 ARCADIA-MD3 200 μm thick sensors
- Threshold, sensor HV and incidence angle parametrisation
- study of cluster size, collection efficiency, spatial resolution
- Data analysis and paper in preparation

(Later on) **Sabrina Ciarlantini**

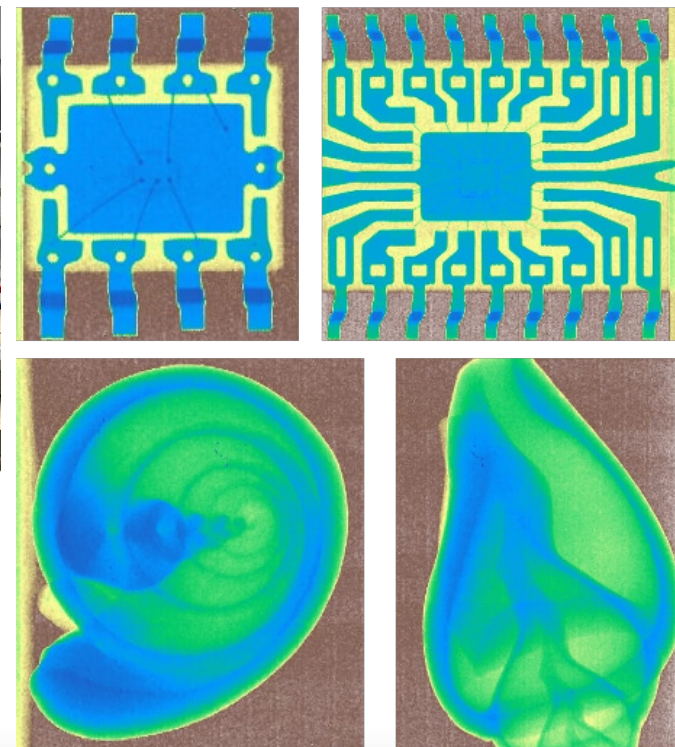
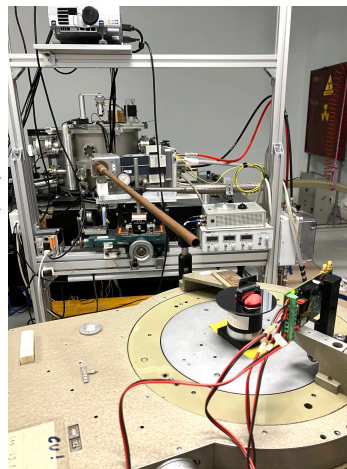
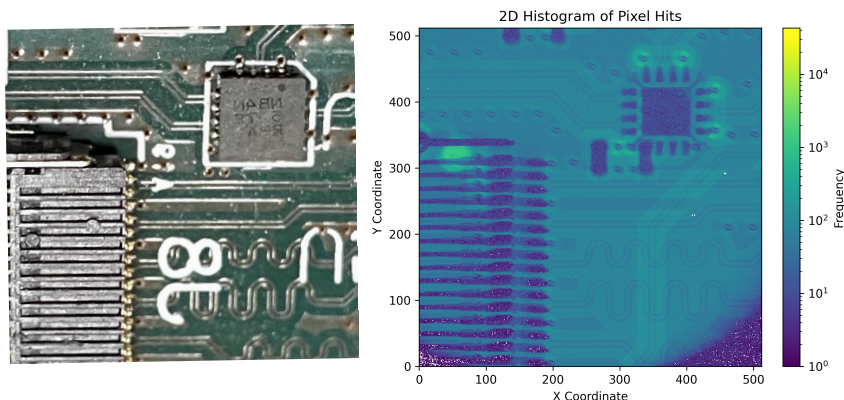
*The ARCADIA Fully Depleted MAPS:
laboratory characterization and particle
tracking performance*



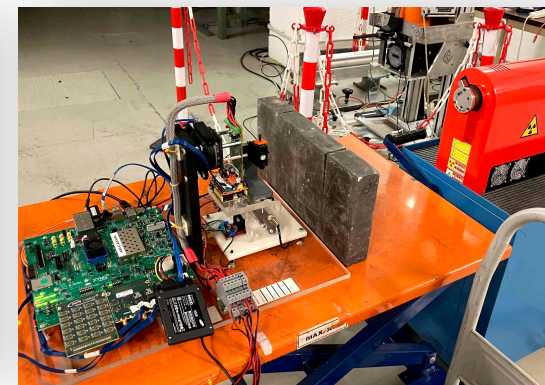
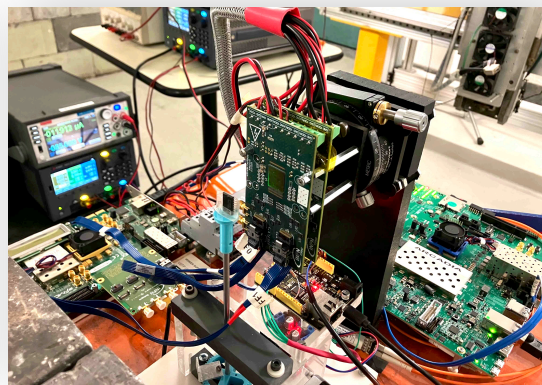
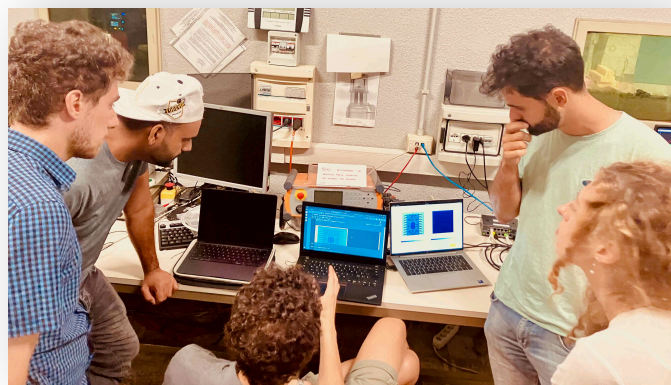
Single-point resolution $\sim 4.7 \mu\text{m}$



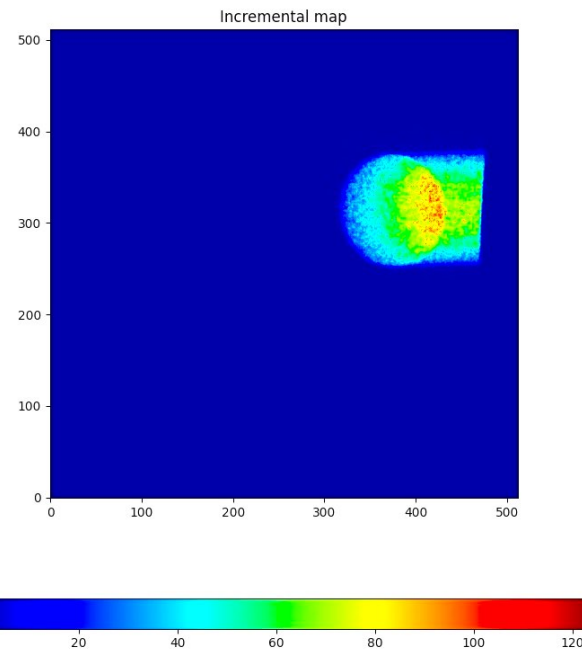
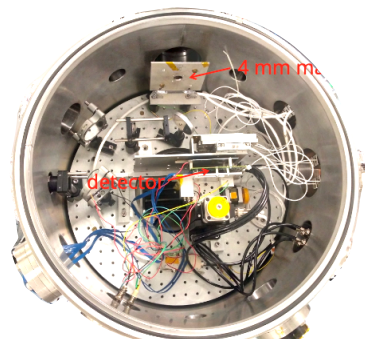
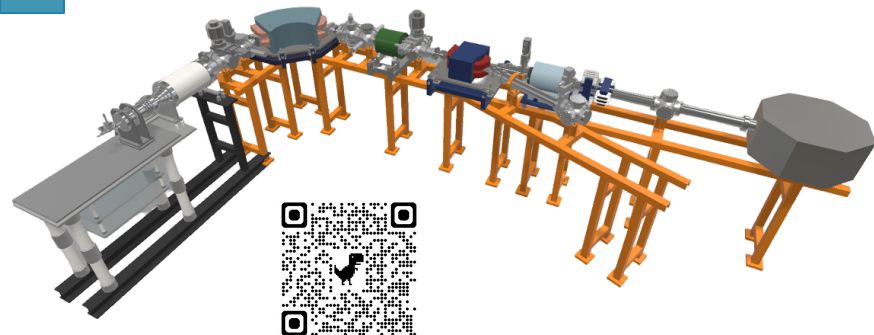
ARCADIA MD3 characterisation with X-rays



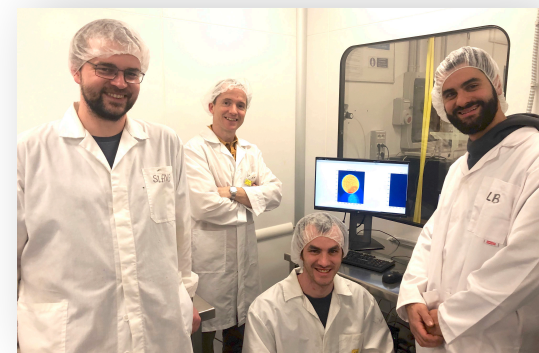
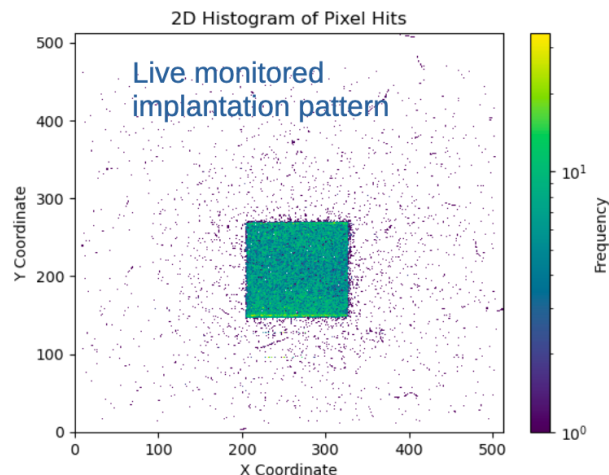
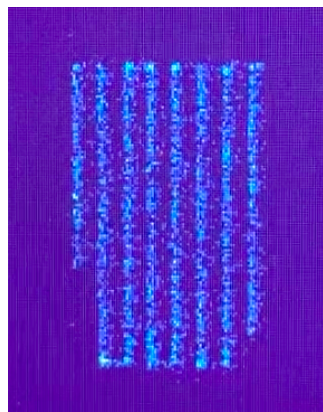
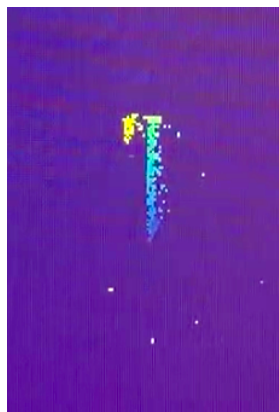
- ◆ Molybdenum $K\alpha_1$ and $K\alpha_2$ X-rays (17 keV)
- ◆ X-ray microfocus (up to 140 keV) for radiography and CT setups
- ◆ Threshold calibration, charge collection, cluster analysis
- ◆ Test-beam at the DESY PETRA synchrotron scheduled 12/2025



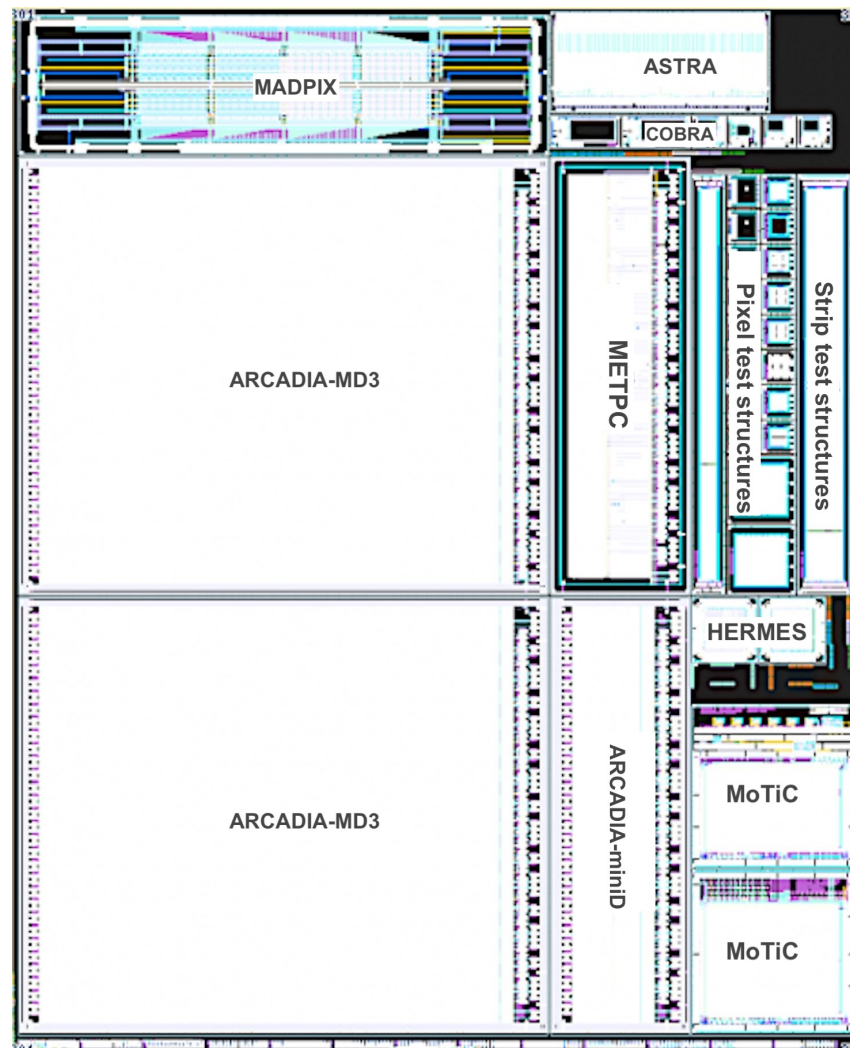
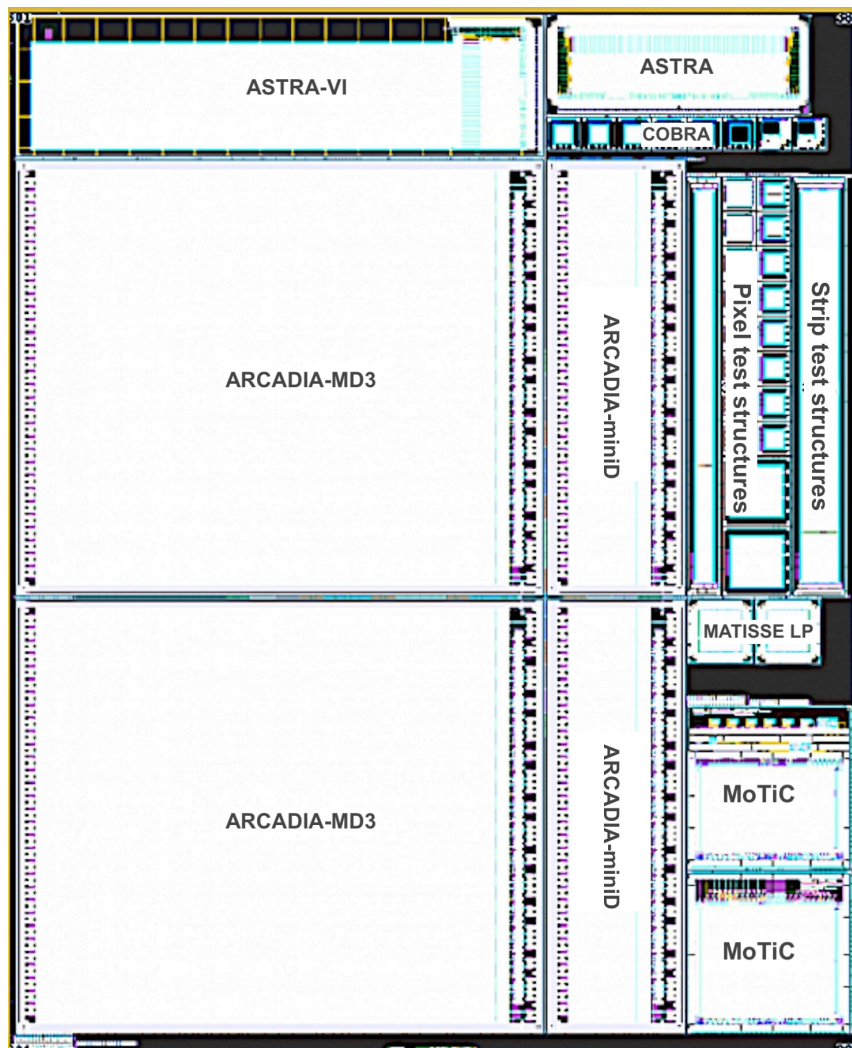
ARCADIA MD3: imaging low-energy ions



- LIUTo Laboratory for Ion implantation at the University of Torino
- Online Beam imaging with ARCADIA MD3: precise reconstruction of beam current and spectrum in real time
- Detection of single ions (H-, C-, O-), down to 17 keV (H-)
- Provides insights into defects, carrier transport and detector performance



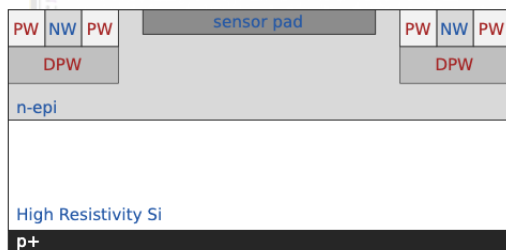
ARCADIA Technology demonstrators



ARCADIA MADPix CMOS-LGAD Demonstrator

- *p-type gain implant beneath the n+ collecting electrode to push the timing performance*
- *time resolution on thin substrates, estimated with Monte Carlo studies based on experimentally-tuned simulations, **expected better than 20 ps r.m.s.***

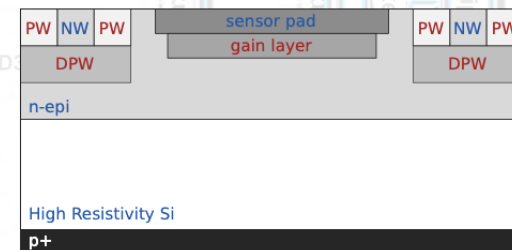
development of fully-depleted MAPS



Standard 110 nm CMOS process at LFoundry



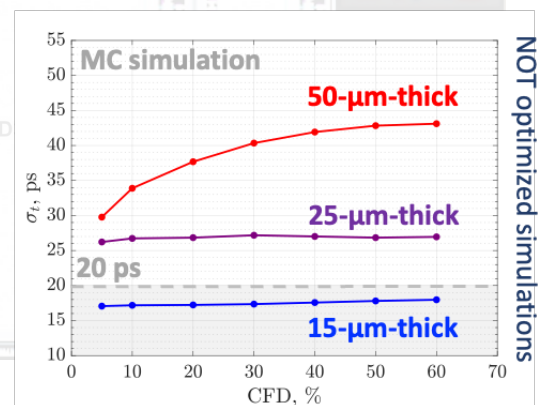
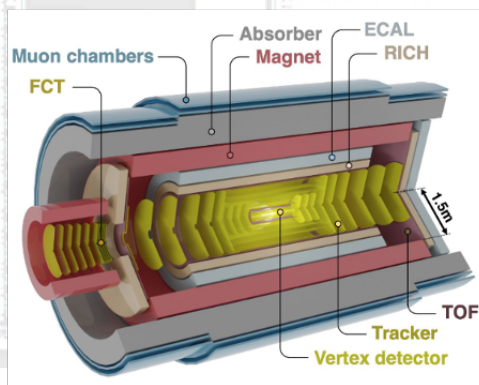
CMOS-LGAD



Add-on *p*-gain implant (gain target: 10 – 30)

ALICE3 TOF detector:

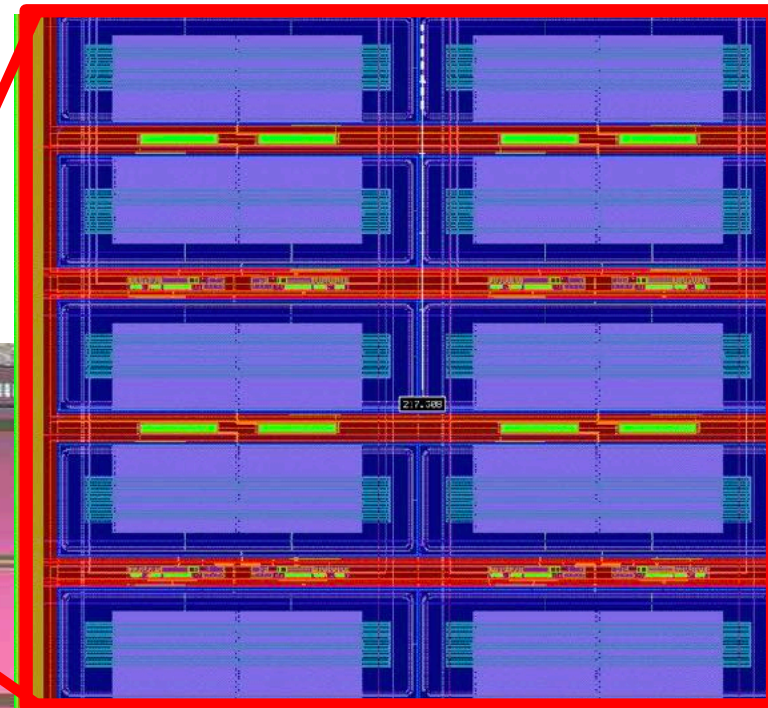
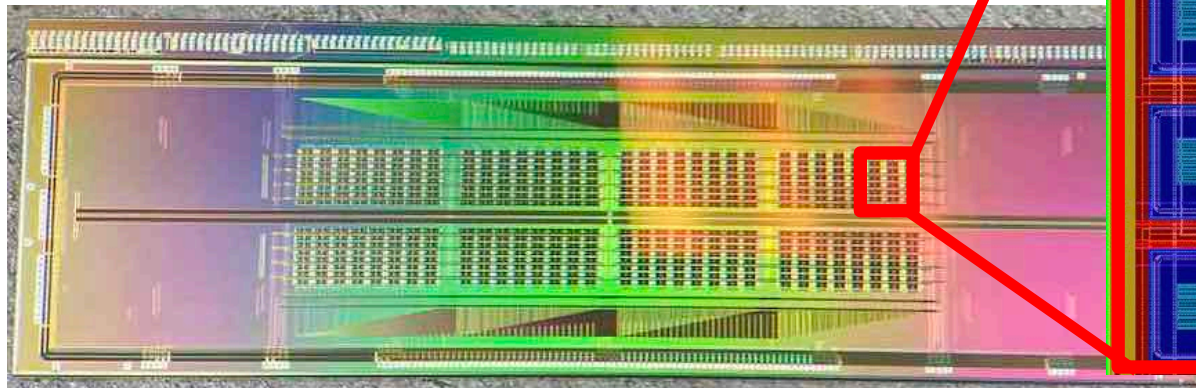
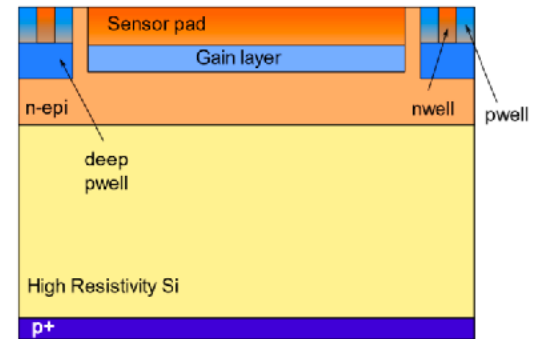
- high-resolution tracking
- particle ID with low $p_T \Rightarrow \sigma_t \sim 20$ ps



NOT optimized simulations

ARCADIA MADPix CMOS-LGAD Demonstrator

- ◆ **MadPix** prototype with gain layer and integrated electronics
- ◆ first small-scale demonstrator 4 x 16 mm²;
- ◆ 8 matrices (64 pixel pads each) implementing different sensor and front-end flavours;
- ◆ 250 x 100 μm² pixel pads;
- ◆ 64 analogue outputs on each side, rolling shutter of single matrix readout;

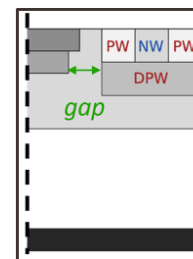
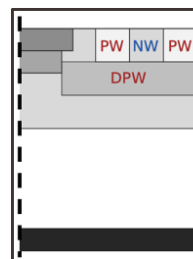
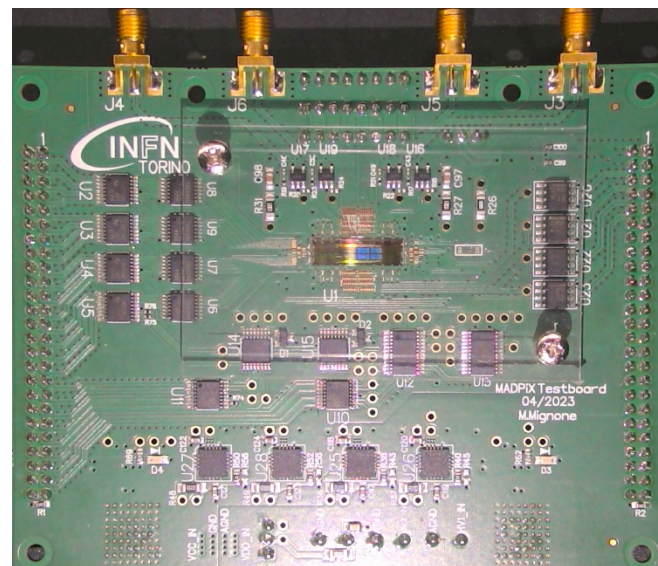


ARCADIA MADPiX CMOS-LGAD Test Beam

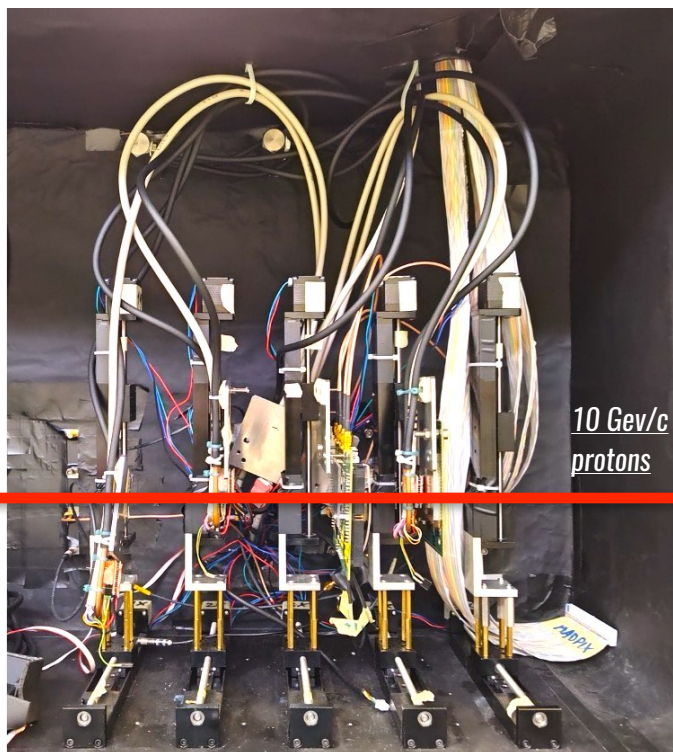
ALICE3 TOF Test beam @ CERN PS - October 2024

Trigger:
LGAD 1x1 mm 50 μ m
reference (28 ps r.m.s.)

MadPiX

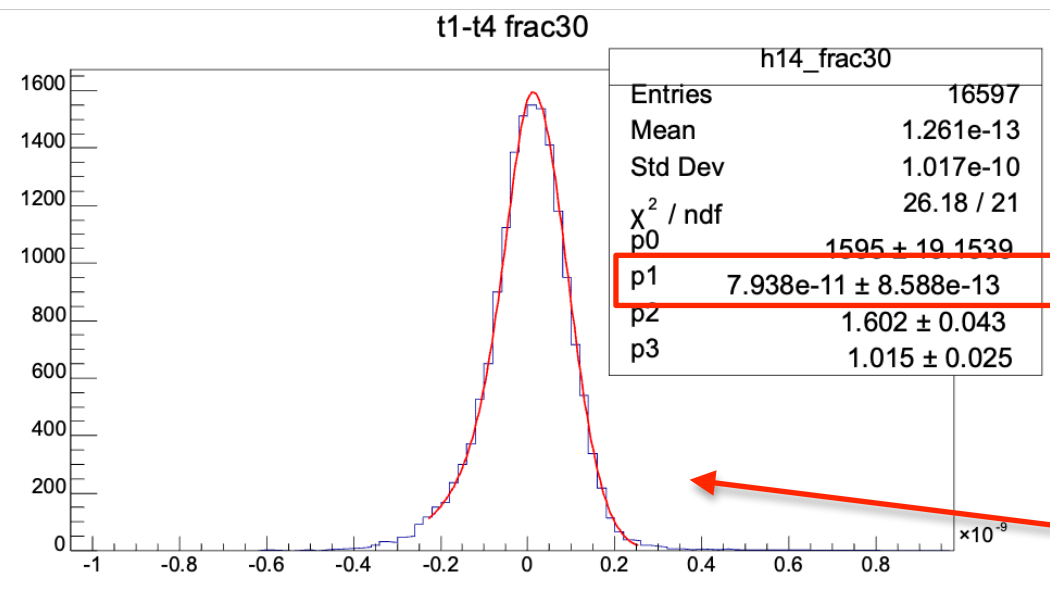


- 3 Test boards
- 2 Flavours
 - A1 and A2
- 4 Pixels
 - J3, J4, J5, J6

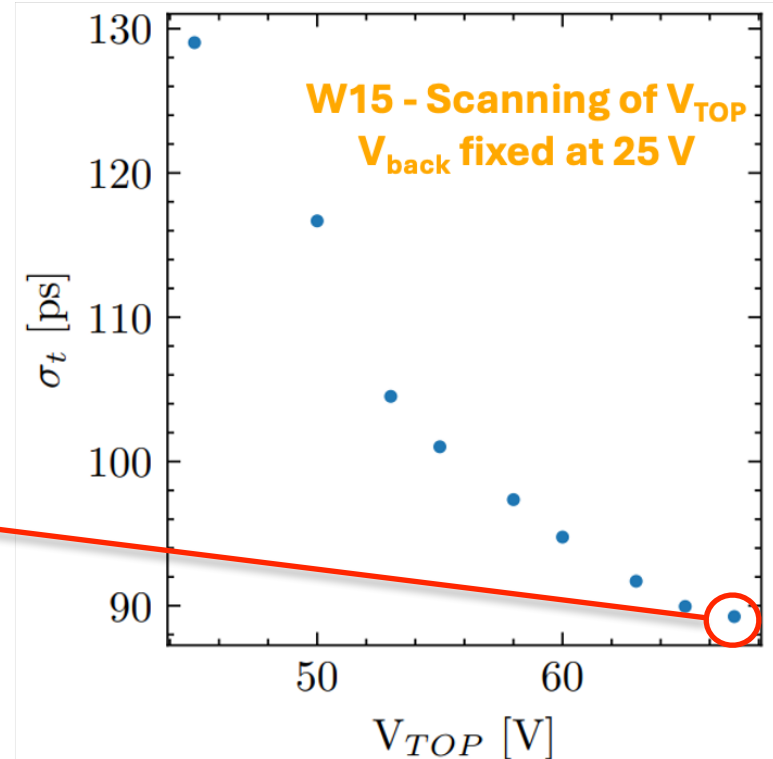


U. Follo et al 2024 JINST 19 P07033 "First results on monolithic CMOS detector with internal gain"

ARCADIA MADPix CMOS-LGAD Test Beam



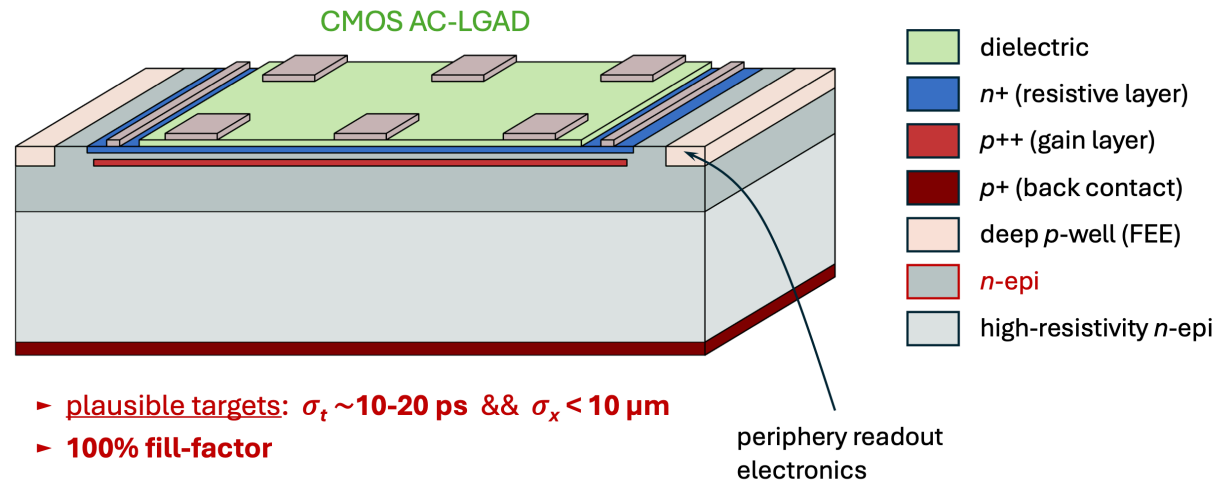
Measured timing resolution (sensor) ~ 72 ps r.m.s.



- ◆ Gain layer implemented (5-15) with very good matching with TCAD simulation framework
- ◆ MadPix test beam just concluded, timing resolution measured < 75 ps (very preliminary results)
- ◆ 48 μm thick active layer on a p+ substrate, timing resolution is sensor limited (FEE jitter ~ 20 ps r.m.s.)
- ◆ Ongoing: new short-loop with ARCADIA mask set and thinner n-epi active layer, start IP design for ALICE3 TOF

R&D for a Si-Wrapper with CMOS AC-LGADs

*Mandurrino, M. et al., Numerical Proof-of-Concept of Monolithic AC-LGAD Detectors for 4D Particle Tracking. Sensors 2025, 25, 4185.
<https://doi.org/10.3390/s25134185>*



- LGAD detector with continuous gain layer (RSD), charge collection through resistive n -layer and readout by induction on AC coupled pads, for a
- ➡ fully active detector, avoiding isolation implants (used to prevent early breakdown) in segmented LGADs
- Timing resolution approximatively independent from pixel pitch
- CMOS integration of the LGAD technology already demonstrated (in LF11is) with the ARCADIA masksets
- Up next for CMOS AC-LGAD: demonstrate the compatibility between the RSD readout scheme and the LF11is ARCADIA CMOS process flow, first prototypes in future silicon production runs.

Setting the stage for the FCC-ee vertex and tracker FD-MAPS detector collaborative design

- INFN and LFoundry agree on the terms to allow for the participation of third-party design groups to joint LF11IS ARCADIA sensor technology development and production runs, enabling straightforward and low-risk ramp-up of the R&D on FDMAPS using the LF11IS platform for new design teams.
- Possibility to explore **multiple wafer splits**: n-epi thickness, n-type or p-type starting substrate, substrate resistivity, FSI or BSI process on different wafer thicknesses, use of a gain layer for the implementation of monolithic CMOS LGADs.
- **Silicon-proven IP** and Synopsys **integration flows** available.
- Several engineering runs (full-reticle sets and multi-layer mask set) funded at INFN through 2026-2028.
- More details at the 2025 DRD7 annual workshop (<https://indico.cern.ch/event/1556239/overview>).

Thank you for your time!

ARCADIA
XXXXXXXXXX



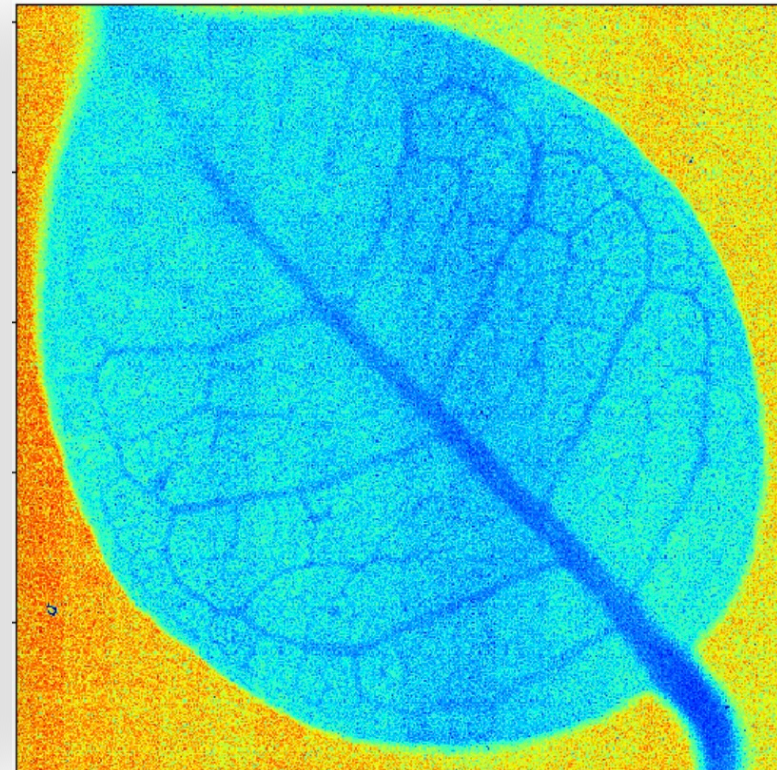
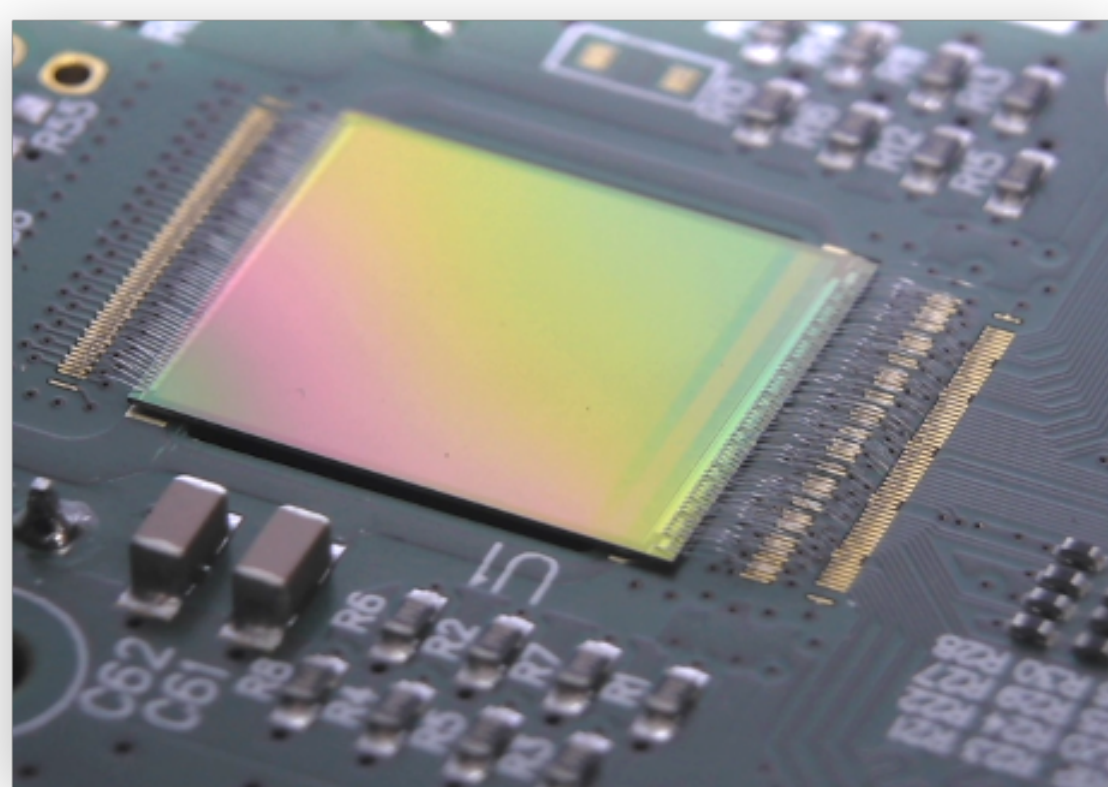
Istituto Nazionale di Fisica Nucleare



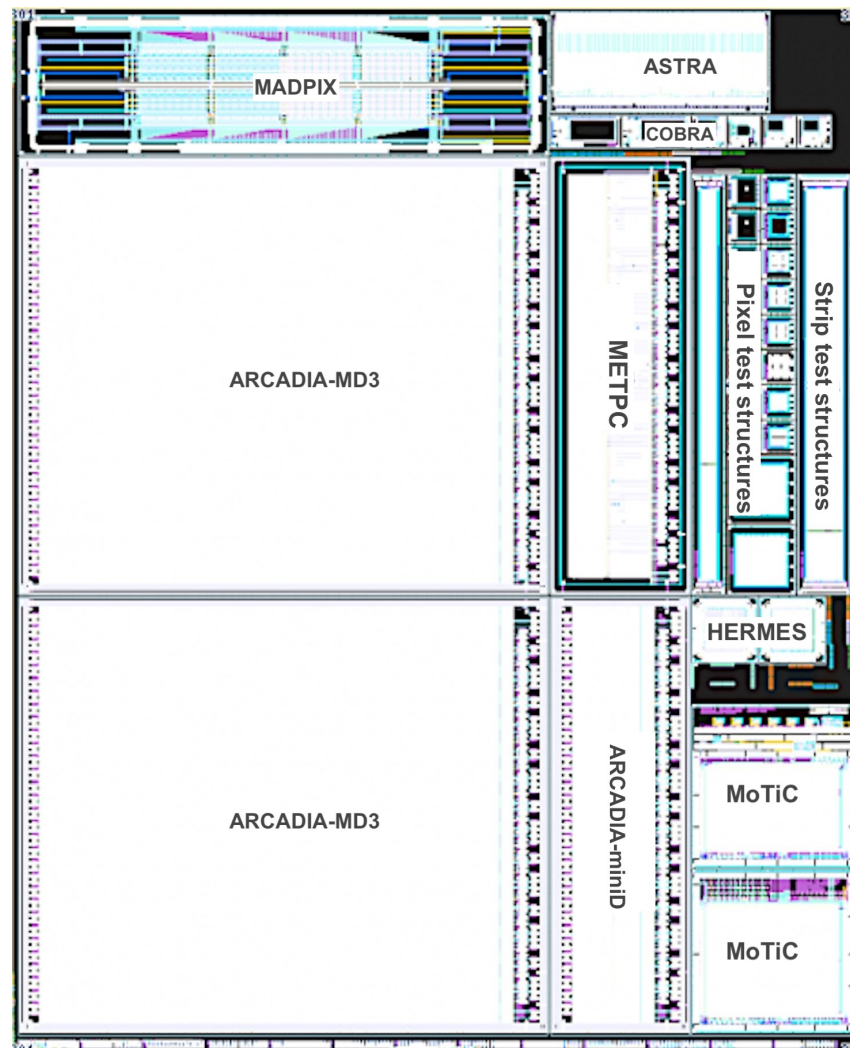
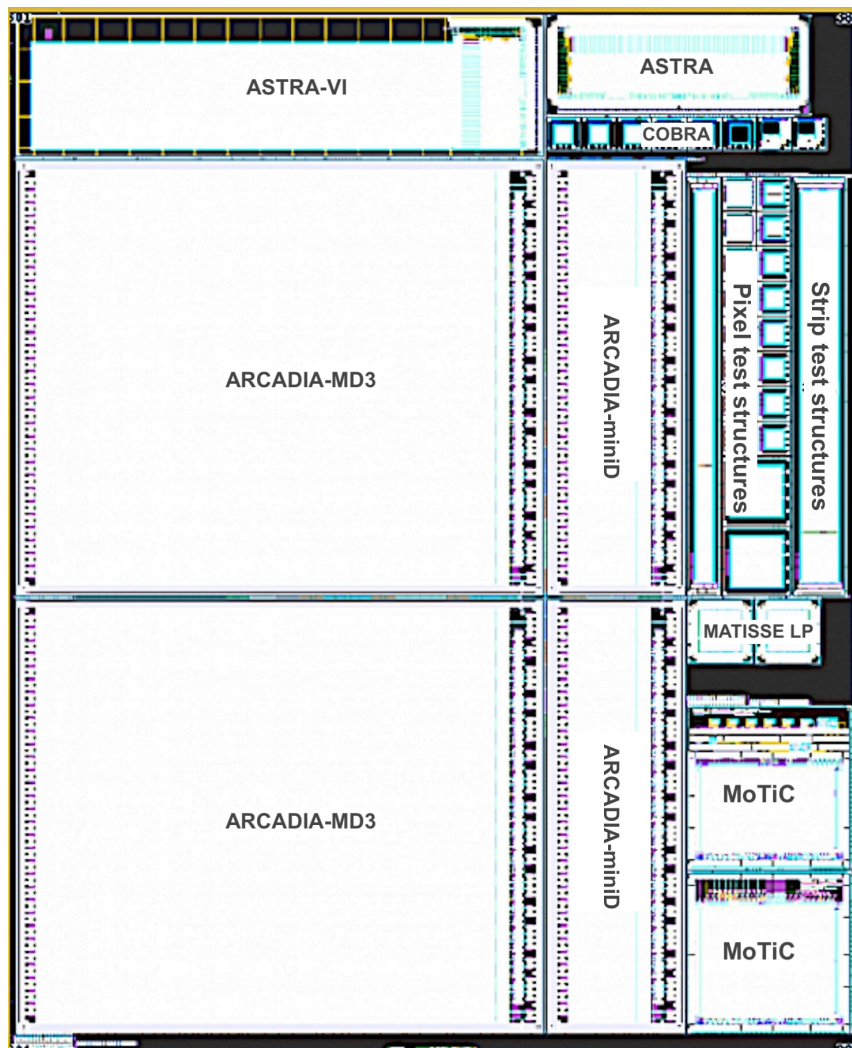
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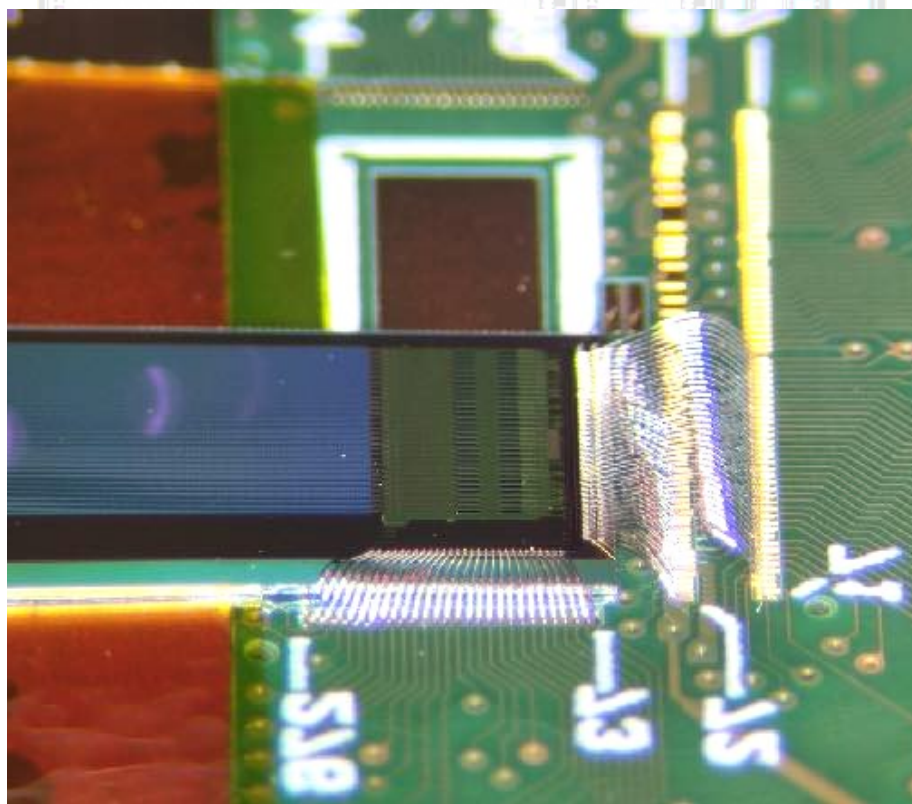
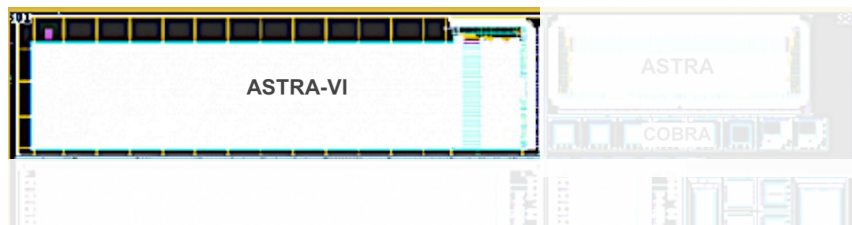
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ARCADIA Technology demonstrators



ASTRA-VI FD Monolithic Active Microstrips



- *Design and Production of continuous and “pixelised” strips, range 10 - 100 μ m pitch*
- *Proof-of-concept: CMOS monolithic strips and embedded readout electronics (active sensor area is 12,8 $\times$ 3,2 mm²)*
- *Analogue (MUX-differential output buffer) and Digital readout (Wilkinson ADC + serialiser)*

