Belle II

# The Belle2-VXD Running Experience and the Mechanical Integration of the DMAPS VTX-Upgrade in the new I.R. Design

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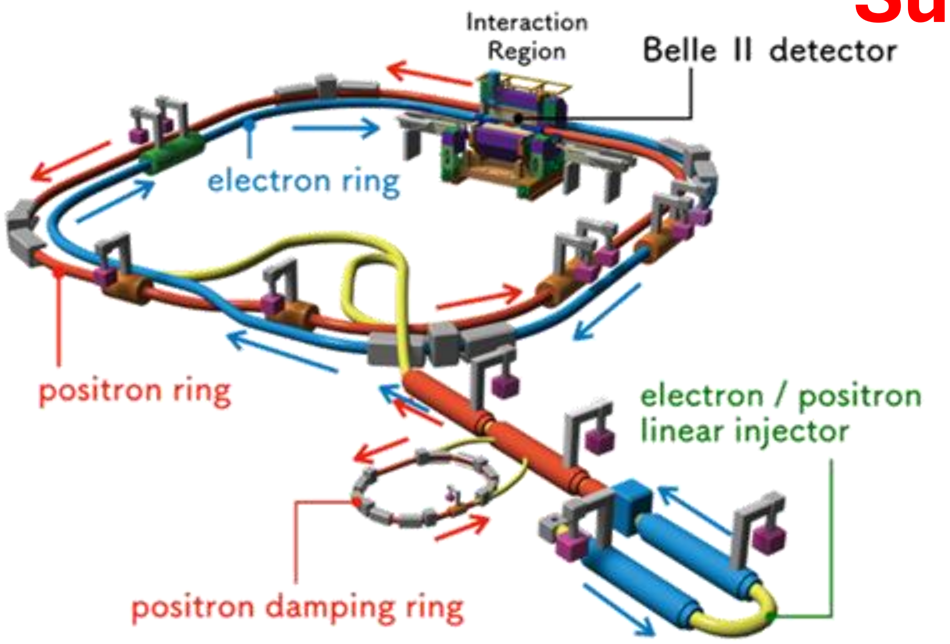
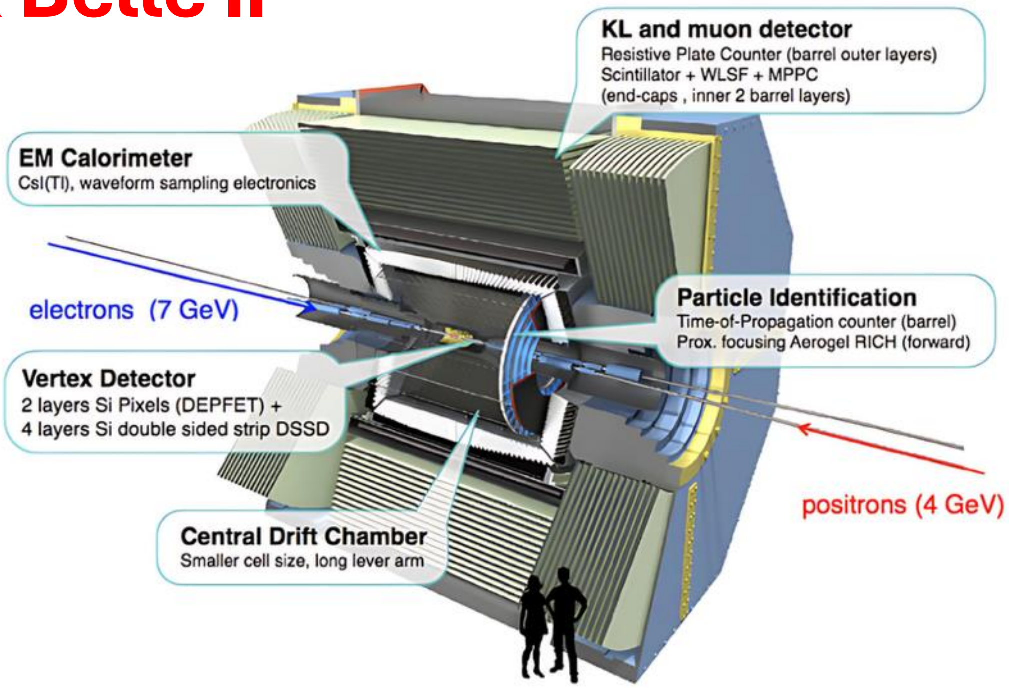
On behalf of PXD, SVD and VTX Collaborations

FCC-ee vertex detector R&D workshop

Pisa, 30-31 October 2025

# SuperKEKB & Belle II

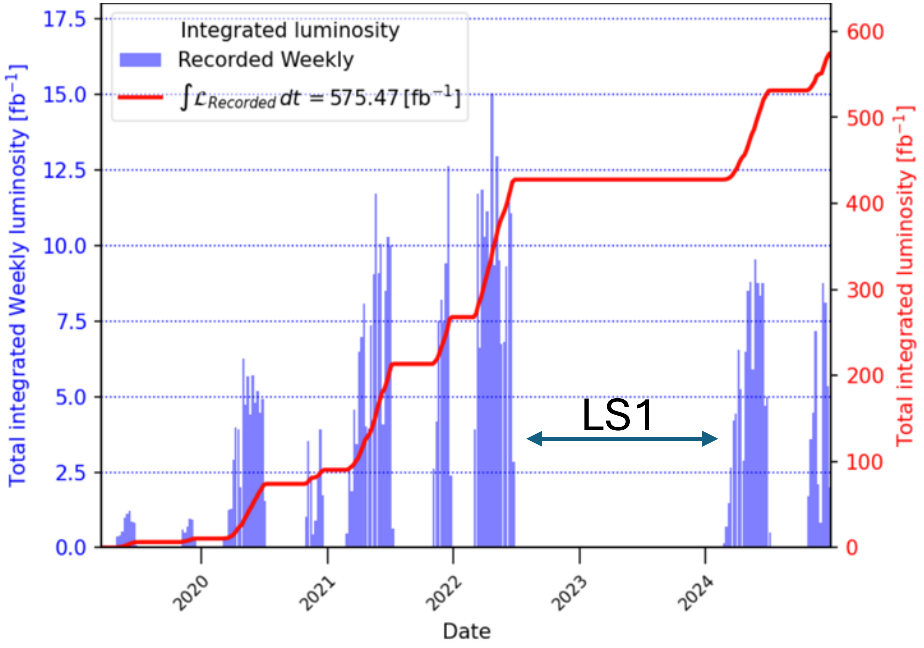



- SuperKEKB: $e^+e^-$ collider with asymmetric beam energies
- $E_{cm}$ [Y(4S)] ~ 10.58 GeV (B-factory)
- Design integrated luminosity: 50 $ab^{-1}$
- Target peak luminosity $\mathcal{L}$ : $6\times10^{35}$ $cm^{-2}s^{-1}$

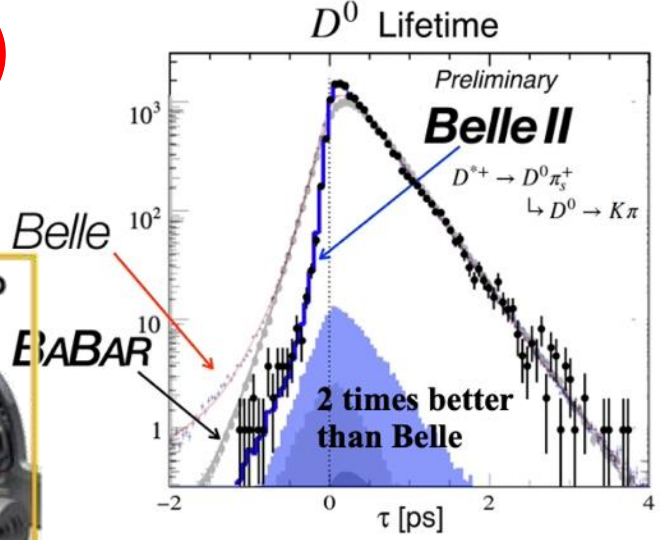
- Start data-taking: April 2019-June 2022 (run1)
- Restart data-taking in 2024 (run2) after Long Shutdow 1
- NOW: restart data-taking (Nov. 2025)

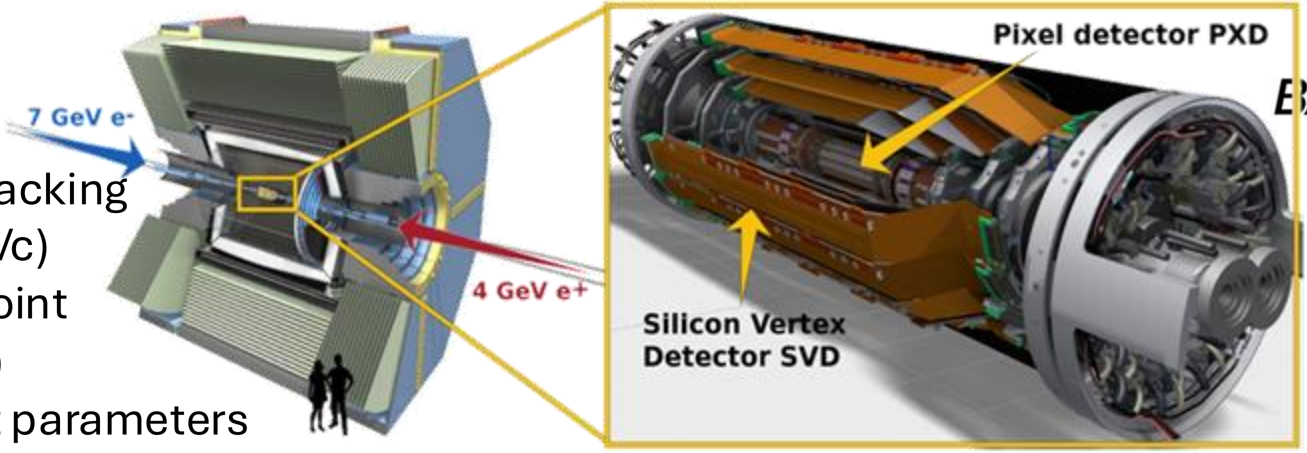
Current integrated luminosity: 575 $fb^{-1}$
Peak luminosity world record: $5.1\times10^{34}$ $cm^{-2}s^{-1}$



# The Belle II Vertex Detector (VXD)

Vertex reconstruction is crucial for time-dependent CP violation and lifetime measurements, enabling precise decay-time resolution for B meson.




## VXD features:

- Excellent Vertexing and Tracking down to low $p_t$ (<100 MeV/c)
- Close to the interaction point (inner layer radius 14 mm)
- High resolution on impact parameters
- Operate in high background environment
- Trigger rate 30 kHz

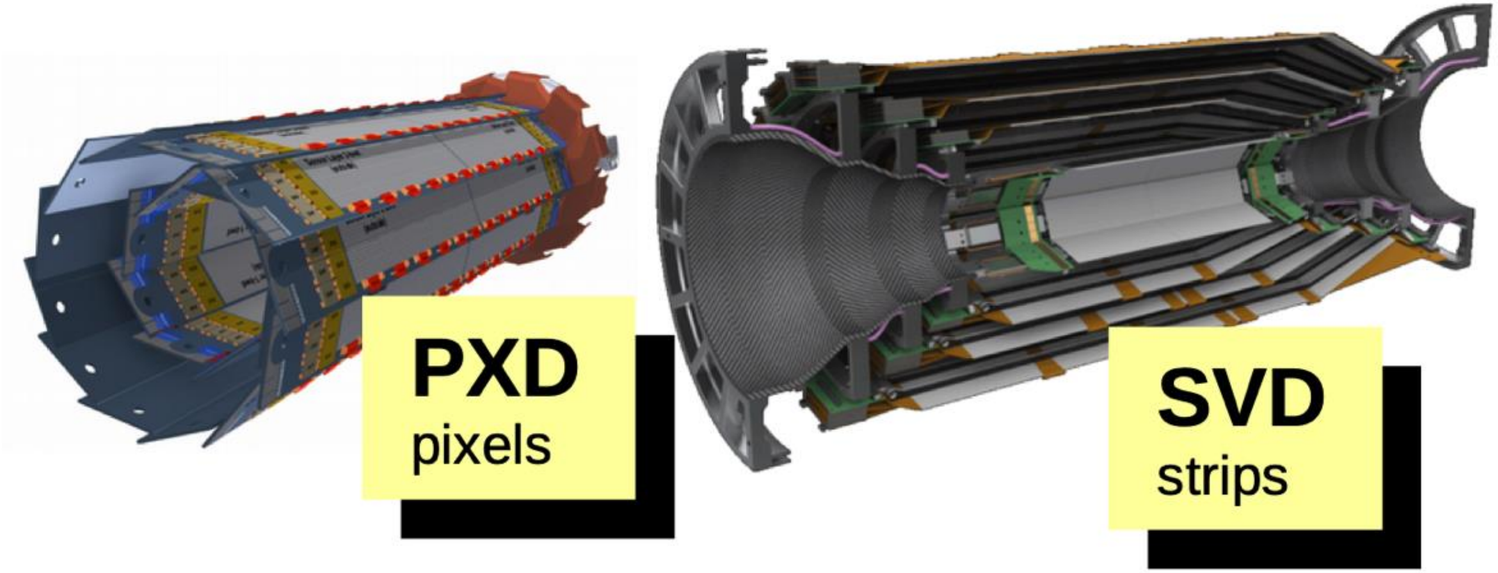
## Two sub-systems:

**Pixel Vertex Detector (PXD)**

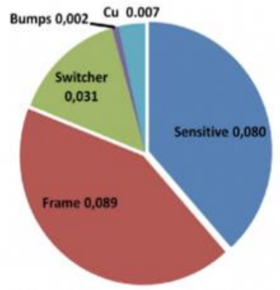
- DEPFET sensors
- 2 Layers : 14, 22 mm radii
- PXD 1: 2019 – 2022 - incomplete 2-layer
- PXD 2: from 2024 (installed in LS1)

**Silicon Vertex Detector (SVD)**

- Four layers double-sided silicon strips
- 39 - 135 mm radii



# The Pixel Vertex Detector (PXD)

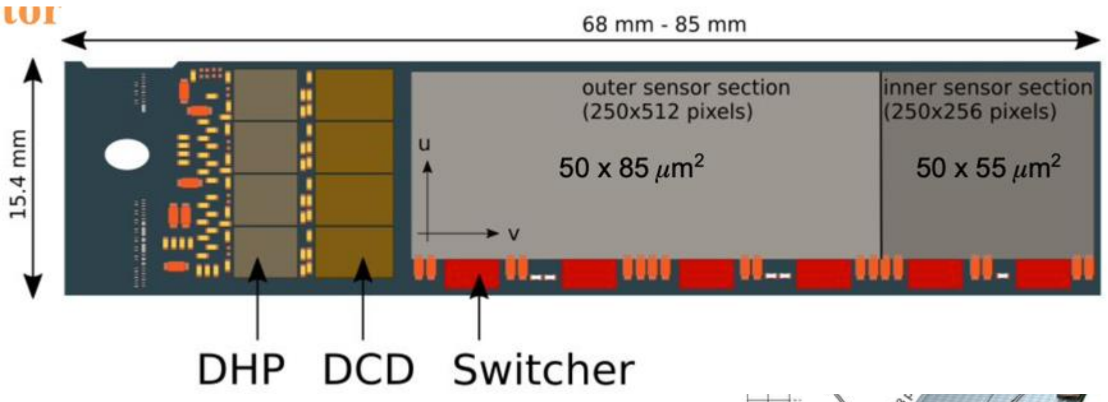



~0.21% $X_0$/ layer material budget

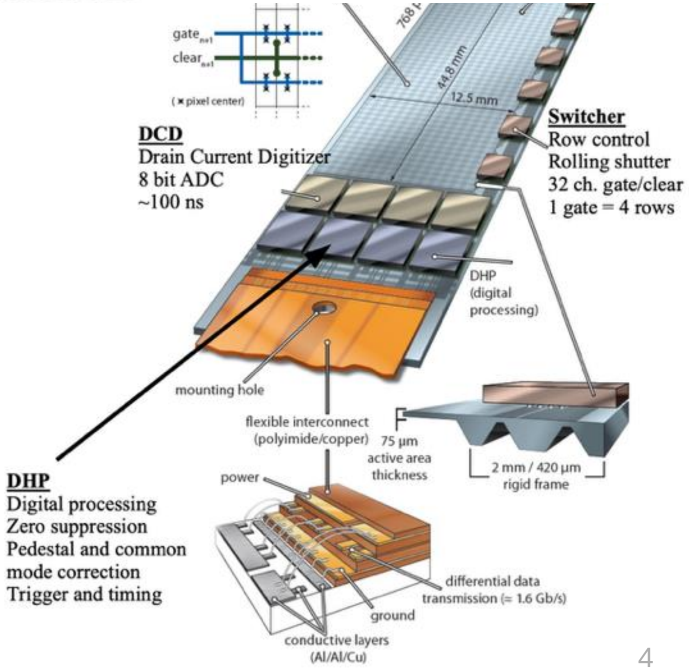
## Depleted P-channel Field Effect Transistor (DEPFET)

Developed at MPG HLL

- Fast charge collection (~ns) into internal gate
- Lower power consumption and heat dissipation in the active area
- Modules: Self - supporting “all - silicon” structure
  - Support frame ~ 525 μm/450 μm thick
  - Monolithic active area 75 μm thick




- Readout Scheme
  - Rolling shutter readout → low power
  - 192 gates, ~100 ns per gate → full frame (integration time) ≈ 20 μs
- Design
  - 1% occupancy (Layer 1)
  - system limit ≈ 3% (DHP/DAQ/tracking)
- Sensor Scale
  - 40 sensors, each 250 × 768 pixels → ~8 Mpixel total




### ASICs on module

- Switcher: consecutive row selection for data readout
- DCD (Drain Current Digitizer): Analog to digital conversion of signal
- DHP (Data Handling Processor): Digital Processing, data formatting

# PXD Design: Modules, Ladders, and Cooling

**Module**

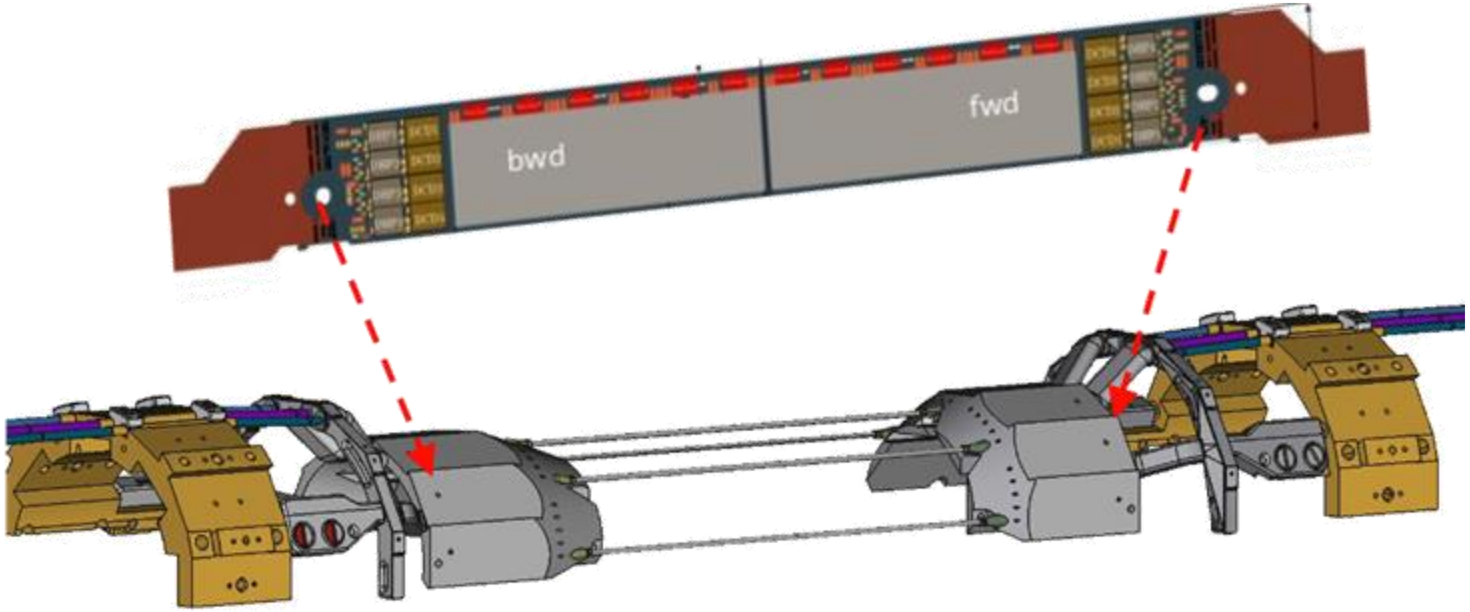
- 2 modules glued to one ladder
- 20 ladders in total (2 modules per ladder)

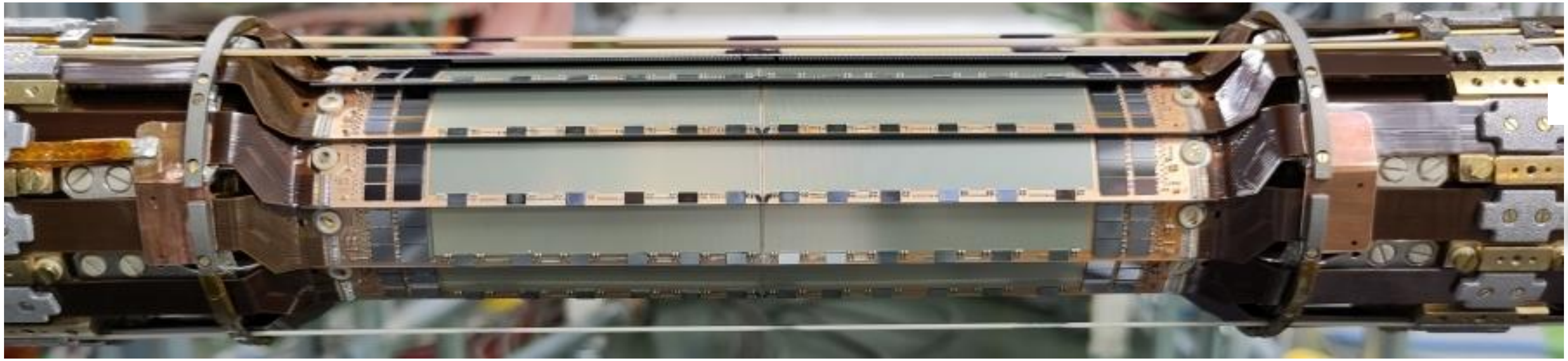
**Ladders**

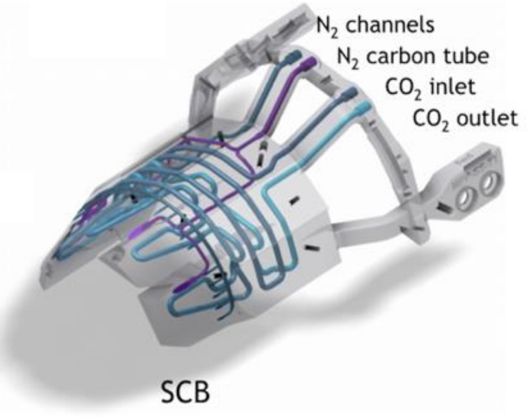
- 10 ladders – 1 half-shell
- Screwed on support colling block (SCB)
- Half-shell (HS) mounted on beam pipe

**Cooling**

- ~ 9 W per module = ~ 360 W for full detector
- 2-phase $CO_2$: DHP + DCD (8 W)
- $N_2$ gas: Switcher + sensor (1 W)



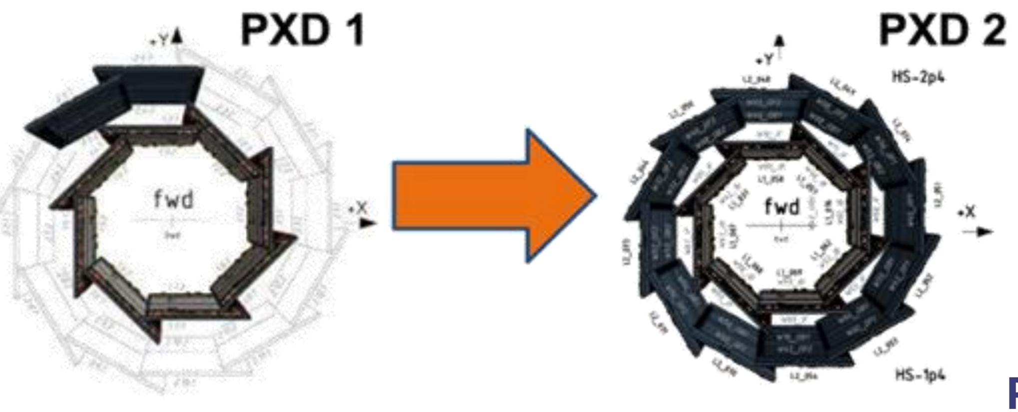


# PXD 2: Installed in 2023 with fully equipped 2nd layer

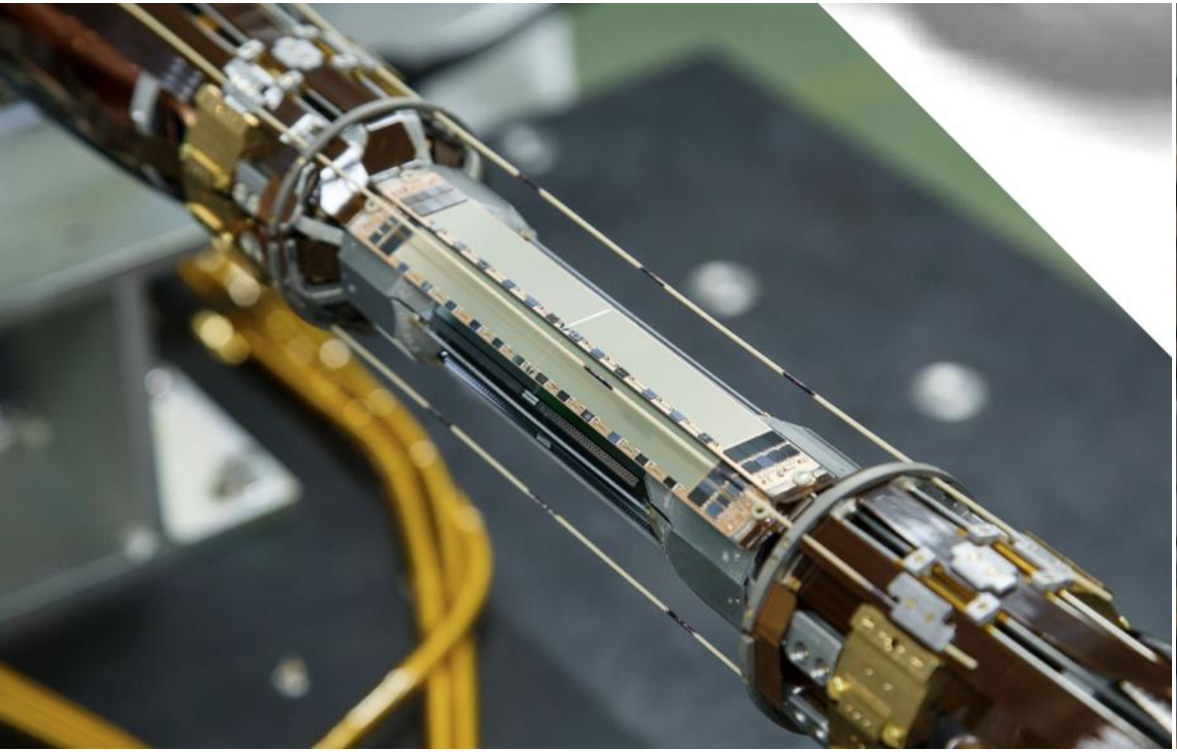
## RUN1 PERFORMANCE

- Di - muon hit efficiency
  - ~ 99 % in fiducial region
  - ~ 96 % in tracking acceptance
  - Noise performance < 1 ADU (~200 $e^-$)
- Impact parameter resolution:

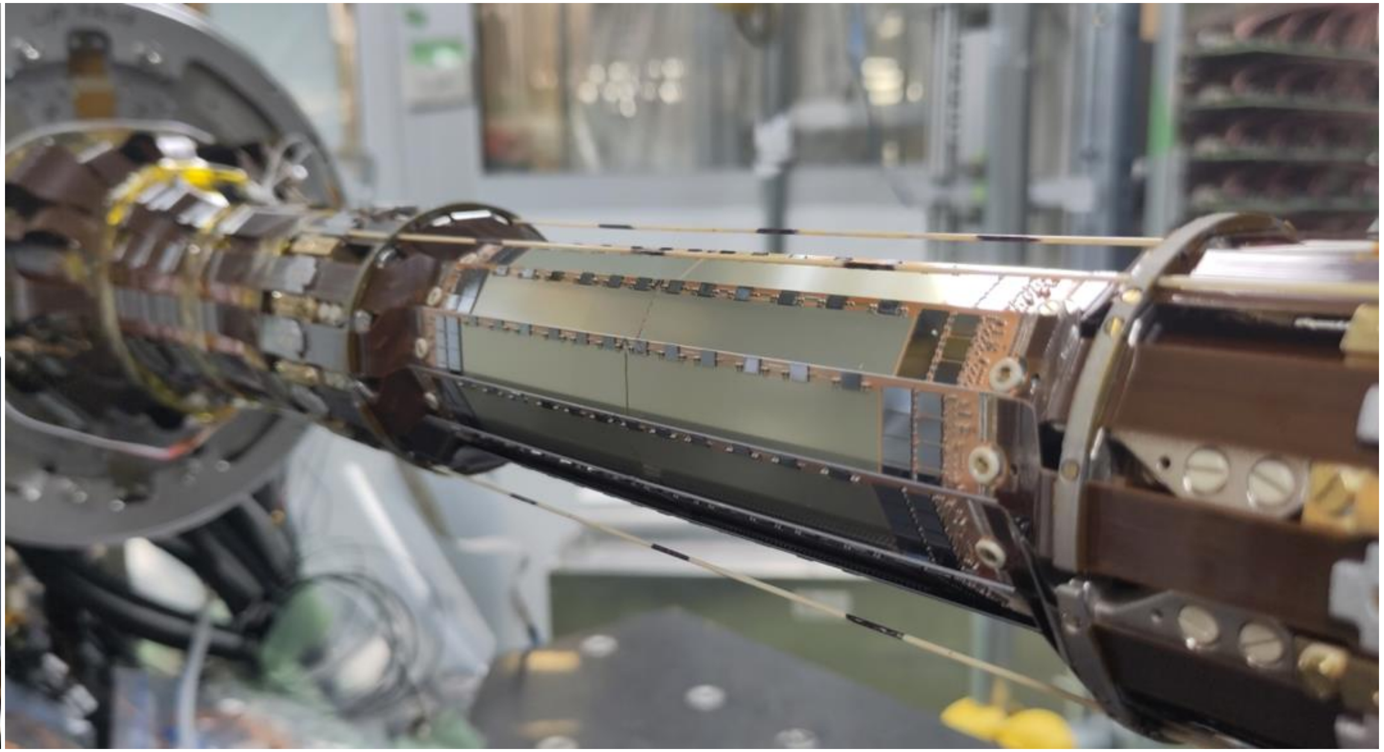
  ~1.5 - 2 times better than Belle




PXD 1: 2019 – 2022



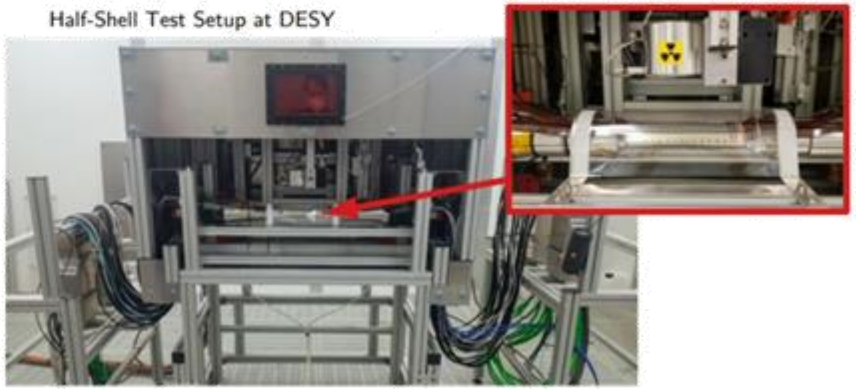
PXD 1: 2024 →

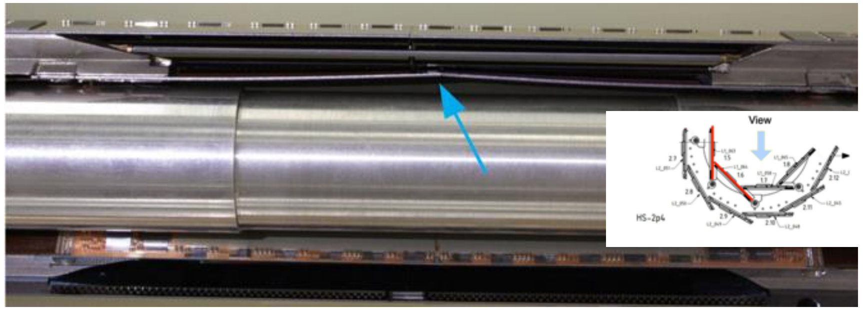


# Commissioning of PXD 2 – From DESY to KEK Installation

## Commissioning at DESY

- Conducted source scans and system tests on half-shell setups
- Tested power supply, DAQ, $CO_2$, and $N_2$ cooling with Aluminium dummy beam pipe
- Two ladders were damaged by glue joint failure, highlighting sensitivity to heating and bending
- The half-shell was repaired with ladder replacements and improved mounting, with careful monitoring of temperature and bending



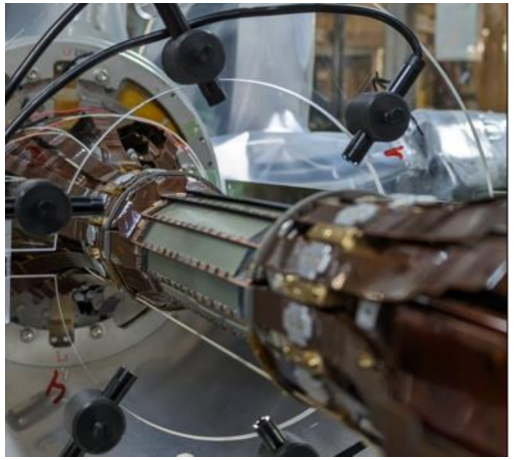



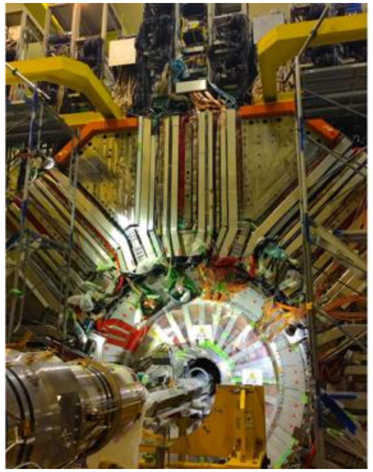

## Commissioning at KEK

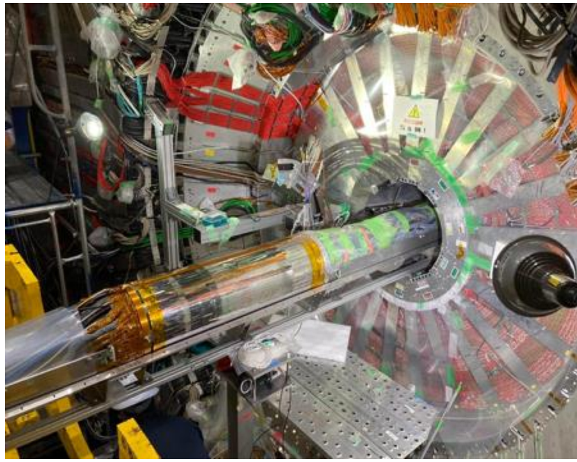
- First operation of full PXD 2
- Issue:
  - 2 ladders with significant bowing
  - One module with high noise

## Installation in Belle II

- Attached SVD and installed in Belle II
- Perform cosmic runs to study bending more precisely





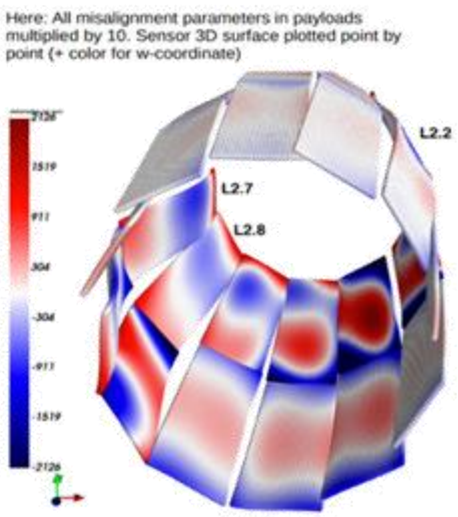


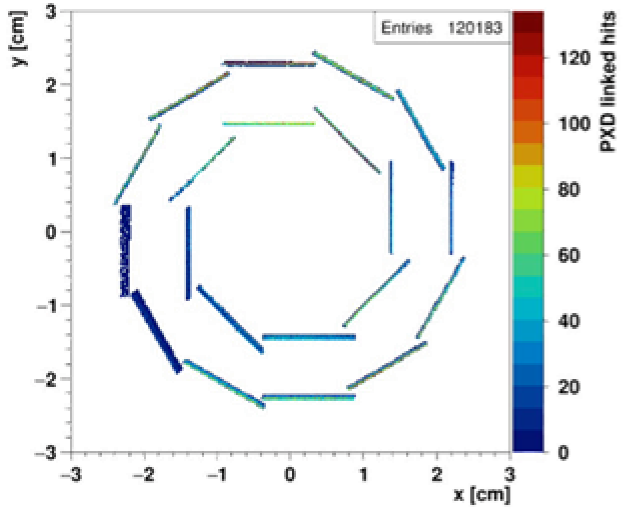
# PXD 2 Cosmic Study and Operation Performance

## PXD 2 cosmic data taking

- Study ladder behaviour with cosmic data
  - Test with different cooling setups
- Bending in 2 ladders (4 Modules):
  - ~1 mm sagitta observed, smaller than the 2 mm, safe limit from endurance studies

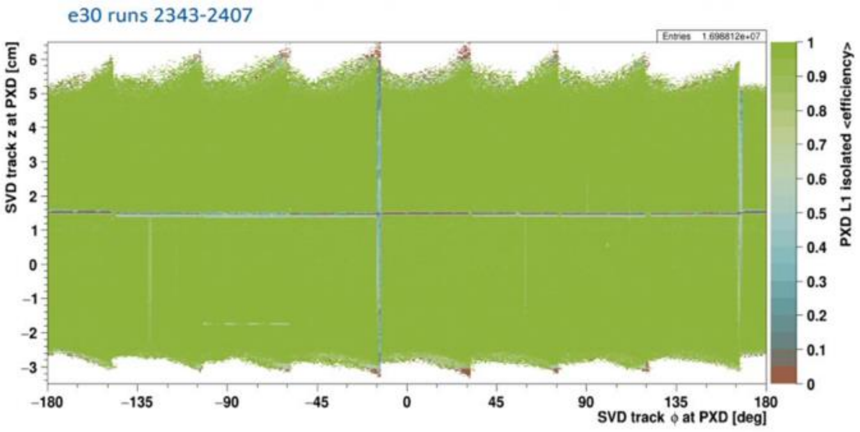
✓ Decided to keep both ladders off during operation start



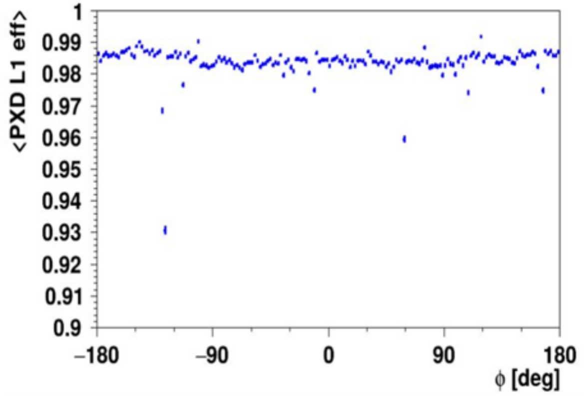




## Operation Performance from March - April 2024

- Running with 35/40 modules:
  - 4 Modules off because of bowing
  - 1 Module off because of noise
- L1 and L2 efficiency > 98 % in the fiducial region
- Operation temperature high but within limits
- Noise <1 ADU
- Smooth operation with minor down times




Efficiency map for the PXD Layer 1 modules




Efficiency as a function of the azimuth angle Φ

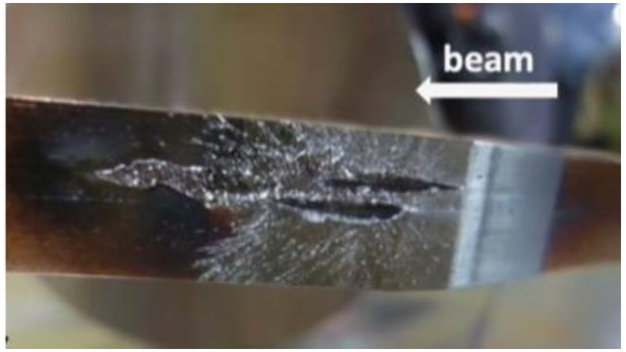
# Sudden Beam Loss (SBL) and Damages

**Two beam loses with high dose in PXD**

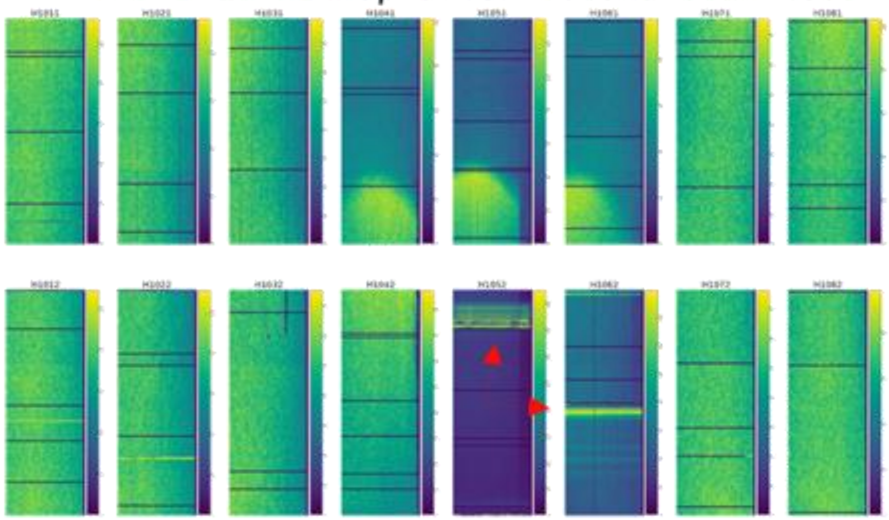
Possible Reason for SBL:

- Vacseal residue in the vacuum system
- Does other sources of SBL exist ?

SBL effects on a collimator

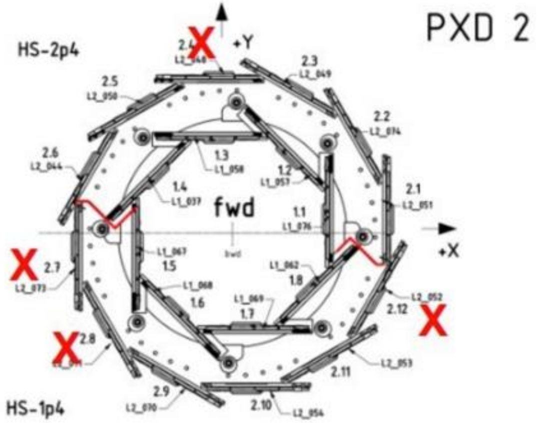



PXD 2 L1 hitmap after second beam loss



**SBL effect on PXD**

- In May 2024: two major SBLs damaged Switcher ASICs, causing ~2% PXD readout loss and increased currents
- After the 2nd SBL PXD 2 was powered down
- PXD 2 remains functional with good performance
- Additional SBL events may cause further damage




Therefore, PXD 2 will be turned off during beam operations to prevent further damage until stable beam conditions are restored!
During this summer shutdown we cleaned from vacseal residual the areas of the beam pipes.

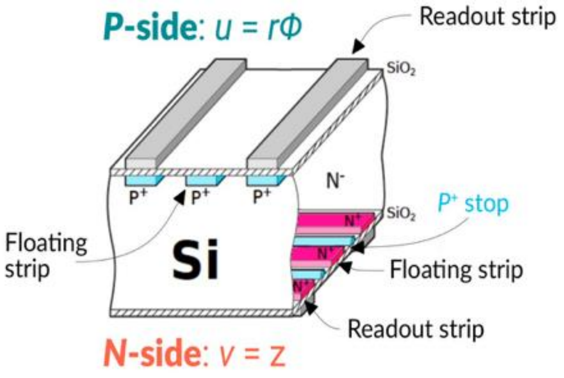
**Future Plans**

- Improving faster detection of beam instabilities earlier beam abort
- Decided to turn off PXD 2 for now to investigate:
  - To optimize beam operation
  - To solve origin of SBL event

Under development a fast-shutdown PS board to rump down the Switcher ASICs rapidly (<30 μs) in the event of on SBL “precursor” to minimize the risk of SBL-induced damage

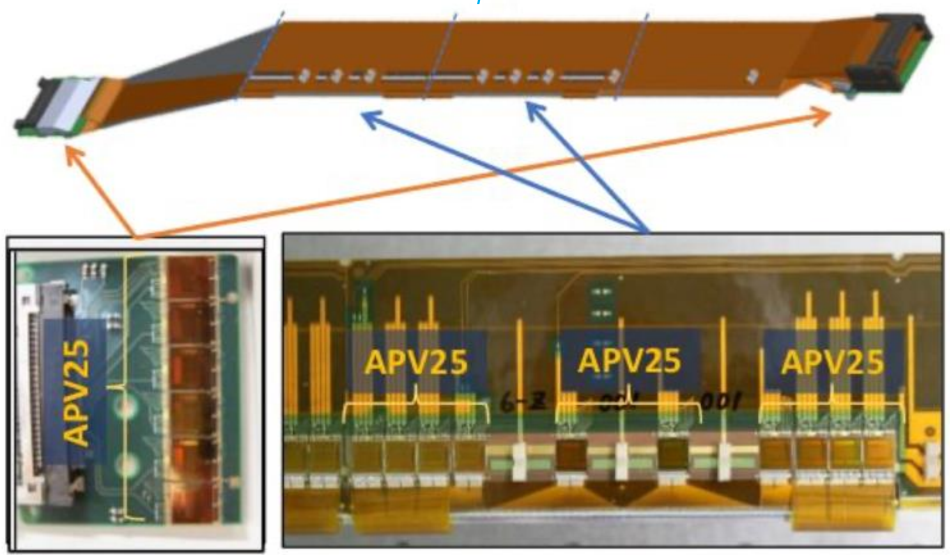
More information on SVD:
K. Adamczyk et al 2022 JINST 17 P11042

# SVD Sensor Design



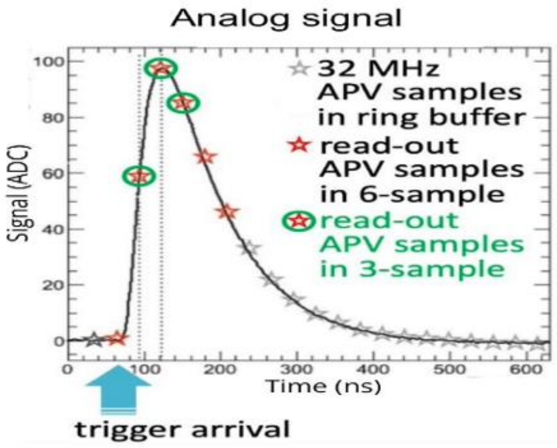

## Double Sided Silicon Strip Sensors (DSSD)

- 172 DSSD with area coverage 1.2 $m^2$
- Bias voltage: 100 V
- Perpendicular strips to provide 2D spatial info
- Depletion voltage: 20 - 60 V
- Strip pitch: 50/75 μm (r-ϕ) and 160/240 μm (z)
- Front-end electronics: APV25 chip, 50 ns shaping time
  - Originally developed for the harsh radiation environment at the LHC
  - 192-cell analog pipeline / 128 channels
  - >100 Mrad tolerance, 0.4 W power
- Cooling: two-phase $CO_2$ system
  (-20° C with PXD1 and -25° C with PXD2 )
- Material budget: 0.7 % $X_0$ /layer




## APV25 Operation mode

- Operated in multipeak mode @32 MHz
  (⅛ of SuperKEKB bunch crossing frequency of 254 MHz)
- (By default) 6 samples of analog output are recorded to reconstruct output waveform
- Alternative 3/6 mixed mode tested for high-luminosity to reduce dead-time



# SVD Operation during Run 1

## Performance in Run 1 (March 2019 – June 2022)

**Cluster charge**

- Stable throughout and matching the expectation;
 $24ke^-$ for a MIP passing through a ~320 μm thick silicon sensor

**Cluster SNR**

- Very good cluster SNR in all 172 sensors
- Small reduction in 2022 due to radiation damage

**Position resolution**

- Stable position resolution within 10–25 μm observed, as expected from strip pitches

**Excellent SVD hit-time performance**

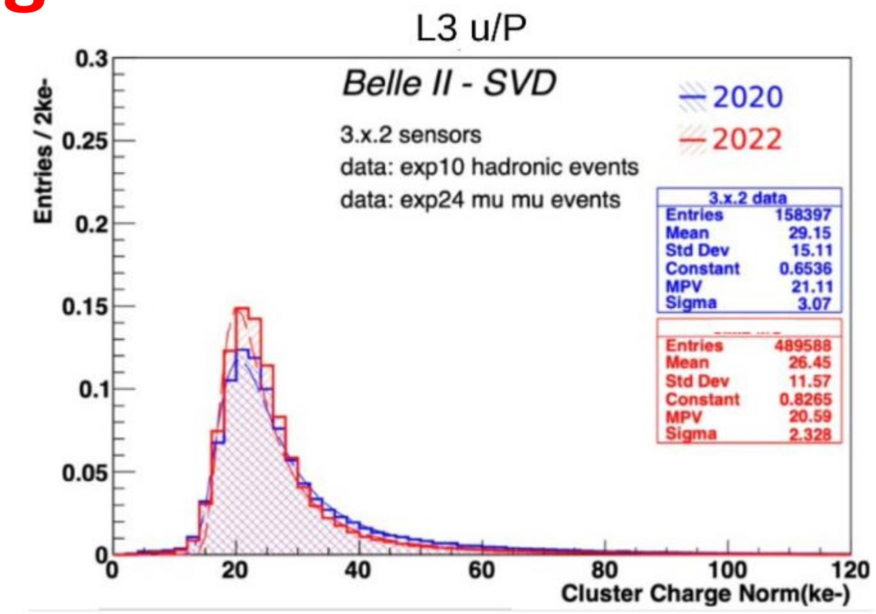
- resolution < 3 ns for signals
(time range of beam-induced background ~100 ns)

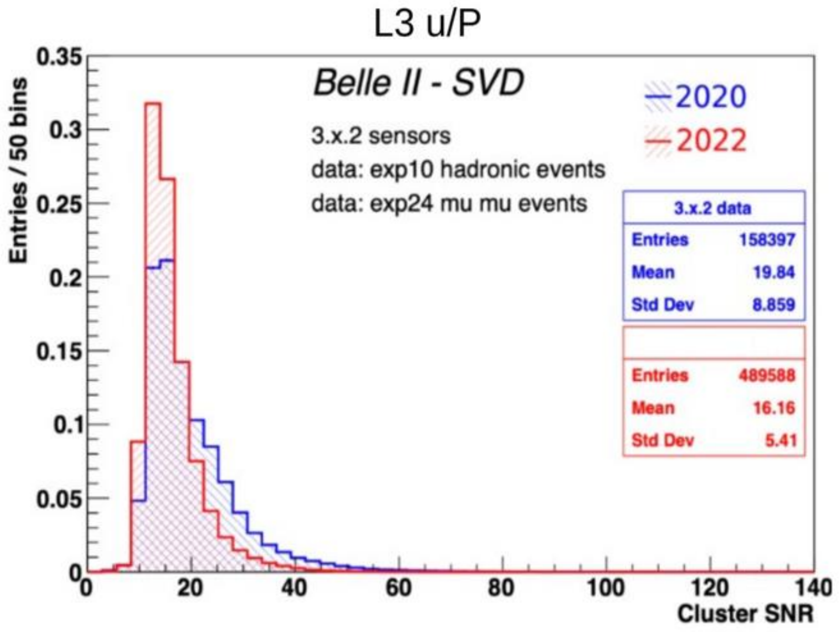
**Hit efficiency**

- Hit efficiency > 99% for most of the sensors

**Masked strips**

- Total masked strips < 1%

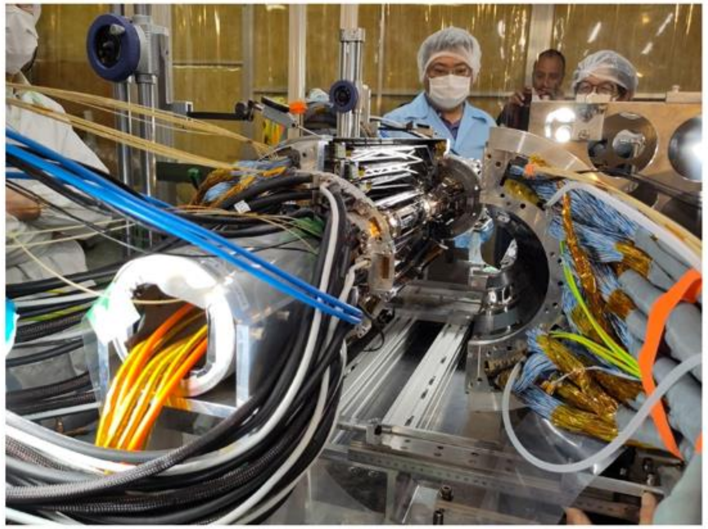


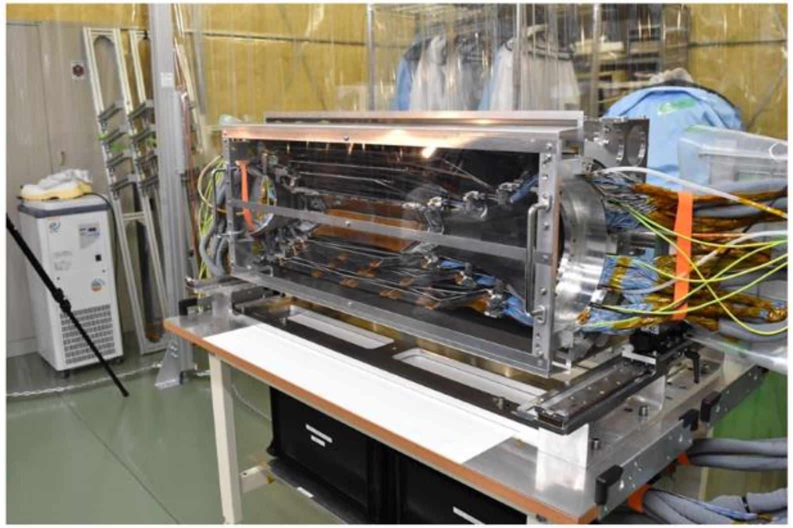
# SVD During long shutdown 1

Feb. 2023

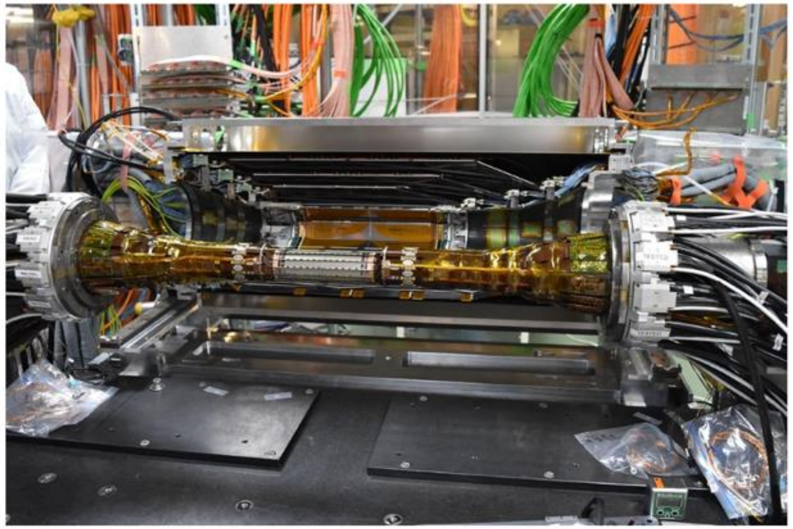
Opening the VXD



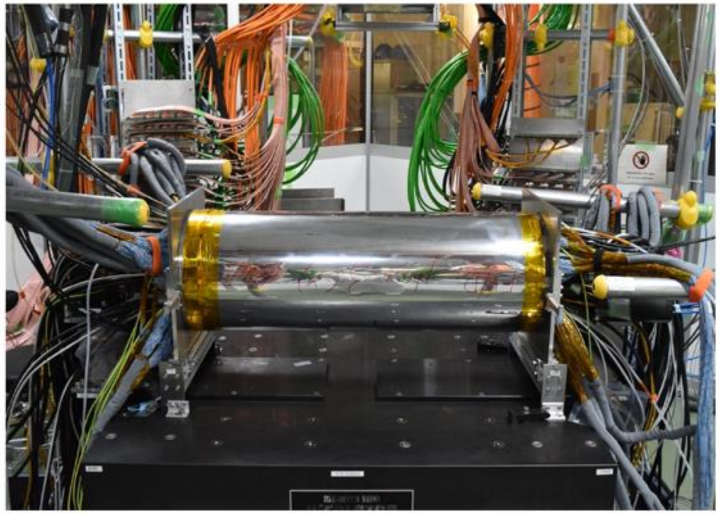
SVD Half



PXD insertion



Completed VXD



Towards Belle II

Reinstalling

August 2023

# SVD Operation during Run 2

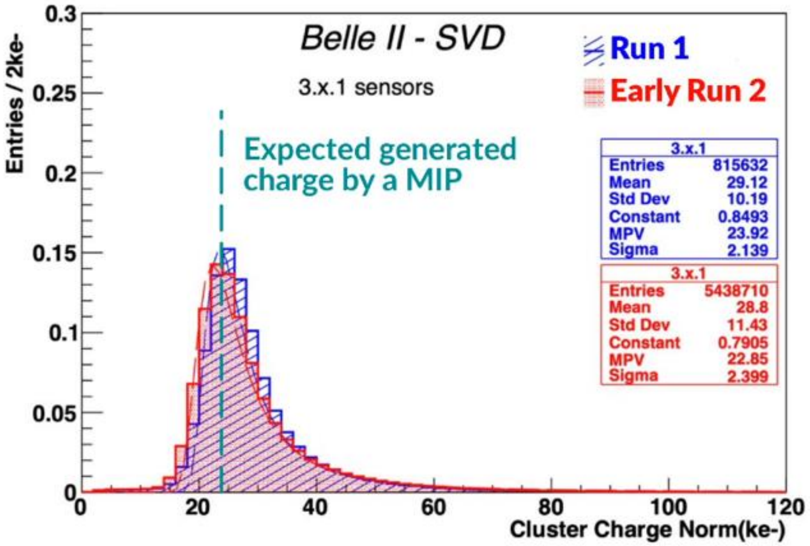
SVD was extracted and reinserted during PXD 2 installation (LS1), making Run 2 performance crucial

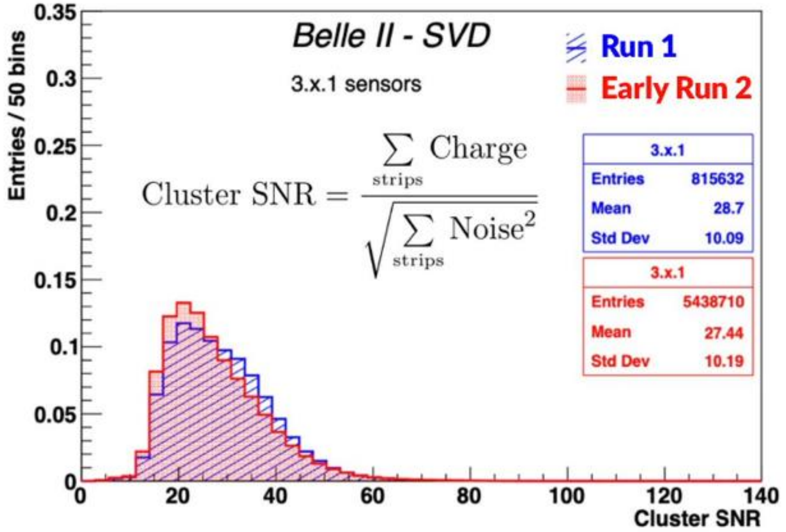
### Run 2: Feb-July+Oct-Dec 2024:

Smooth and stable operations!

### Cluster charge and SNR

- No significant changes in cluster charge and SNR

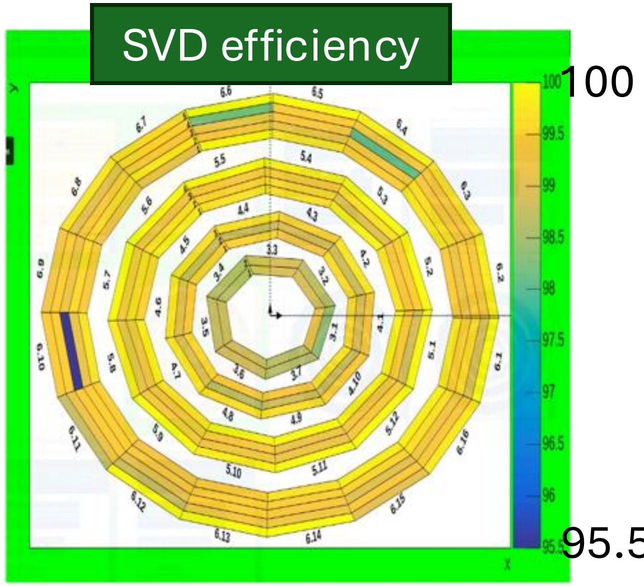



### Sensor efficiency

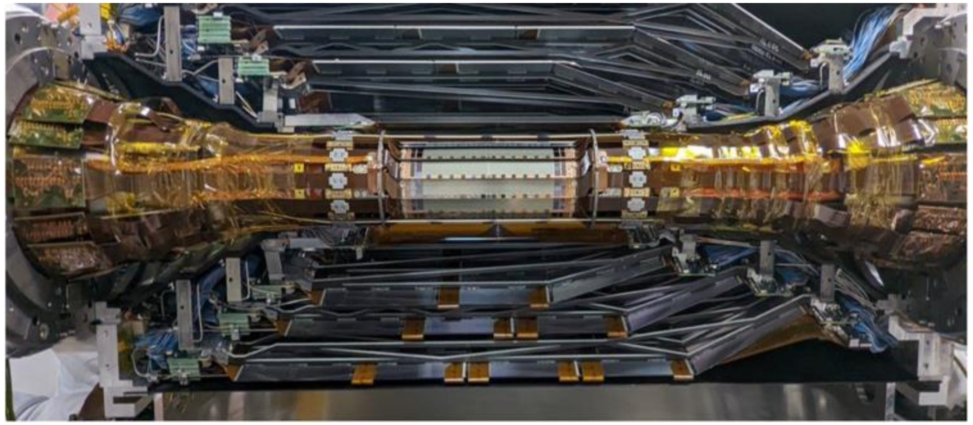
- Sensor efficiency is very high (>99%) for most of the sensors

Occupancy during this run ~1%




### Future Plan

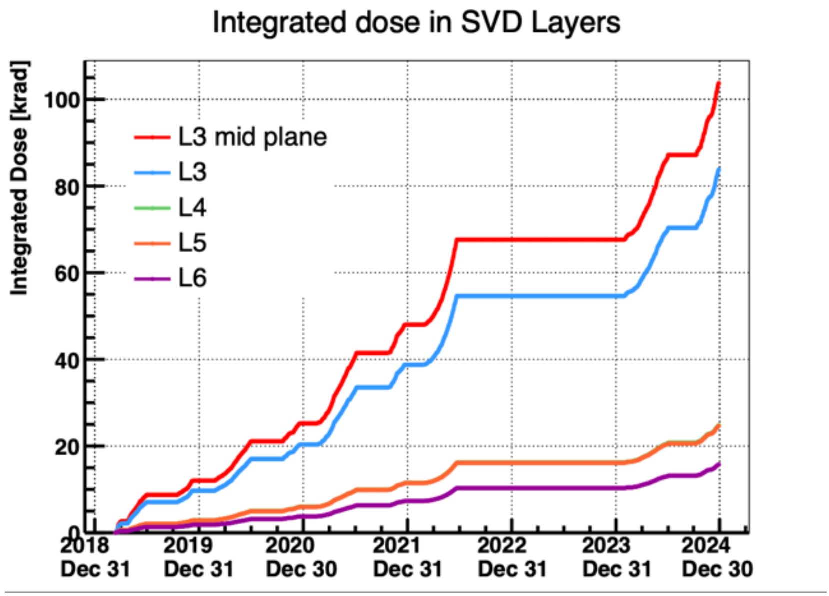
- New algorithms based on time resolution to suppress background and preserve tracking performance at high rates
- Maintain SVD performance with higher occupancy anticipated with increased SuperKEKB luminosity



# Radiation and Beam Background Effects on SVD

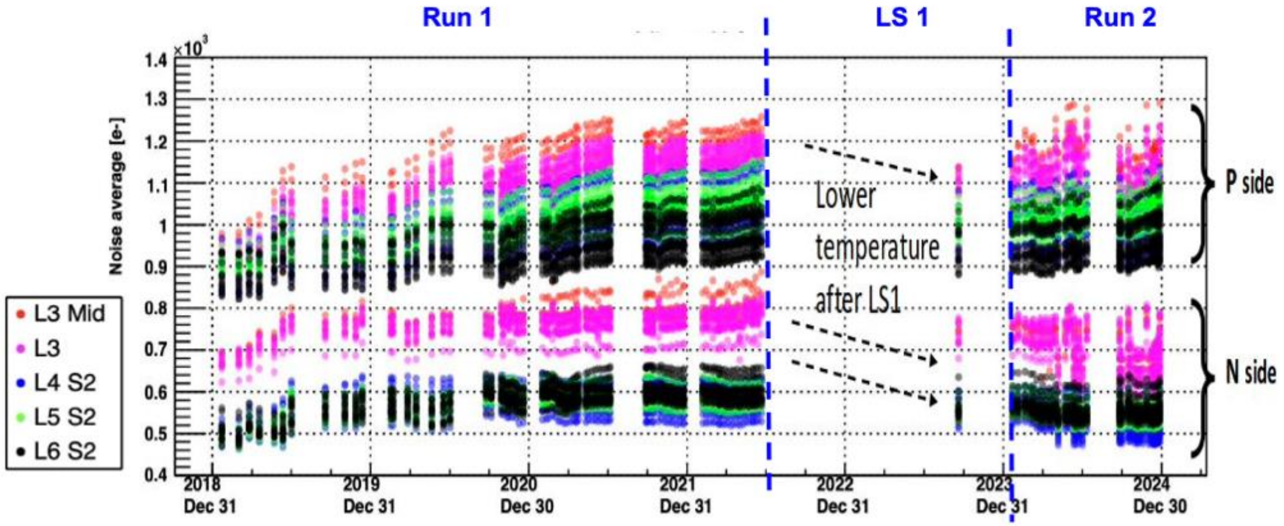
## Beam Background Effects

- Sudden beam loss are a risk, but no pinhole defects observed in DSSDs during Run 2
- Integrated radiation dose can still degrade sensor performance: increase leakage current, strip noise, decrease charge collection (SVD limit from S/N ratio: 6 Mrad).




## Radiation Dose Measurements

- Total integrated dose on Layer 3 mid-plane: ~100 krad, equivalent to ~$2.5\times10^{12}$ n/cm$^2$ (measured via diamond detectors) with no observed performance degradation
- Sensor noise increased 10-35% in Run 1 (due to radiation)
- Partially recovered (10%) after LS1 (annealing + lower cooling temperature)



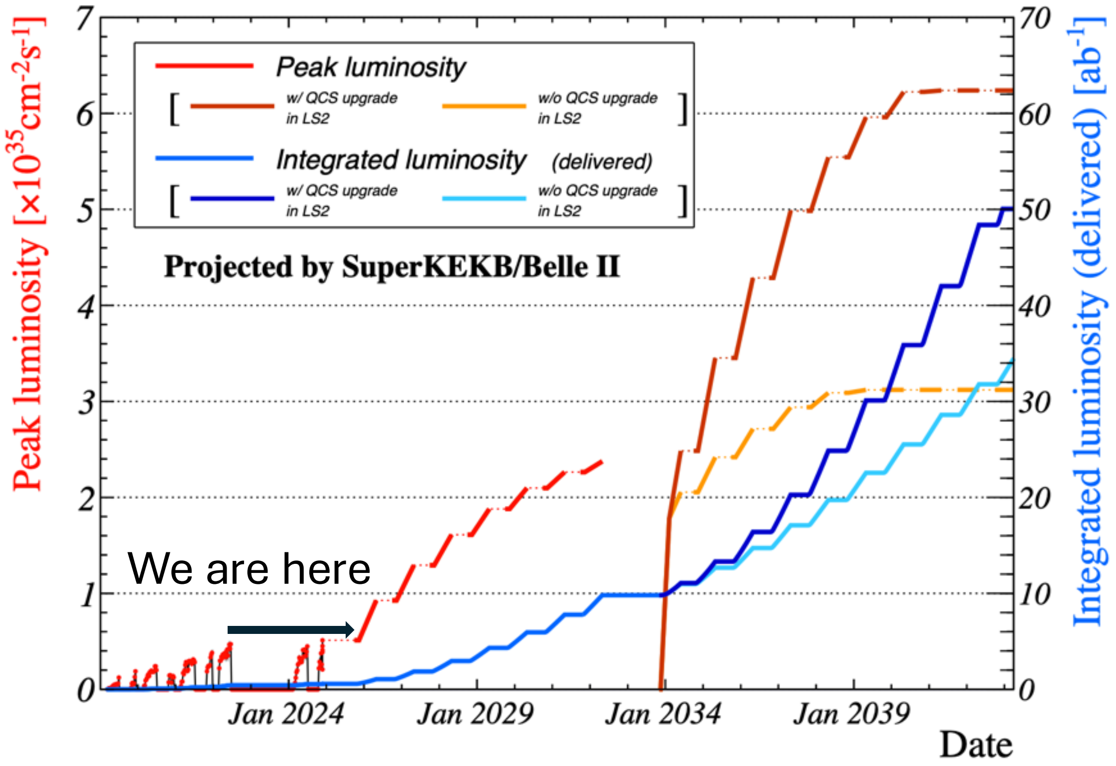

## SVD Performance Resilience:

- No significant degradation in SVD performance was observed
- Current SVD hit occupancy <1%, increased during Run 2 due to machine conditions
- Sensors still collect charge effectively after 10 Mrad from test campaign

# Upgrade Proposal VXD → VTX

To achieve the target $\mathcal{L} = 6 \times 10^{35}\,cm^{-2}s^{-1}$ and $\int\mathcal{L}dt = 50\,ab^{-1}$ a major re-design of the I.R. (i.e. QCS upgrade) is needed.

- The VXD provides excellent performance at occupancy < 1%.
- Performance degradation expected in high BKG scenario at target luminosity, where (with large uncertainties in the extrapolation):
  - PXD layer 1: 32 $Mhz/cm^2$ → 2% occupancy
  - SVD layer 3: 9 $Mhz/cm^2$ → 9% "




## A new fully pixelated CMOS detector proposed to replace the VXD. Requirements:

- Improved tracking resolution and space-time granularity to cope with increased backgrounds at target luminosity:
  - Hit rate up to 120 $Mhz/cm^2$ / resolution < 15 um / Integration time 50-100 ns
- Improved radiation tolerance to ensure long-term detector performance:
  - TID: 100 Mrad
  - NIEL: $5\ 10^{14}\ n_{eq}/cm^2$
- Reduced material budget about 3.0% $X_0$ (sum of all layers)
- Adapt to the new interaction region re-design
- VTX Installation planned during the long shutdown 2, starting in 2032, TDR preparation in 2027.

Belle II Upgrade CDR https://doi.org/10.48550/arXiv.2406.19421

# The Vertex detector upgrade: VTX

## ❑ Concept: 6 straight layers with DMAPS

- Higher space-time granularity & lower material budget
  - More robust in high background & better tracking & vertex resolution at low momentum
- Lighter services & “easy” geometry
  - adaptable to potential changes of Interaction Region

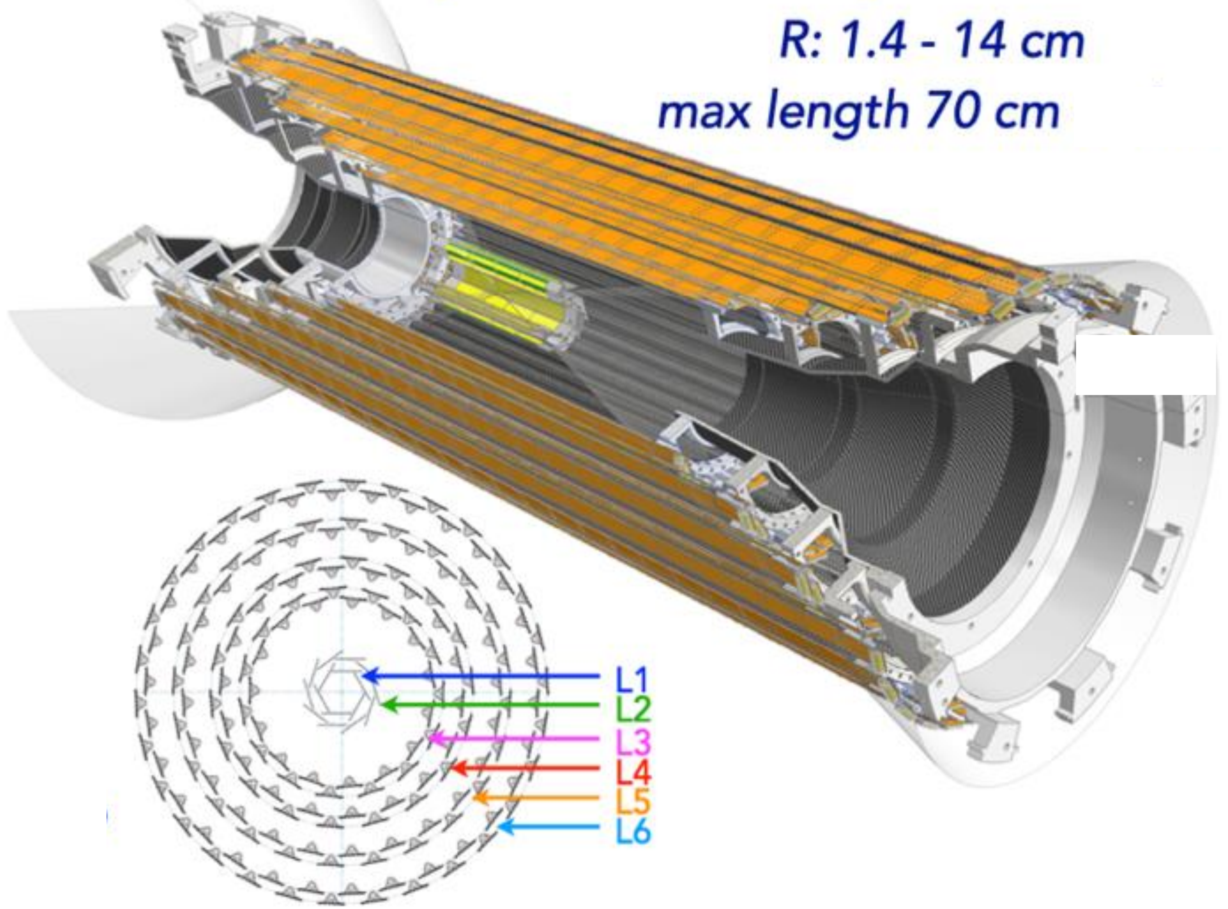
## ❑ Technical choices

- Identical pixel sensor on all layers: **O**ptimized **BEL**le II p**IX**el (**OBELIX**) chip
  - Thin DMAPS sensor, derived from TJ-Monopix2: 33 um pitch & 50 ns timestamping
  - Operated at room temperature: power 200 → 300 mW/cm$^2$
- **iVTX**: innermost 2 layers, all-silicon, self-supported, different cooling options under evaluation → 0.3 % $X_0$
  1. Thermal conduction by thermal pyrolytic graphite
  2. Liquid in Al thin pipes
- **oVTX**: 4 outer layers, carbon fiber frame, water cooled: 0.6→0.8 % $X_0$

## Baseline VTX layout with 6 layers

*R: 1.4 - 14 cm*

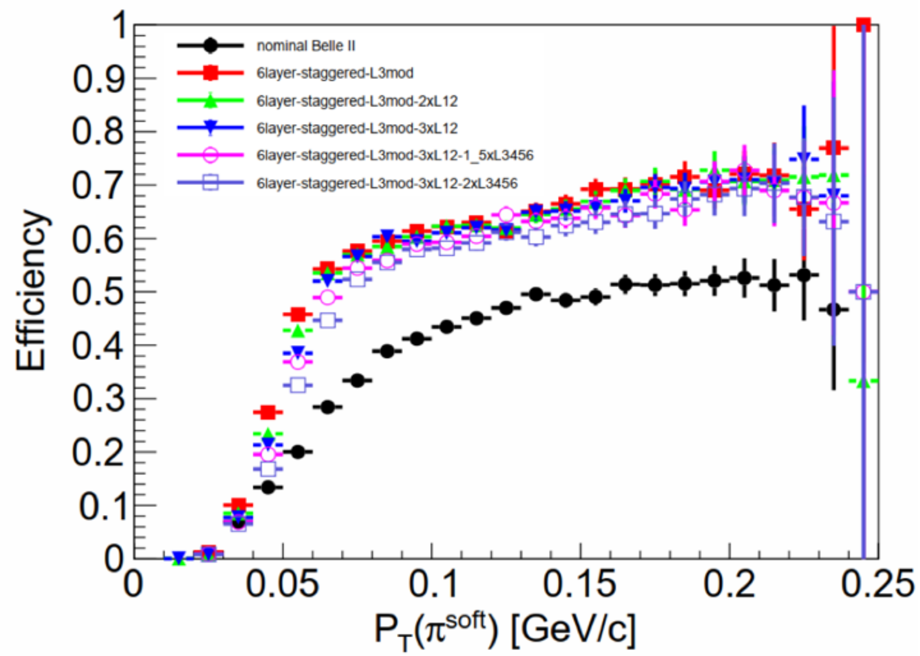
*max length 70 cm*

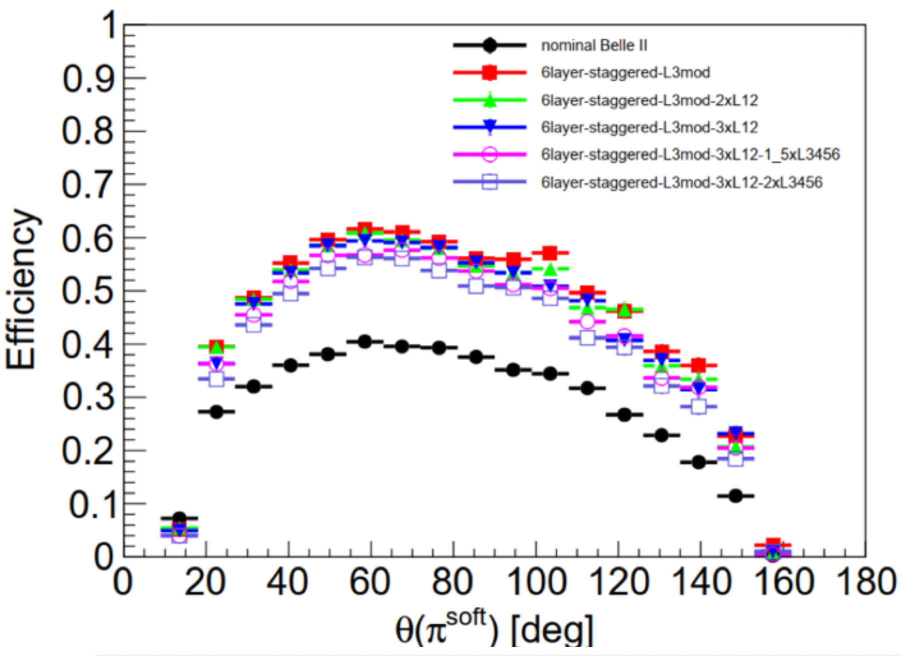



Most conservative BKG extrapolation

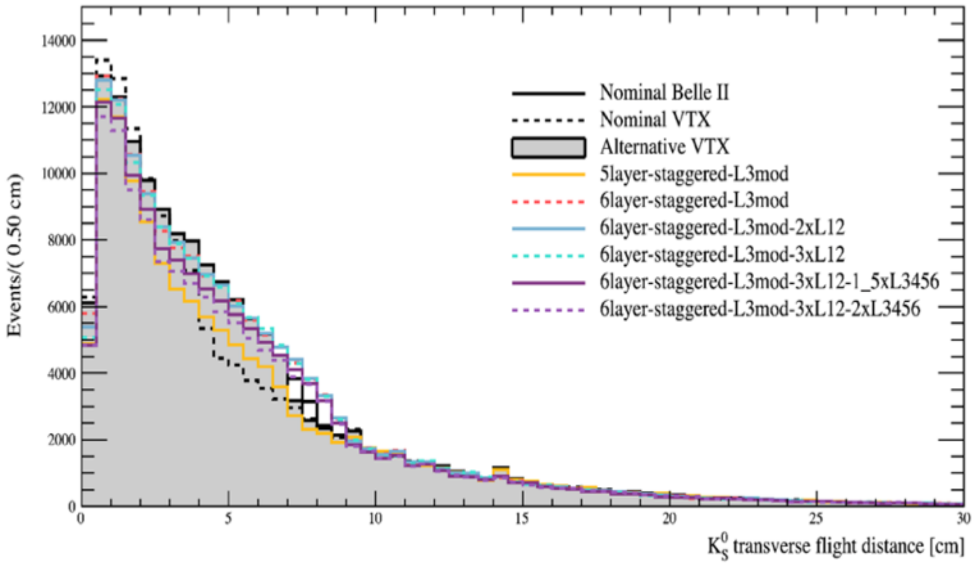
| | L1 | L2 | L3 | L4 | L5 | L6 | Unit |
|---|---|---|---|---|---|---|---|
| Radius (mm) | 14.1 | 22.1 | 62.5/69.0 | 82.5/89.0 | 108/114.5 | 133.5/140 | mm |
| # Ladders | 6 | 10 | 30 | 36 | 48 | 60 | |
| # Sensors per ladder | 4 | 4 | 12 | 16 | 20 | 24 | per ladder |
| Mat budget (% X0) | 0.3 | 0.3 | 0.6 | 0.6 | 0.6 | 0.6 | % X0 |
| Expected hit rate* (MHz/cm2) | 34 | 16 | 1.13 | 0.76 | 0.41 | 0.27 | MHz/cm2 |

# Performance Simulation Results




Slow $\pi$: all the VTX geometry versions perform better than the nominal Belle II




Legenda:
material in $\%X_0$ for L1&2 / L3,4,5,6:

- -- 0.1 / 0.4
- -- 0.2 / 0.4
- -- 0.3 / 0.4
- -- 0.3 / 0.6
- -- 0.3 / 0.8

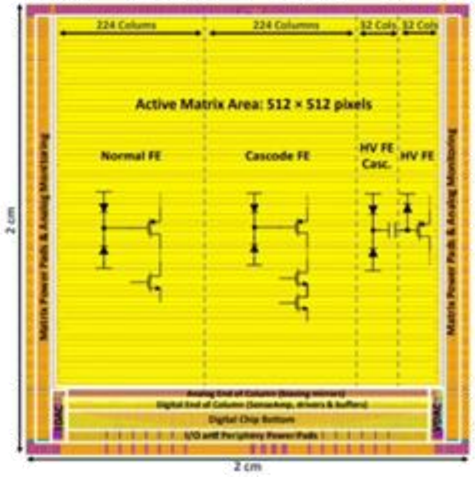
$K^0_S$:
The higher material budget on L1&2 has negligible impact on the efficiency, but worsens the B vertex resolution significantly
(though 0.3% $X_0$ is still better than nominal Belle II).

# VTX Sensors: TJMP2 & OBELIX Overview

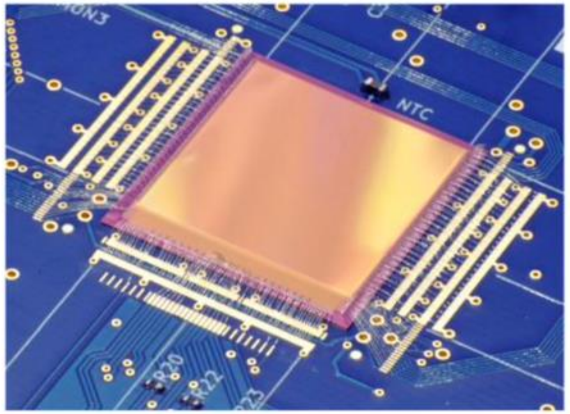
## TJ-Monopix2 (TJMP2): the OBELIX forerunner

Developed for the ATLAS ITK as a DMAPS using Tower 180 nm CMOS, modified for rad-hardness & faster readout (good at high fluence at low temps), FE derived from ALPIDE

- Pixel & Matrix Specs:
  512×512 pixels (2×2 $cm^2$), pitch 33.04×33.04 $\mu m^2$, 7-bit ToT, 3-bit threshold tuning, thicknesses ~30 μm (epi/CZ-bulk)
- Readout Architecture:
  Column-drain R/O for >120 $MHz/cm^2$, triggerless in TJMP2, 25 ns integration.
- Front-End Flavors:
  4 variants in amplifier & coupling (AC/DC) for rad environments




*Layout of TJMP2 sensor: divided in 4 regions with different FE*

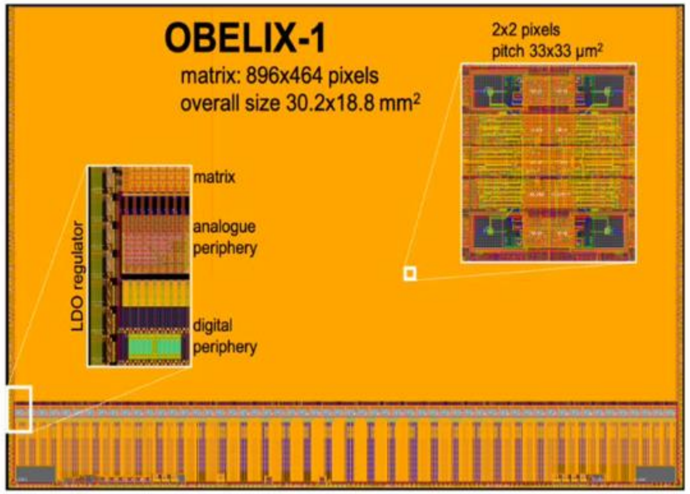



*TJM2 sensor bonded on a test board*

## OBELIX

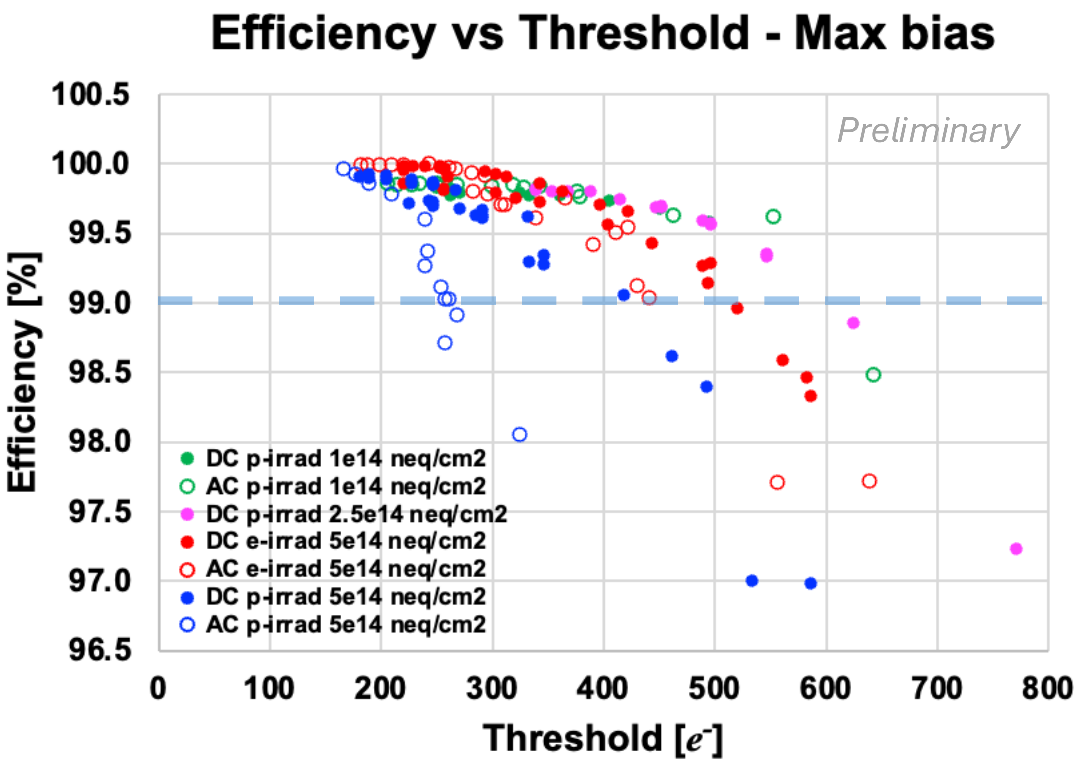
### Optimized Belle II pIXel sensor

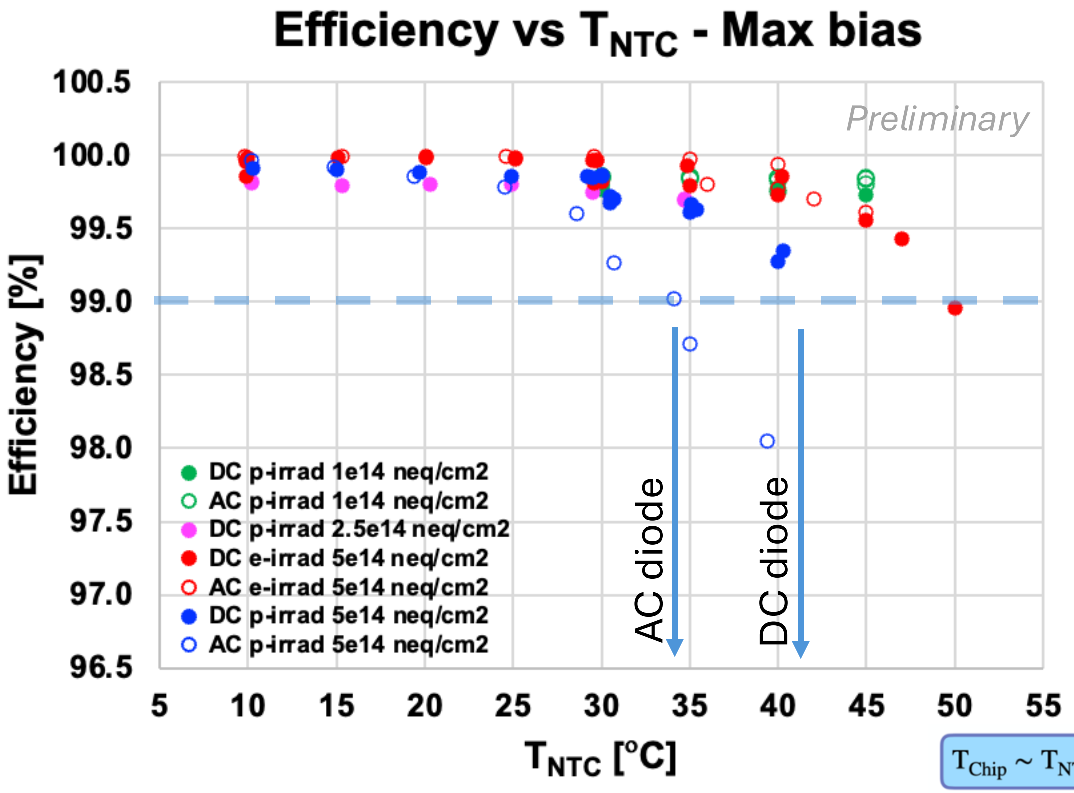
- Based on Tower Semiconductor 180 nm CMOS & TJMP2 design + new digital periphery
- Designed to stand high hit rates (120 $MHz/cm^2$) with strong radiation tolerance (TID 100 MRad, NIEL $5\times10^{14}$ $n_{eq}/cm^2$)
- High performance with <15 μm spatial resolution, <200 - 300 $mW/cm^2$ power consumption, for hit rate from few to 120 $MHz/cm^2$ and <50 ns time stamping




**First full-scale prototype (OBELIX-1)** targeted for submission in **Winter 2025**

# Efficiency on irradiated TJMP2: TB March 2025 @ DESY

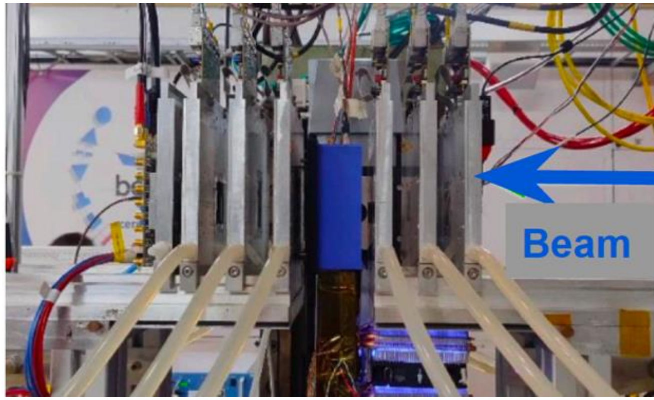



$T_{Chip} \sim T_{NTC} + 7°C$

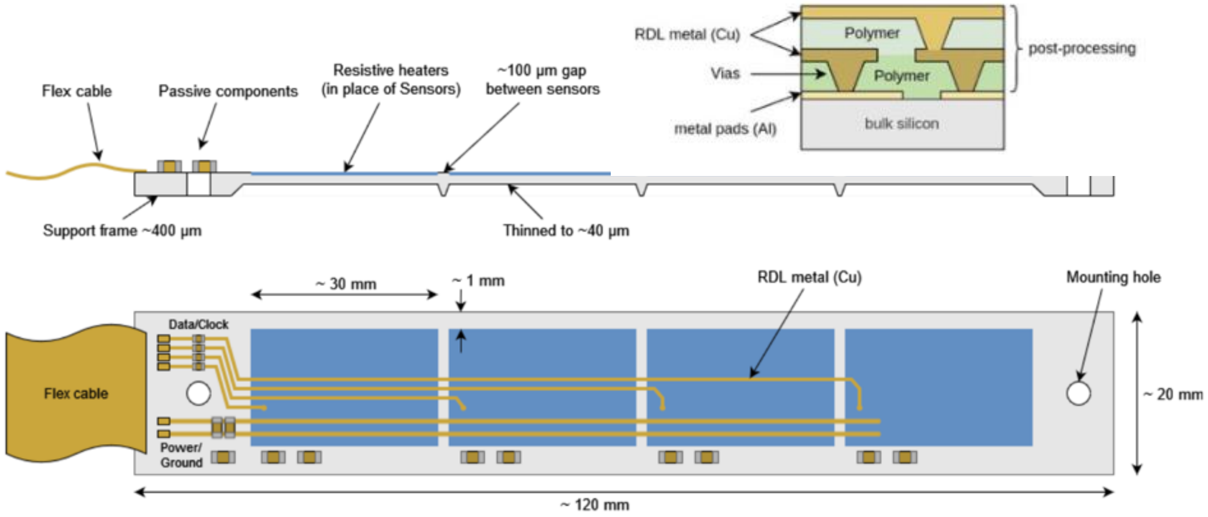
Defined the operation temperature based on 99% efficiency measured on test-beams after chip irradiation@5 x $10^{14}$ $n_{eq}/cm^2$: iVTX sensor should stay < 40 °C (less strict for oVTX)

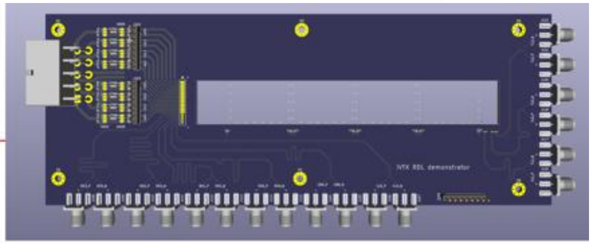
DC front-end (OBELIX1 choice for the whole matrix ) provides higher operation range than AC.

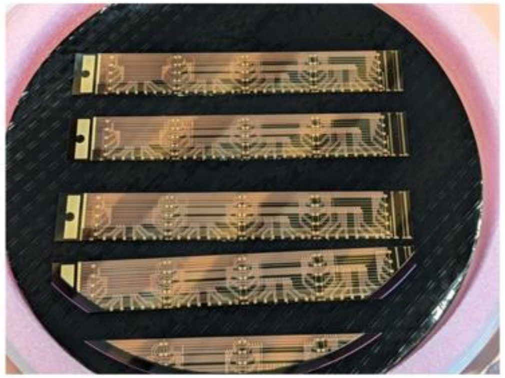


# iVTX (L1&2) Ladders

- All-silicon module 4 contiguous OBELIX sensors diced as a block from the wafer, thinned to 50 um
  - Post-process redistribution layer (RDL) for interconnection
- Prototypes:
  - First real-size ladder at IZM-Berlin with dummy Si & resistive heater to test cooling too





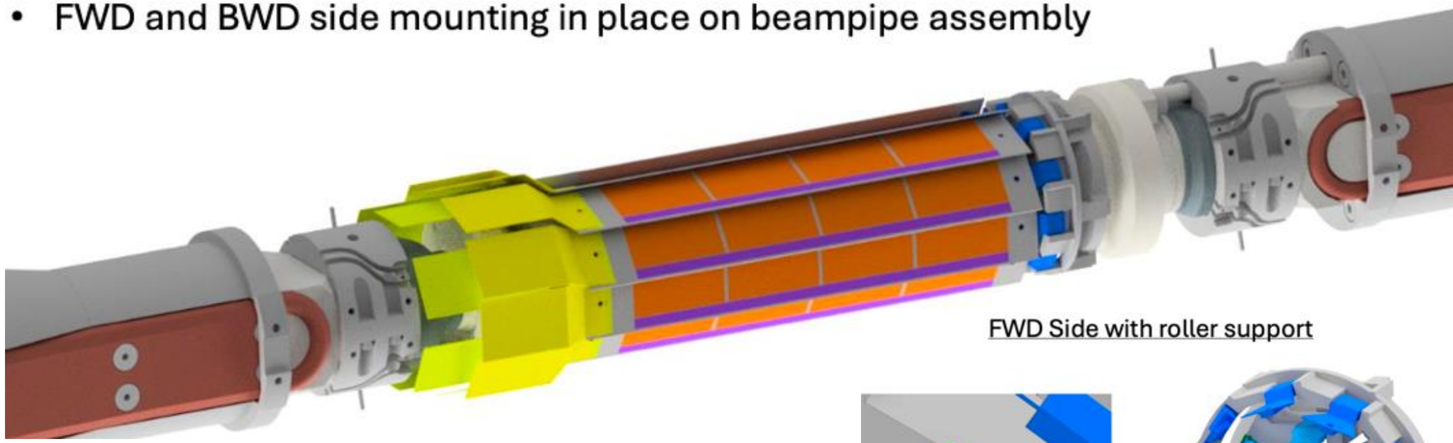
Multi-reticle ladder
Size: 12x2 cm² (4x chips interconnected)

Full front and backside processing
Impedance, continuity of the RDL, integrity data lines
Selective etching

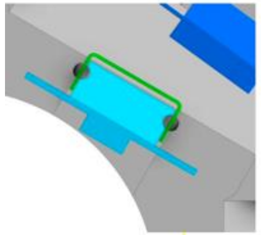


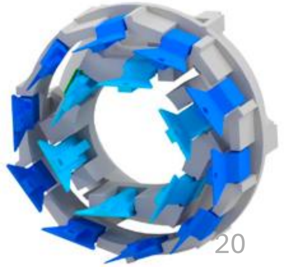
## Modelling progressing on iVTX mechanics

- Ladder re-modelled with active region / periphery shown
- FWD and BWD side mounting in place on beampipe assembly



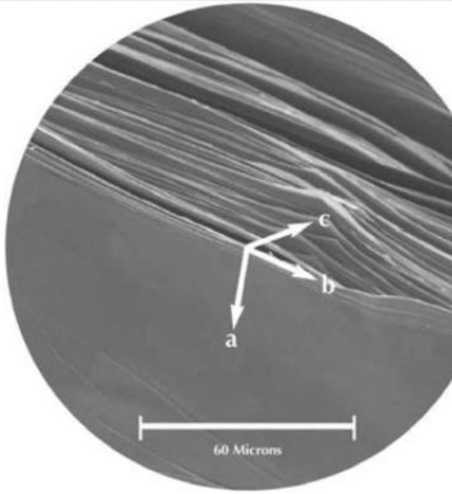
FWD Side with roller support





**To be updated to the new I.R. geometry**

# iVTX Cooling by Thermal Contact




(This solution already adopted in the MVD of the CBM experiment)

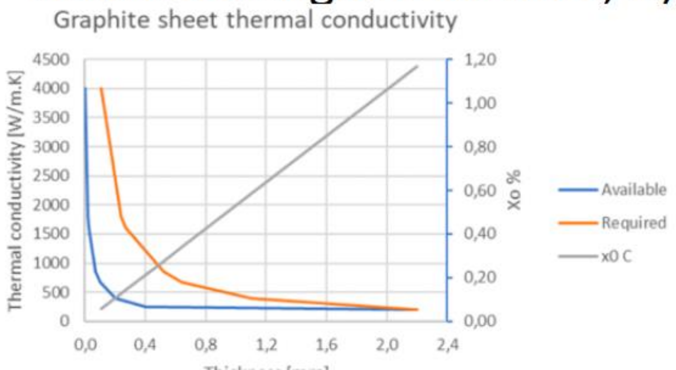
- Thermal Pyrolytic Graphite (TPG): high crystalline graphite manufactured from thermal decomposition of hydrocarbon gas at an extremely high temp.
- iVTX ladder supported by a TPG plate, acting as:
  - Thermal heat sink

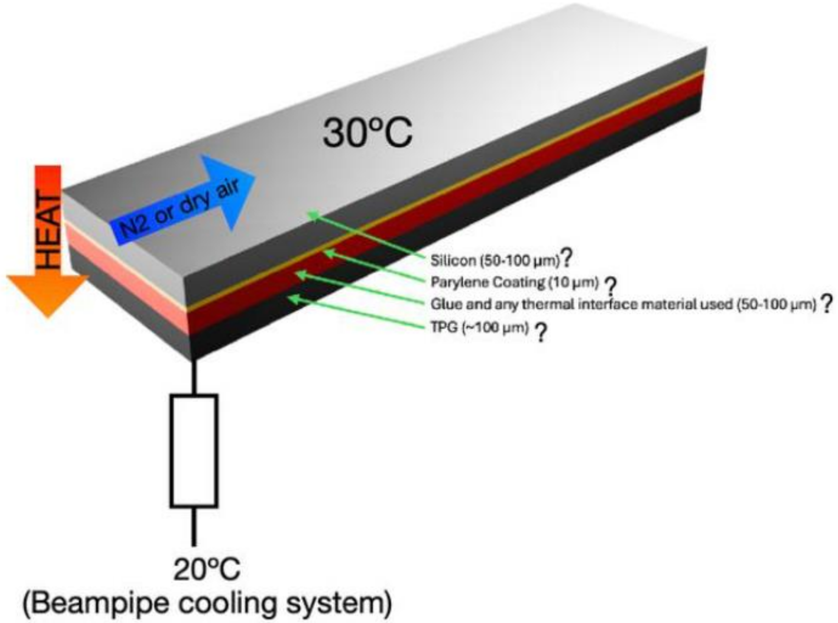
    the high alignment of the graphene layers causes superior thermal conductivity which makes it an excellent thermal management material with thermal conductivity around 1500W/(m K) for 380 um thickness

    (i.e. 4x higher thermal conductivity than Cu
    but with 1/4 of copper's weight
  - Mechanical stiffener

    TPG Young's modulus 20 GPa, 1/4 of Al

    tensile strength is 80 MPa, 1/5 of Al



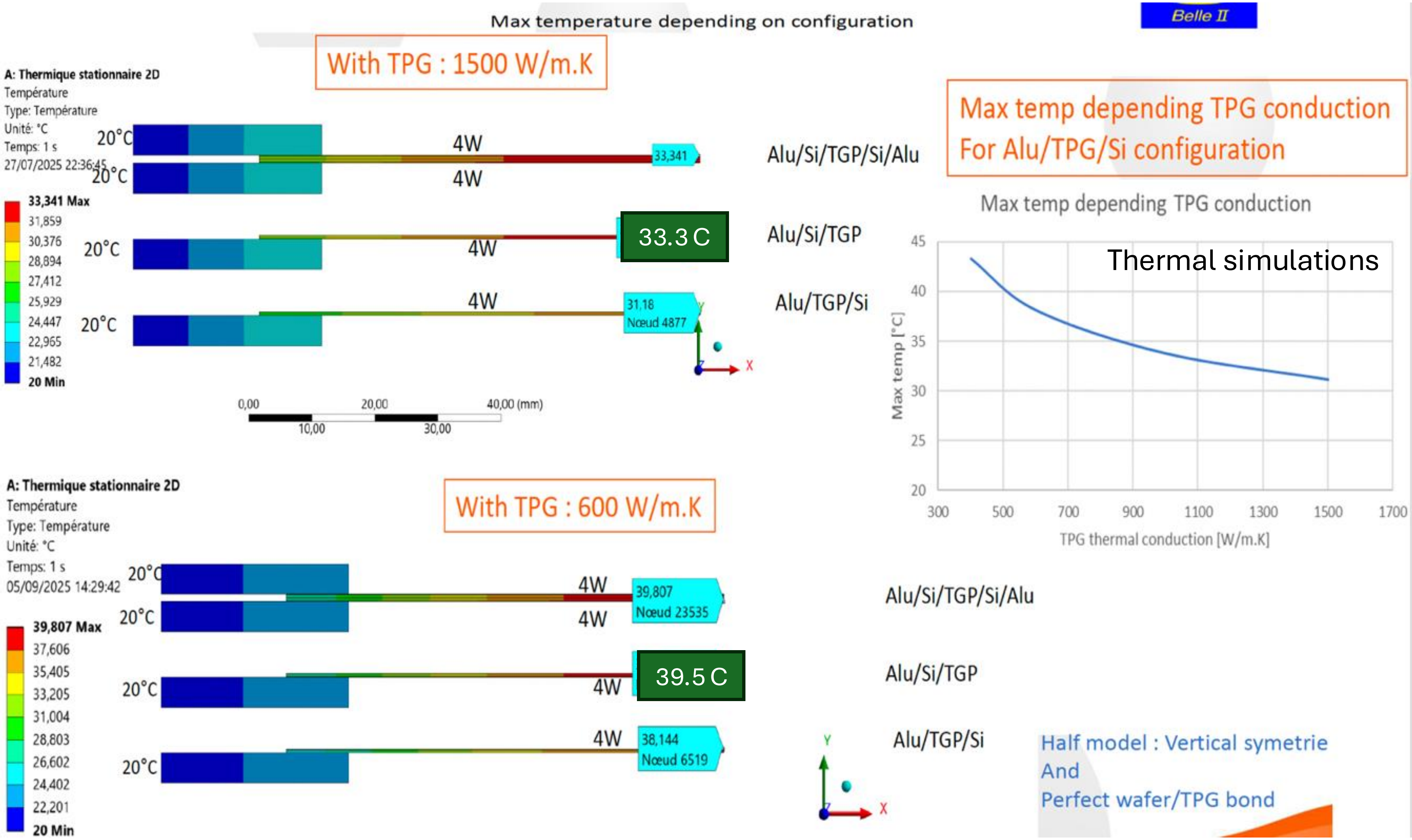

iVTX prototype ladder
(under construction)

# iVTX ladder developments

iVTX: Two Ladder cooling solutions → critical study now

Thermal simulations: we are below 40 C even with the lowest TPG conductivity.

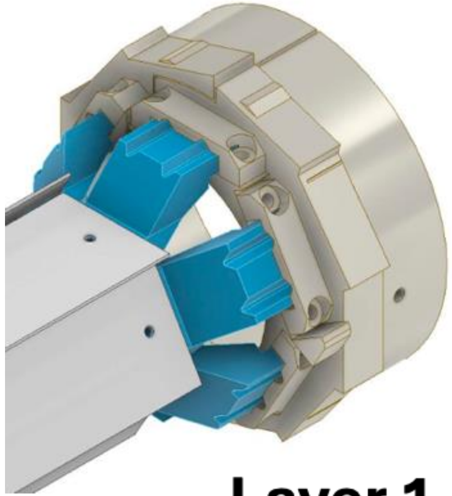
- **Plan A:**
**Solid thermal conductor (TPG)**
-easier for mechanics but still many question (gluing, coating, …)
-requires water cooling at the end-piece
-low radiation impact on heat conductivity, according to ATLAS SCT experience(*)
-first iVTX TPG prototype ladders expected in December



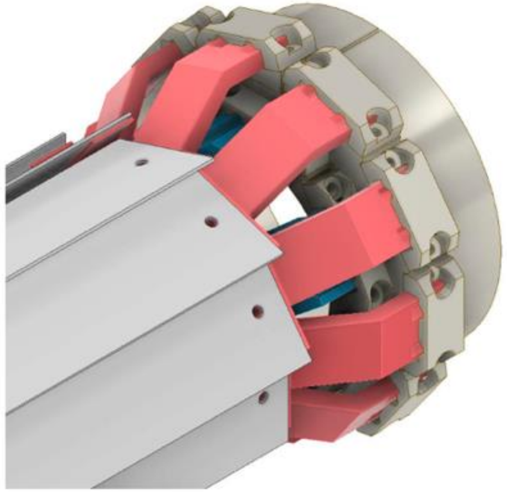

(*): Measurement of the thermal conductivity of PG substrates for use in SCT modules (by G.A. Beck et al.)

- **Plan B:**
**Al water tubes**
-relatively more complex
-greater material budget

# Solution for iVTX with TPG heatsink cooling FWD side



Layer 1

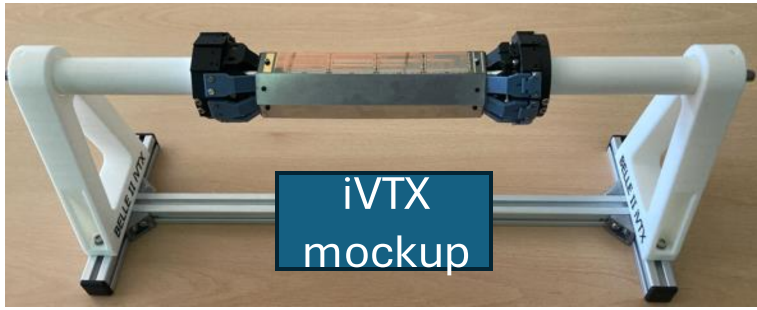


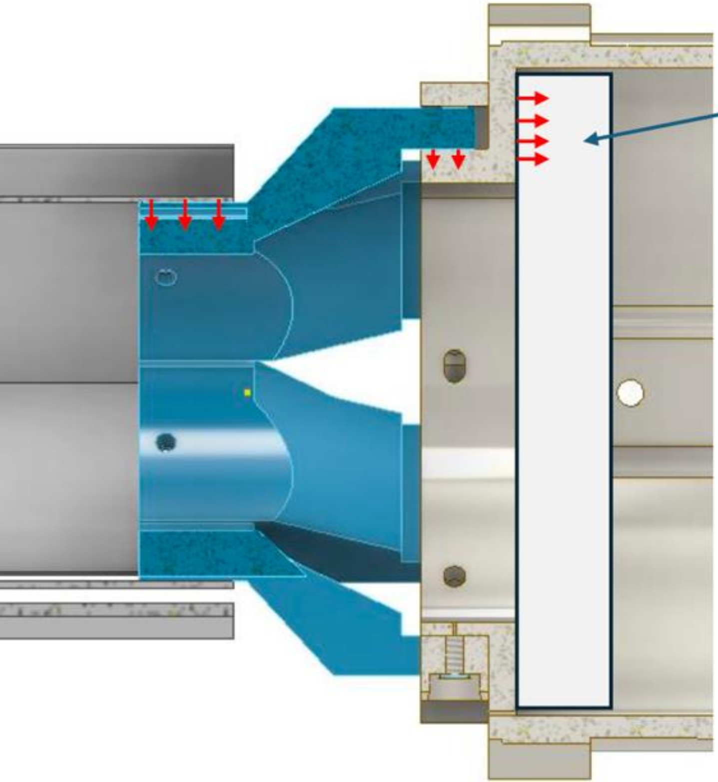
Layer 2

**Structures FWD Side:**
1. Ladder Support Arm
2. Linear Guide
3. FWD Support Flange

**Structures BWD Side:**
1. Ladder Support Arm
2. BWD Support Flange

**Assumes paraffin manifold provides the cooling; if not, we need to add an additional cooling block or manifold to this list on both sides**

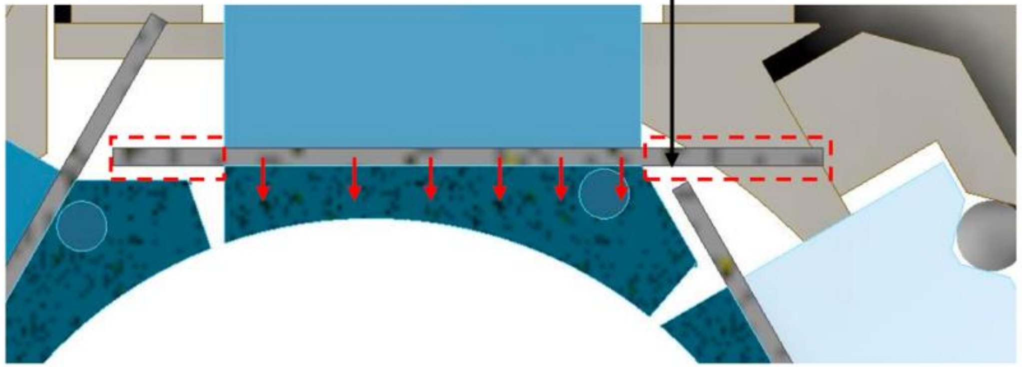


Paraffin manifold

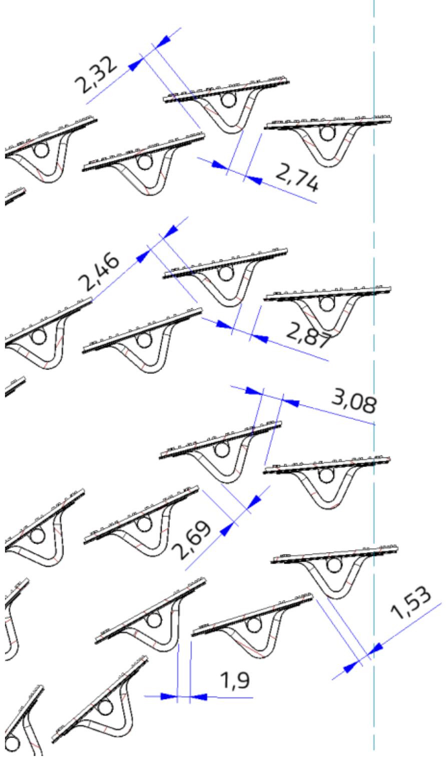
Red arrows show thermal pathway via conduction

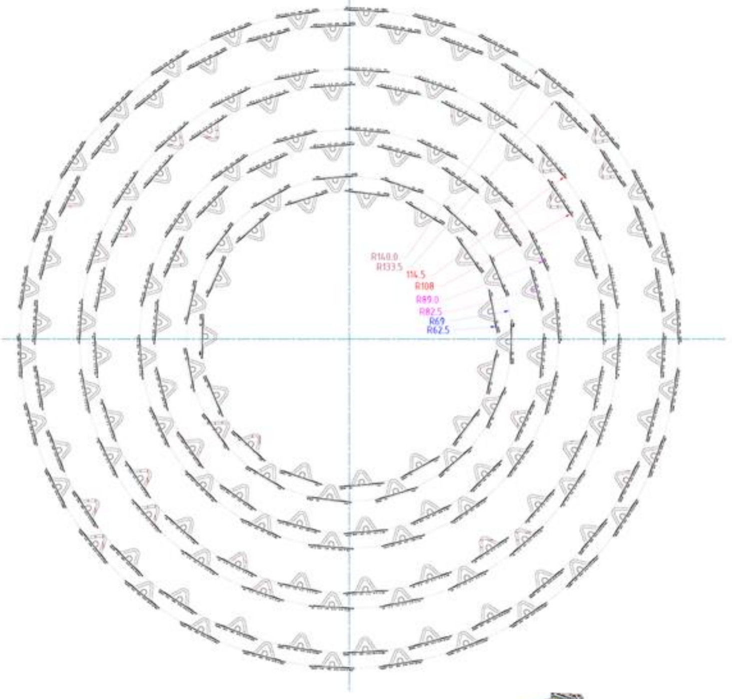
Note it is unlikely that the support will be able to cover the entire width of ladder

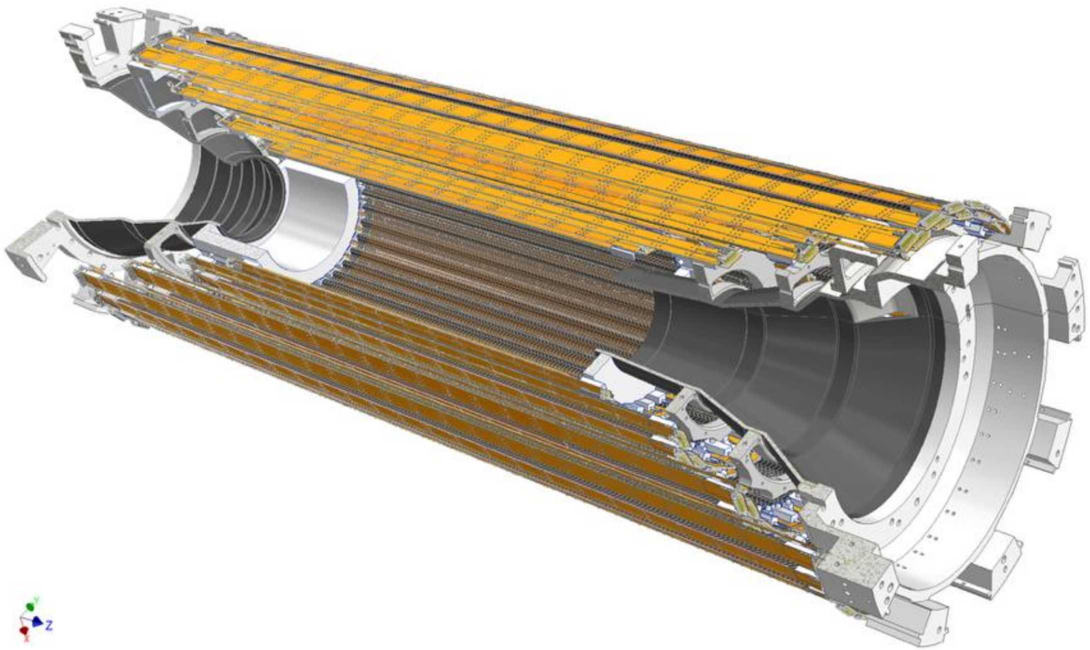


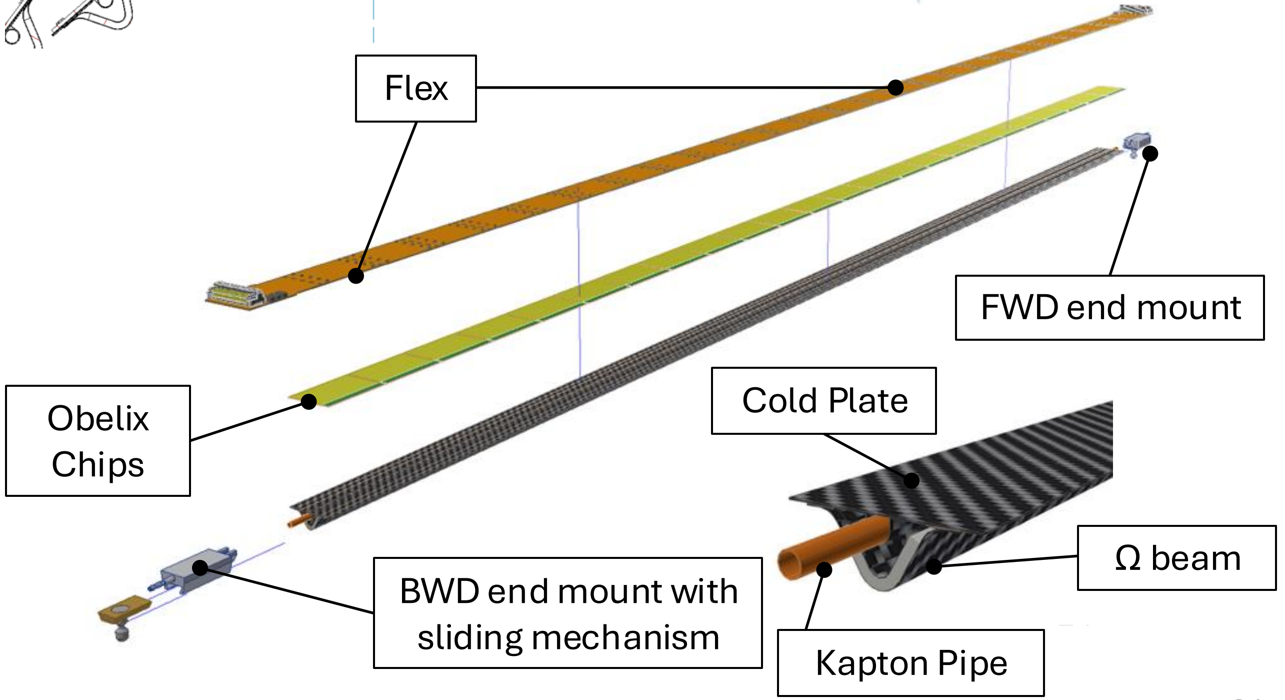
# oVTX

- Ladder structure (ALICE ITS2-inspired):
  - CF support structure (Ω beam), cold-plate with 1 pipe and liquid cooling
  - Chip and Flex circuit for power & signal
- Prototypes:
  - Mechanical & thermal characterization done for the longer ladder ~70 cm (outermost layer)
- Mechanical design & prototypes already advanced

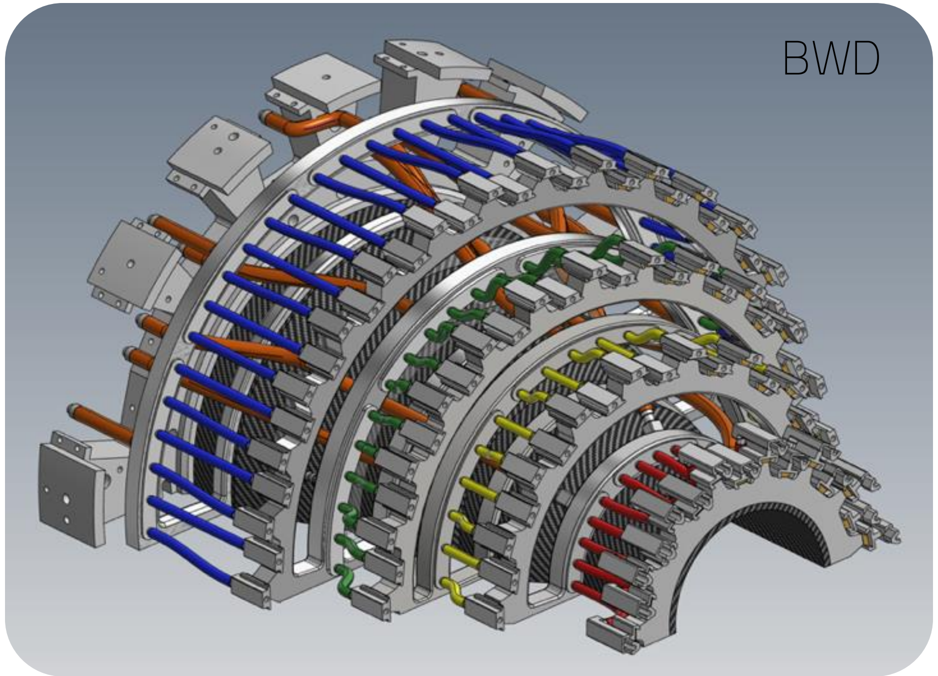


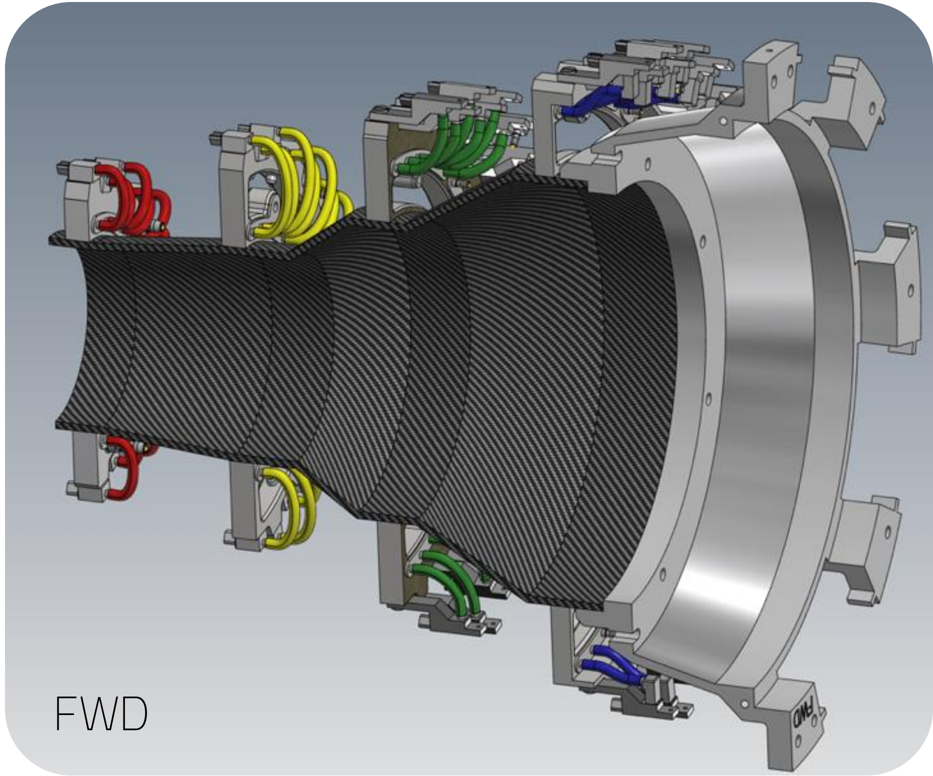







# Design of the hydraulic services (in the old I.R.: to be re-done for the new QCS)



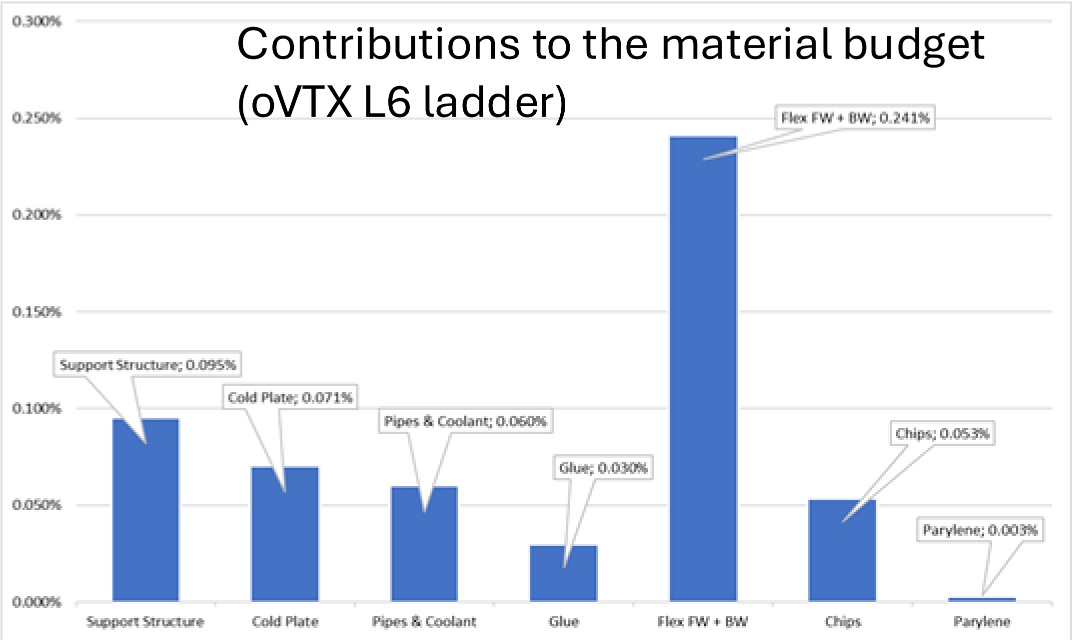

- *All the manifolds (except for Layer 6) integrated into the end rings.*
- *The scheme: Layer "X" with manifold on the Layer "X+1" end ring.*
- *The pipes are grouped into manifolds (sets of 5 for the L3, of 6 for the other layers).*
- *The end rings are hollow to allow space for cables routing.*

| Legenda: | |
|---|---|
| (blue) | L6 - ladders to manifolds |
| (green) | L5 - ladders to manifolds |
| (yellow) | L4 - ladders to manifolds |
| (red) | L3 - ladders to manifolds |

| | |
|---|---|
| (brown) | Manifold Inlet (or Outlet) |

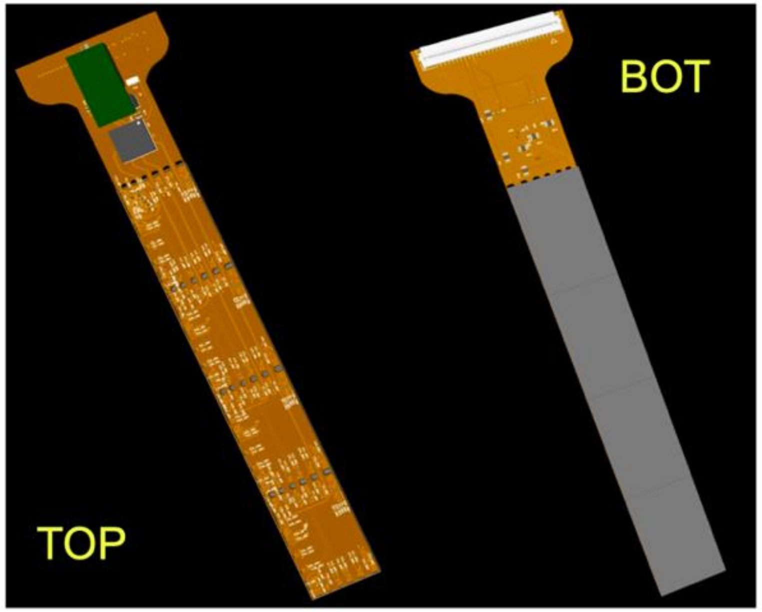
- *Working to find a solution w/o modifying the FWD end flange*
- *Each layer has the manifold located on its own end ring, preventing the piping and flex cables from crossing*
- *A mock-up is needed to evaluate the tube's flexibility and its minimum bending radius.*

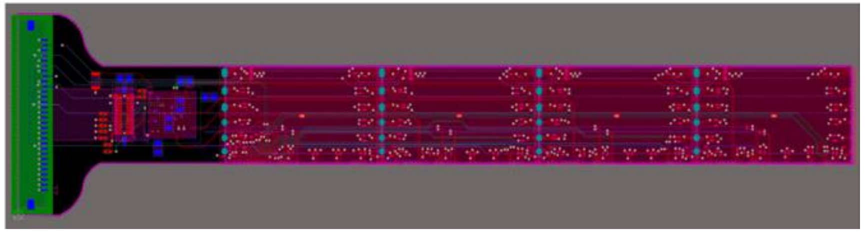
# Al Flex for minimal material budget



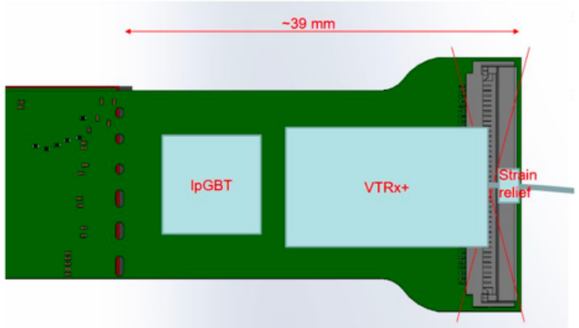

## lpGBT/VTRX+ integration

Design of the
Dummy Al-Flex



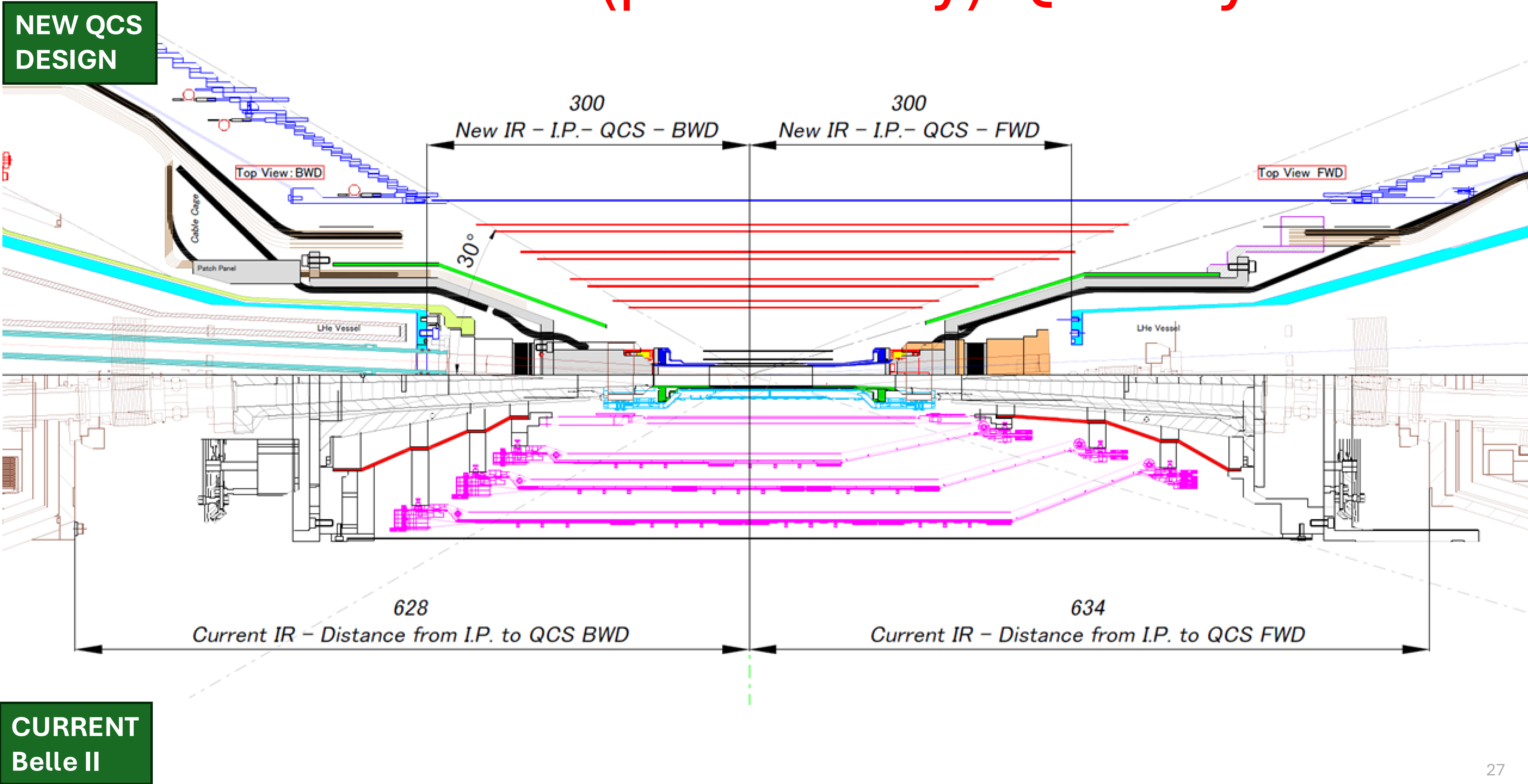



- Remove data connector (top side)
- Integration of the lpGBT/VTRX+ on the top layer
- Keep bottom connector for: chip power supply and bias voltage, VTRX+/lpGBT power supply
- Replace 40-pin connector with Molex FD19 – 30 pin – 1mm pitch
- Flex head widened to ≈ 39 mm
- Simplified flex with 4 chips (1 master - 3 slaves)
- 6 layer stack-up, compliant with CERN fabrication requirements



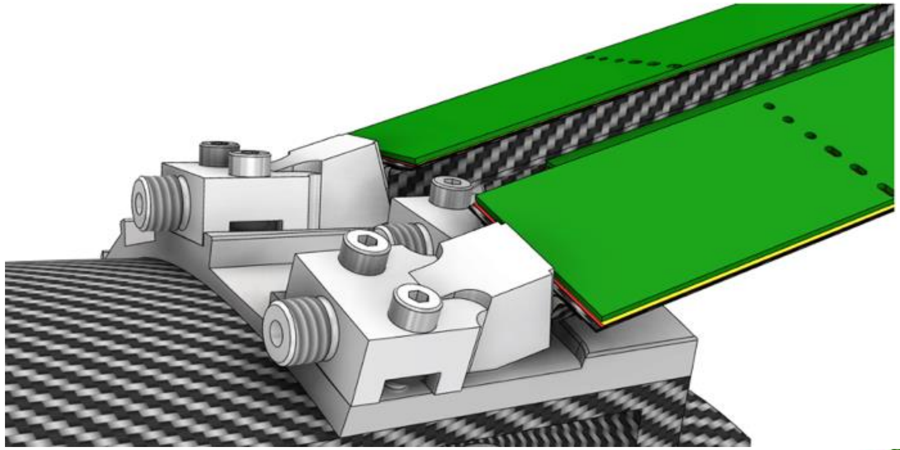

Design to be adapted to the new OBELIX-1 gds file (already validated by CERN!)

# The old vs NEW (preliminary) QCS layout

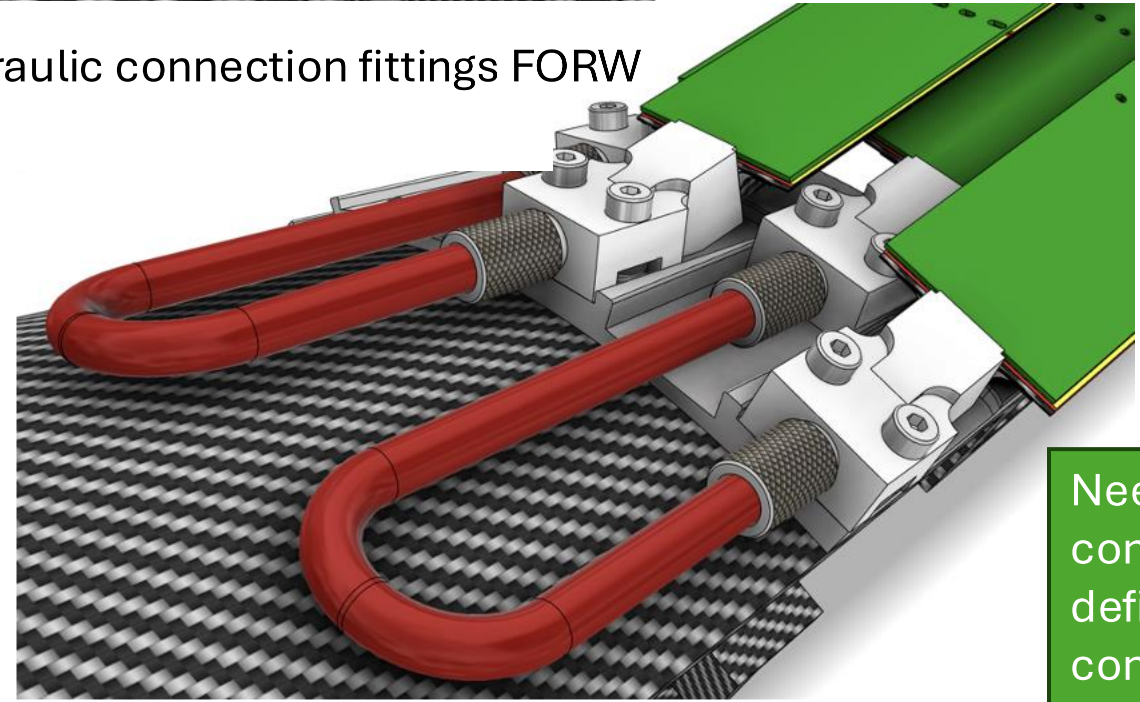


# Specific issues under study (waiting for the new/conservative QCS design)

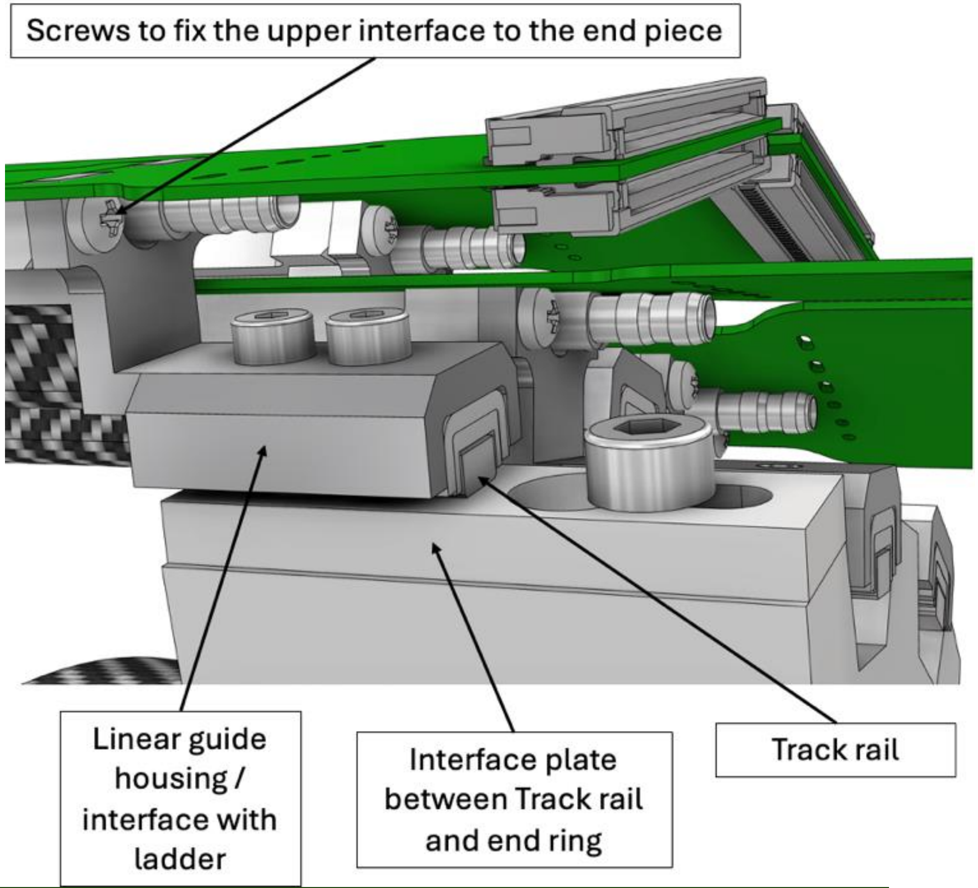
L3A and L3B FWD Side Clamping



Hydraulic connection fittings FORW



Sliding mechanism (BACKW)

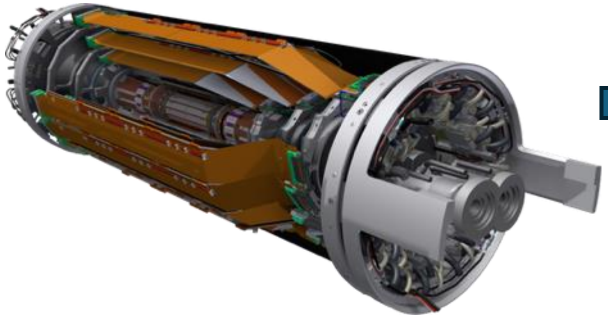


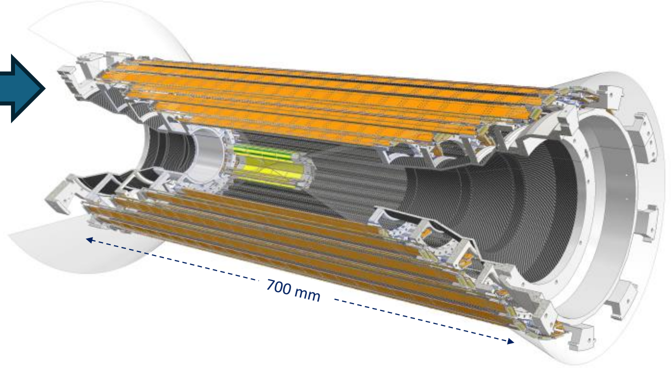

Needed engineering developments to translate conceptual ideas into a CAD model and prototypes, by defining the (hydraulic/electrical) services in the new constrained space, still ensuring that the old/tested ladder-mount procedures work.

# Conclusions

- After months of preparation (Vacseal cleaning, new RF gun, …) SUPERKEKB is going to restart collisions in November. Belle II will restart data taking with SVD efficient as ever and PXD OFF, waiting for stable beam conditions, i.e. hopefully w/o observing SBL any longer, in case implementing enhanced fast-shutdown systems to safeguard the PXD.
- The plan (A) is to collect up to 1 $ab^{-1}$ in 2026ab runs reaching $10^{35}$ $cm^{-2}$ $s^{-1}$ of inst. luminosity.
  Such achievements are the crucial steps for the final goal of the project!

- To reach the target luminosity 6 $10^{35}$ $cm^{-2}$ $s^{-1}$ and 50 $ab^{-1}$ by 2042 a major redesign of the I.R. is needed.
- The mechanical design of the new vertex detector depends critically on the confirmed position and design of the QCS and other constraints from the machine around the interaction point.
- The Obelix chip is going to be submitted to foundry.
- Continue R&D and engineering activities on VTX ladder prototypes.
- Needed MEXT Review (under discussion)
- Path for the Belle II upgrade to LS2 (2032):






Define upgrade *baseline* → BPAC/ARC review

Finalize *baseline* upgrade configuration

TDR review

LS2

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 2025 | 2026 | 2027 | 2028 | 2029 | 2030 | 2031 | 2032 | 2033 |

Prepare TDR

Construction

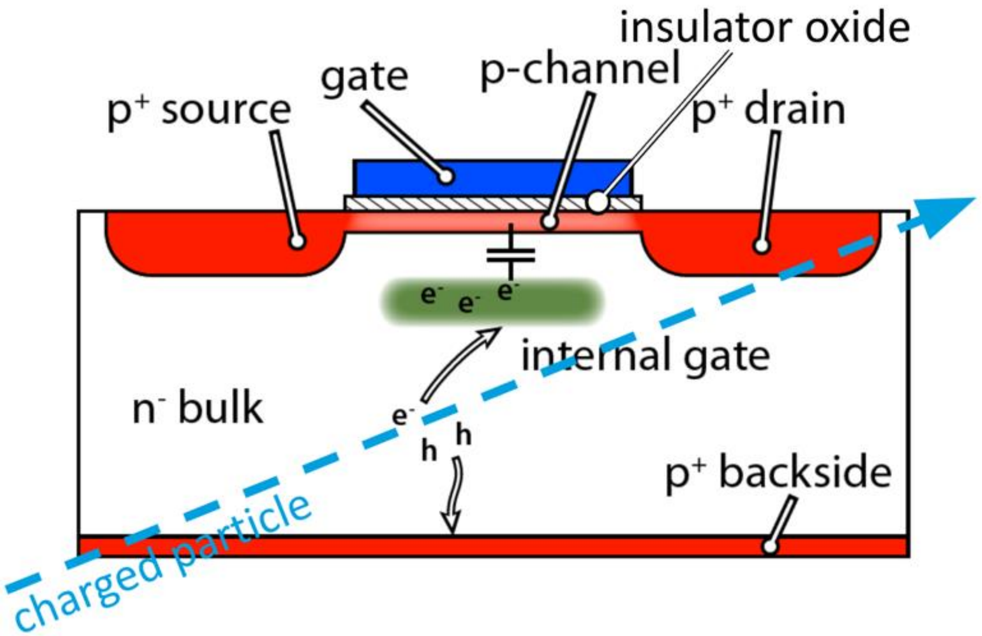
Installation

# BACK UP SLIDES

# DEPFET sensor principle

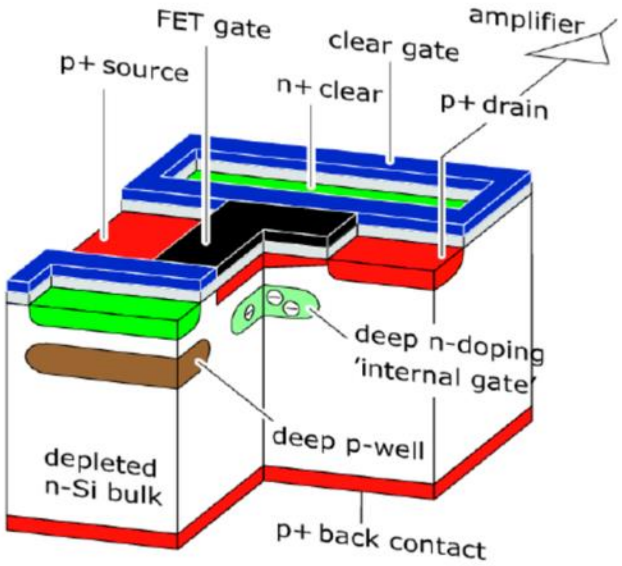
### How it works

- A Field Effect Transistor (FET) is built directly into a fully depleted silicon bulk.
- The internal gate (a deep n-implant beneath the channel) collects signal electrons, which in turn modify the source–drain current.
- After readout, the stored charge is removed through an n+ implant using a punch-through reset mechanism.




### Why it's Important

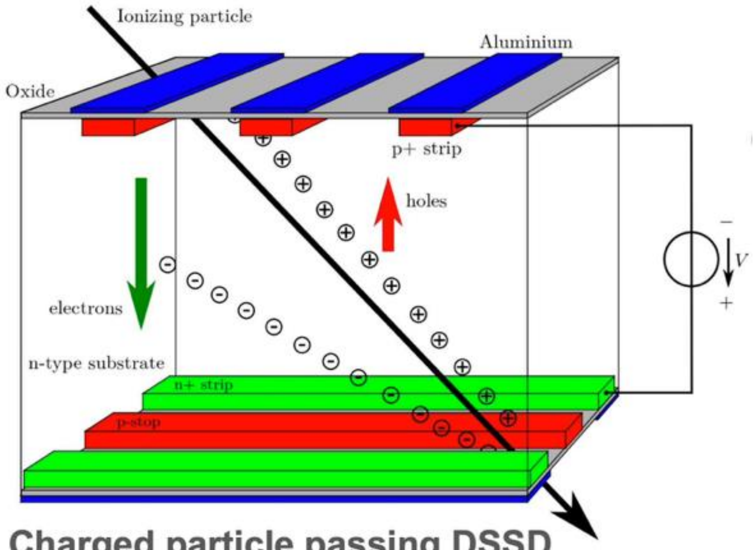
- Fast response
  - charges are collected within nanoseconds
- ensuring excellent signal-to-noise performance
- Low power and low mass
  - with only ~75 μm active thickness, the sensor adds minimal material to the tracker
- Non-destructive readout



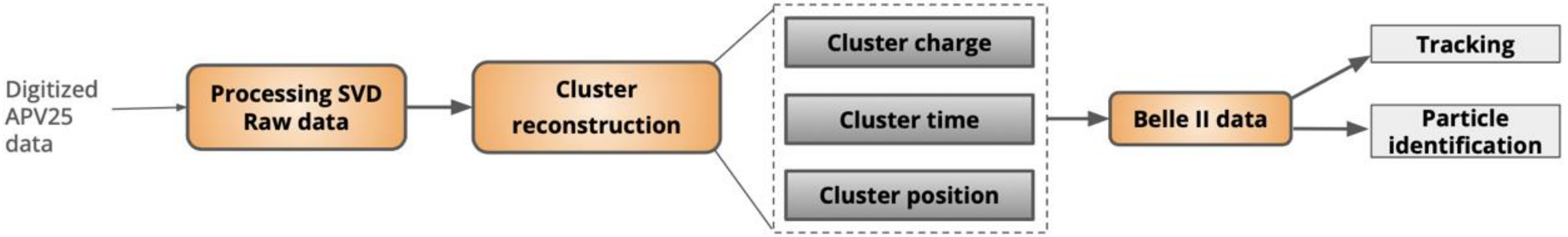
# SVD Data Reconstruction

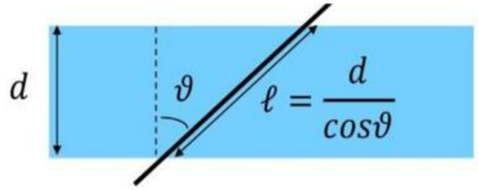
Charged particles passing through fully depleted sensors creates e-h pairs, which produces hits in the strips

- **Cluster**: Collection of strips with signal-to-noise ratio (SNR) above certain threshold
- A cluster has
  - **Charge**: Sum of the charges of each strip belonging to the cluster, depends on incident angle of the particle
  - **Time**: Charge-weighted average of strip times relative to trigger
  - **Position**: reconstructed from strip charges
  - **Noise**: Quadrature sum of noise of each strips




Charged particle passing DSSD




d ≡ 300 - 320 μm

# SVD Towards Future High Luminosity

(alghoritms to maintain high performance)

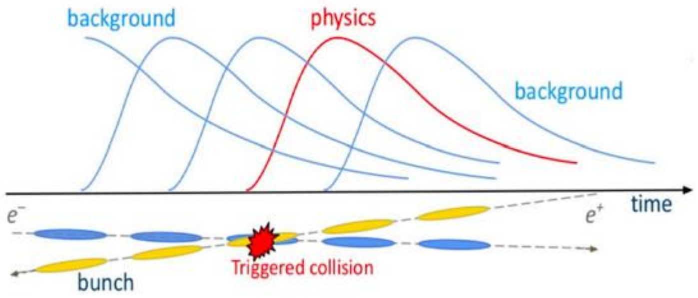
### Hit time selection

PoS ICHEP2024 (2025) 855

Excellent SVD hit-time performance: resolution < 3 ns for signals, while time range of beam-induced background is around 100 ns

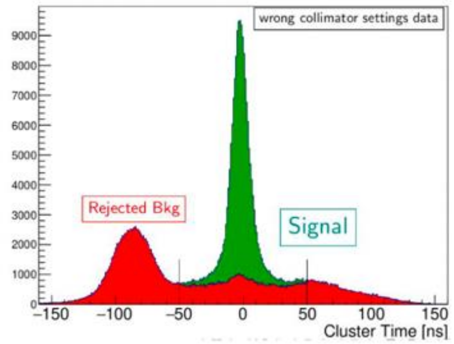
- ❑ Efficient to remove 50% off-time hit background, keeping signal efficiency above 99%
- ❑ Background rejection based on SVD hit-time selections already tested but not yet deployed on real data reconstruction

*SVD occupancy limit for Layer 3 can be set at 4.7%*




$|t_{hit}| < 50$ ns

$|t^{p}_{hit} - t^{n}_{hit}| < 20$ ns

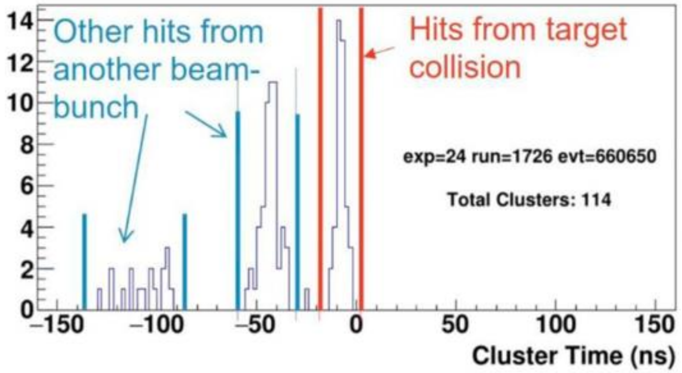



### Cluster grouping

PoS ICHEP2024 (2025) 855

*Grouping the clusters on event by event basis using the cluster times*

- ❑ Selection based on Grouping further reduces the fake rate by 15% on high-background data

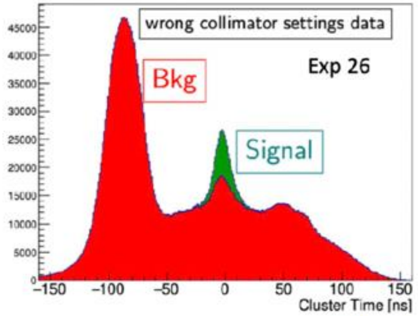



### Track time

*Average time of clusters belonging to the outgoing arm of the track, relative to time of collision*

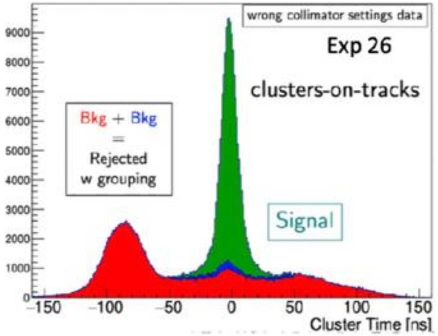
- ❑ Remove off-time track, further reducing fake rate by a factor 1.5 for the high background scenario

SVD hit time: all clusters




Cluster grouping

SVD hit time: cluster on track



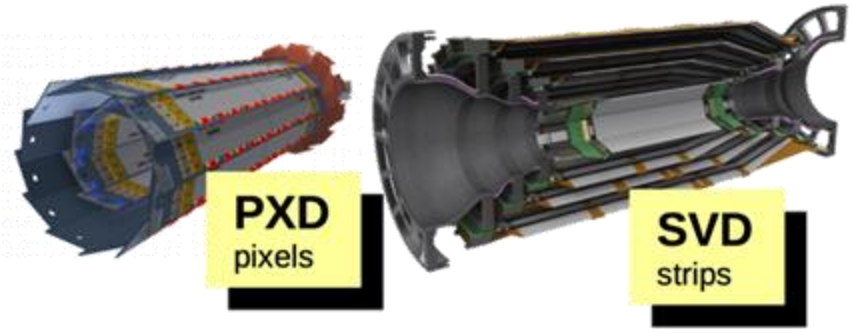

Not implemented yet

Further increase SVD occupancy limit for Layer 3 from 4.7% to 6%

# Vertex Detector Alignment

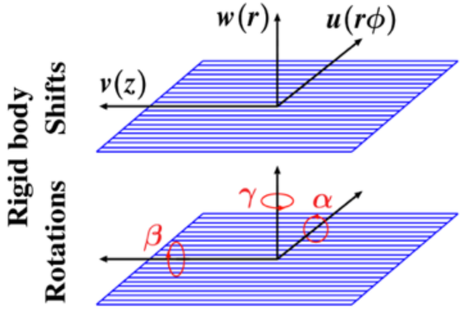
## What is detector alignment?

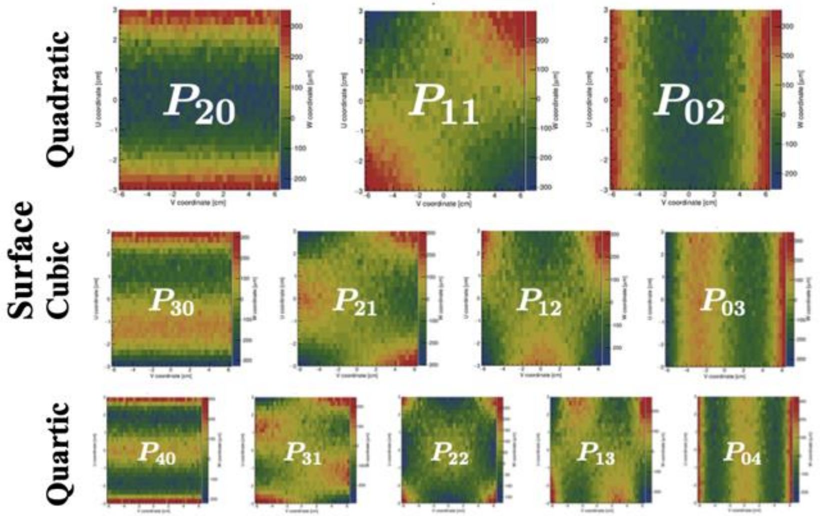
- Calibration of the true spatial positions and orientations of detector sensors (PXD, SVD)
- Track reconstruction is matched with actual hit measurements using global track-based fits
- Minimizes track-to-hit residuals across thousands of events




## What do we align?

- VXD includes: 2 PXD half-shells, 4 SVD layers (~ 65 ladders)
- Each has 6 rigid-body DOFs (translations and rotations)
- Includes surface parameters (Legendre polynomials up to 4th order)
- In total >4000 parameters are solved using Millepede II

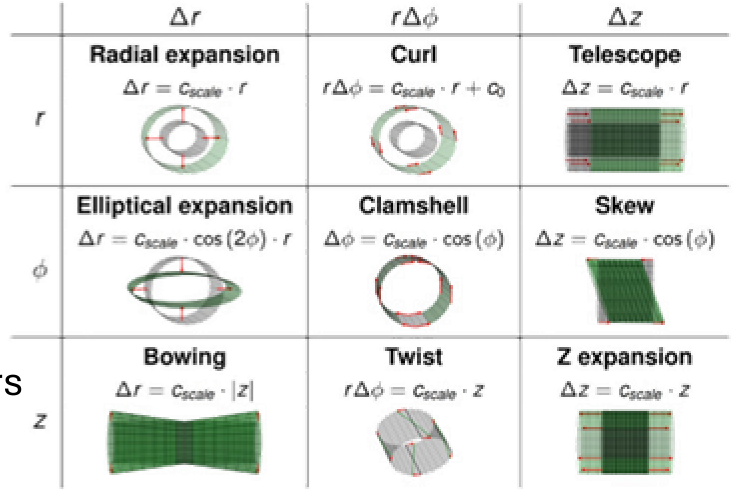



## Why is alignment needed?

- Unaligned detectors show up to hundreds of μm shifts
  - Essential for maintaining vertex and tracking resolution required for Belle II physics
- Detector positions change due to vibrations, temperature fluctuations, and mechanical shifts

# Alignment Monitoring and Results




## Challenges

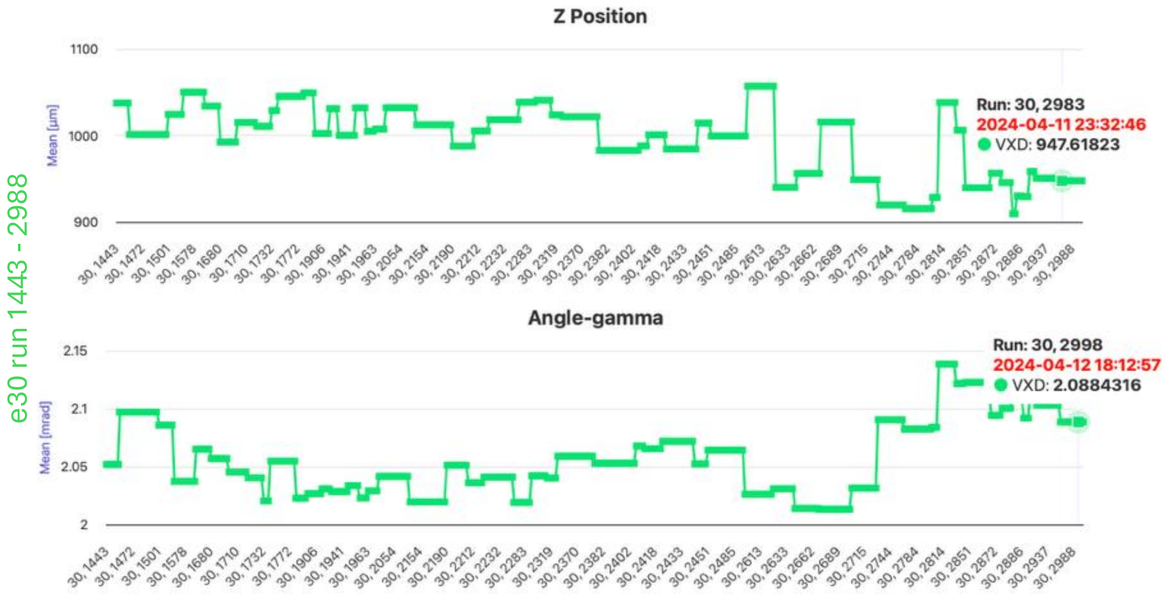
- Misalignments
- Weak Modes
- Deformations

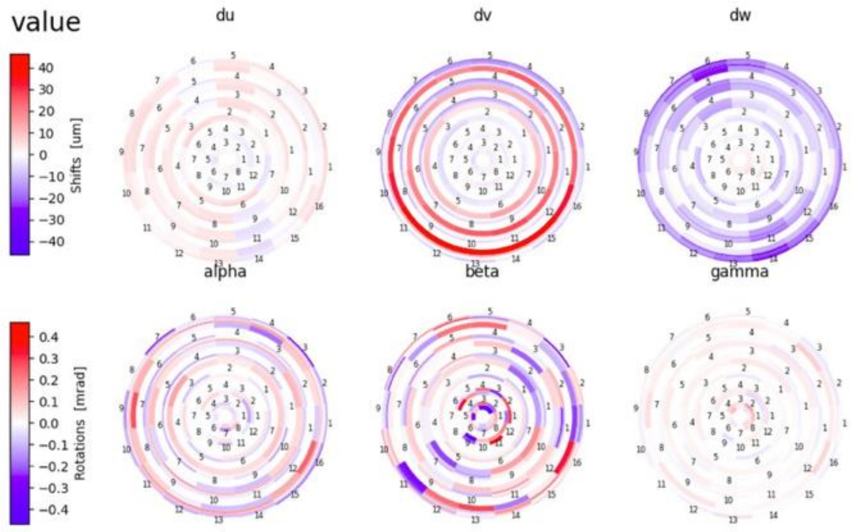
## Track-based alignment method

- Performed using Millepede II and GBL track model
- Simultaneous global fit of rigid-body DOFs, surface shapes, and time-dependent parameters

## Alignment data

- Cosmic-ray muons with B-field off/on
- Collision events: dimuons, hadronic events

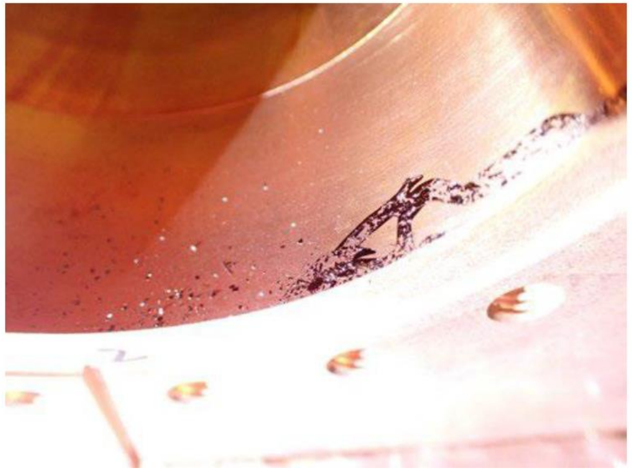


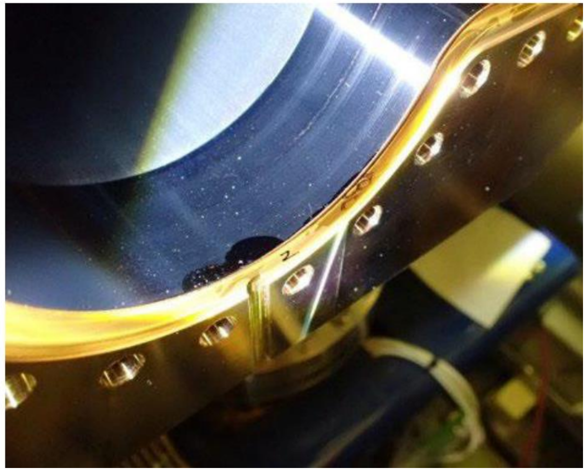



# Vacseal Cleaning

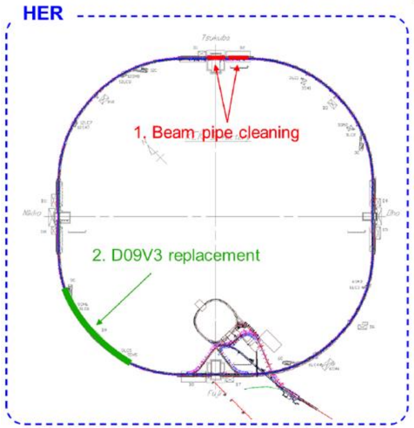
## Beam pipe cleaning

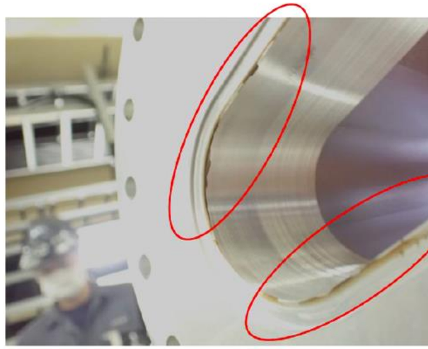
- Internal inspections have been completed, where
  - All MO-type flange connections where VACSEAL was likely used.
  - IR (HER, LER), LER wiggler sections (D04, D10, D11), others
    - Black stains were found on many flange connections and removed.





- During D9V3 collimator replacement work
  - Black stains were found on HELICOFLEX flange connections.
    - VACSEAL had been used.
    - This is the first time such stains have been found on HELICOFLEX flange.
- Three HELICOFLEX flange connections will be inspected before operation.

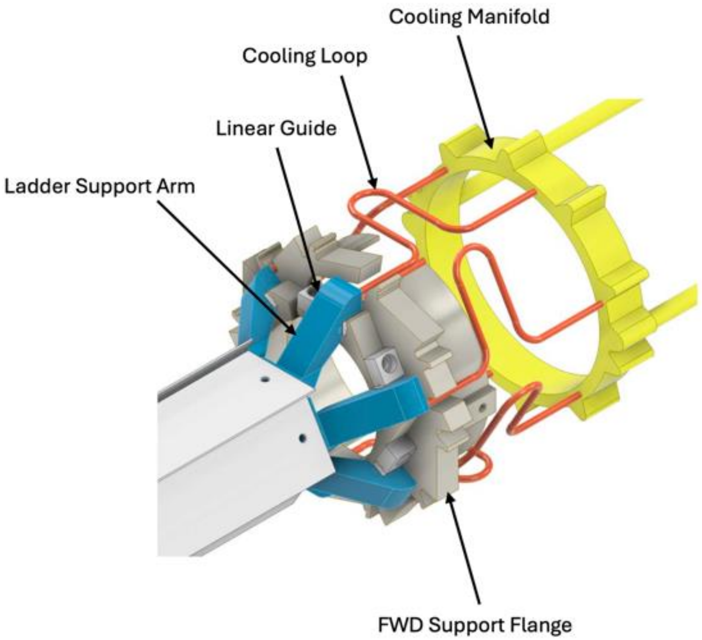


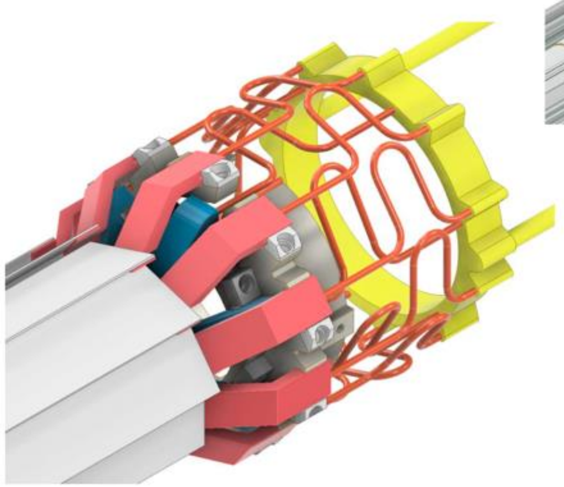
After removing the vacseal we observed decreasing the SBL happening from the cleaned area.

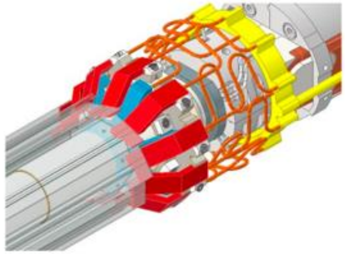
# Solution for iVTX with cooling pipes FWD side

Layer 1




Layer 2

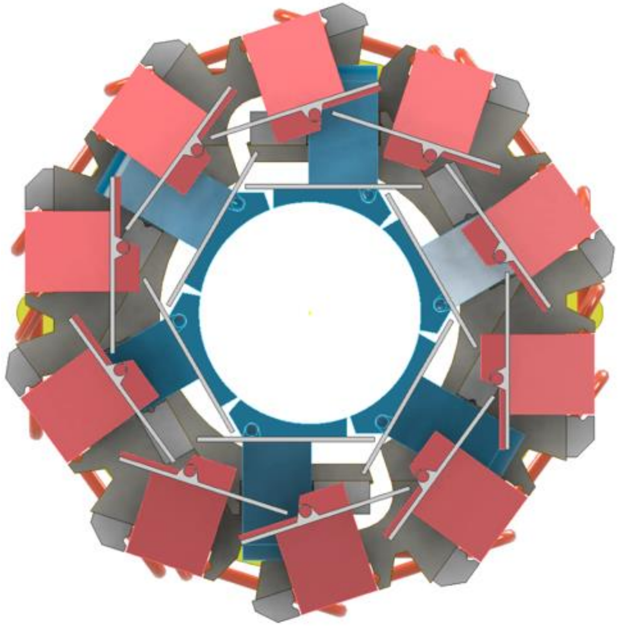




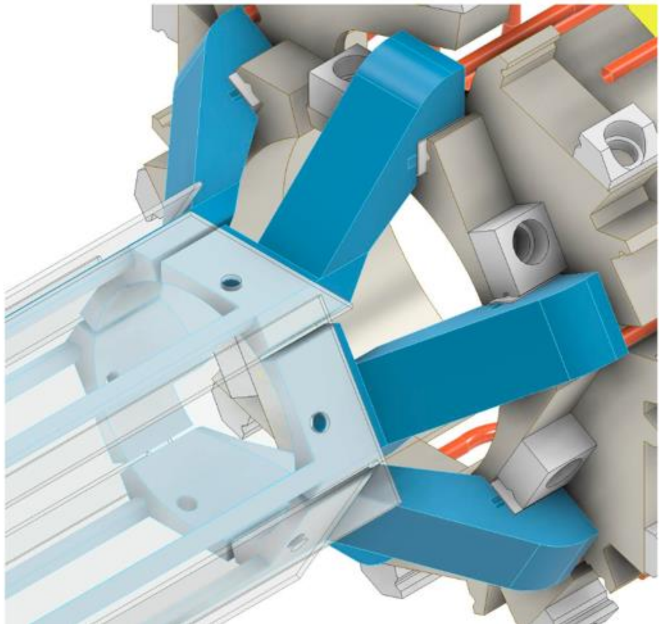
**Structures FWD Side:**
1. Ladder Support Arm
2. Linear Guide
3. FWD Support Flange
4. FWD Cooling Loop
5. FWD Cooling Manifold

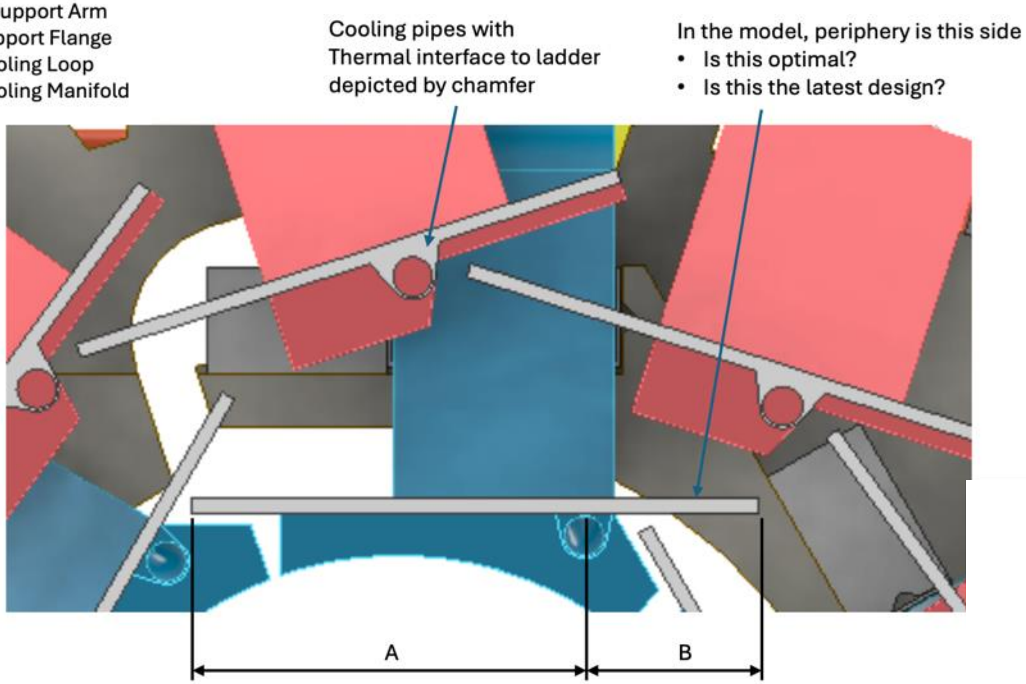
**Structures BWD Side:**
1. Ladder Support Arm
2. BWD Support Flange
3. BWD Cooling Loop
4. BWD Cooling Manifold

View on FWD Side



Layer 1 only shown






Consider thermal performance with pipe in this position and how it changes when modifying A & B

# VTX Collaboration

## VTX collaboration

| | | | |
|---|---|---|---|
| *IGFAE, Santiago* | *Jilin University* | *IJCLab, Orsay* | *IPHC, Strasbourg* |
| *University of Bergamo* | *KIT, Karlsruhe* | *RAL, Oxford* | *University of Tokyo* |
| *University of Bonn* | *IPMU, Kashiwa* | *INFN & University of Pavia* | *KEK, Tsukuba* |
| *University of Dortmund* | *Queen Mary University of London* | *INFN & University of Pisa* | *IFIC (CSIC-UV), Valencia* |
| *University of Göttingen* | *CPPM, Marseille* | *IFCA (CSIC-UC), Santander* | *HEPHY, Vienna* |