Expression of Interest for a lightweight vertex detector for FCC-ee

Involved Laboratories:
Italy: INFN - Genova, Frascati, Milano, Padova, Perugia, Pisa, Torino, Trieste-Udine
Switzerland: ETH Zurich, Paul Scherrer Institute, University of Zurich
United States of America: Brown University, BNL, FNAL, LBNL, MIT, SLAC, Stony Brook University

Contact persons:

Fabrizio Palla*[1], Attilio Andreazza[2], Nicola Bacchetta[3,9], Manuel Rolo[4], Florencia Canelli[5], Armin Ilg[5], Anna Macchiolo[5], Malte Backhaus[6], Rainer Wallny[6], Lea Caminada[7], Grzegorz W. Deptuch[8], Loukas Gouskos[9], Artur Apresyan[10], Carl Haber[11], Christoph Paus[12], Caterina Vernieri[13], Valerio Dao[14], and Giacinto Piaquadio[14]

[1]INFN Pisa and University of Pisa, Italy
[2]INFN Milan and University of Milan, Italy
[3]INFN Padova and University of Padova, Italy
[4]INFN Torino and University of Torino, Italy
[5]University of Zurich, Switzerland
[6]ETH Zurich, Switzerland
[7]Paul Scherrer Institute, Switzerland
[8]Brookhaven National Laboratory, USA
[9]Brown University, USA
[10]Fermi National Laboratory, USA
[11]Lawrence Berkeley Laboratory, USA
[12]Massachusets Institute of Technology, USA
[13]Stanford University and SLAC, USA
[14]Stony Brook University, USA

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1 Scientific Context and Objectives

The vertex detectors at the e^+e^- Future Circular Collider (FCC-ee) need to satisfy stringent performance requirements, mainly coming from the measurement of the Higgs boson properties and heavy flavor physics (b and c quarks and τ leptons). The reconstruction of secondary and tertiary vertices, for instance, in the rare decay channel $B^0 \to K^{*0}\tau^+\tau^-$, demands very high precision tracking, especially at low momentum, which is typical of the entire center of mass collision energy regime at FCC-ee.

A good figure of merit for assessing the capabilities of vertex detectors is the track impact parameter resolution $\sigma(d_0)$. For FCC-ee, the requirement on the transverse impact parameter resolution is

$$\sigma(d_0) = 3\text{µm} \oplus \frac{15\text{µm}}{p \sin\theta^{3/2}} \ . \quad (1)$$

*corresponding author: e-mail: Fabrizio.Palla@pi.infn.it

Sensors with a small point resolution are required to achieve the 3 µm asymptotic resolution for high-momentum particles, represented by the first term in Eq. 1. At the same time, the detector material budget must be minimized to keep the second term of Eq. 1 small ($\lesssim 0.3\,\%$ of a radiation length X_0), thus enabling good vertexing performance for low-momenta particles. Additionally, time resolving capabilities, matching bunch spacing must be provided to ensure assignment of hits to the correct events to reduce background noise and pileup and enhance the reconstruction.

The radiation environment expected at the Z pole is of the order of 100 kGy/year for the innermost detector layer, placed right after the beam pipe, which has an internal radius of 1 cm. The expected fluence for the same layer is of the order of a few 10^{13} $\mathrm{n_{eq}}$ cm^{-2} per year.

The most significant hit rate contribution is coming from the background process of Incoherent Pairs Creation (IPC) [1], which describes a class of interactions between two photons emitted by a single electron and a single positron at the IP, $e^+e^- \to (e^+e^-)e^+e^-$. Although the bulk of these pairs is emitted below the vertex detector acceptance, the hit rate expected in the first layers is of the order of 100 MHz cm^{-2}, to be compared to the highest physics event rate expected at the Z pole of about 100 kHz.

Summarising all the above requirements for the innermost vertex detector layers as foreseen by current concepts explored for the FCC-ee Feasibility Study at the Z peak:

- 3 µm point resolution and 20 ns timing resolution
- sensor thickness smaller than 50 µm and material budget of $\lesssim 0.3$ % of X_0
- Power consumption $\lesssim 50$ mW cm^{-2} to allow for air-cooling
- few 10^{13} cm^{-2} $\mathrm{n_{eq}}$ /year fluence per year
- 100 kGy/year total ionizing dose
- $\mathcal{O}(100\,\mathrm{MHz\,cm^{-2}})$ highest particle hit rate for the innermost layer at a radius of 1.37 cm
- Acceptance up to $|\cos\theta| < 0.99$ for all layers

Further essential aspects of the design include the requirement for high detection efficiency, robustness against environmental conditions, and stability and maintenance of calibration and alignment.

CMOS monolithic active pixel sensors (MAPS) are the ideal candidates for building such a vertex detector thanks to the possibility of thinning them to small thicknesses and the feasibility of achieving a small pitch and low-power dissipation. None of the current MAPS prototypes [2, 3, 4, 5, 6, 7, 8, 9] fulfills all of these requirements at the same time, and specific R&D for FCC-ee vertex detectors is needed.

This EoI outlines an R&D program for adopting new techniques and designing, simulating, and producing prototype vertex detector elements that can achieve the required performance. It also aims to explore possible improvements in the vertexing capabilities beyond the currently defined requirements and investigate how this expands and enhances the FCC-ee physics programme.

The Institutes of this EoI have long-standing experience designing, fabricating, and operating vertex detectors at e^+e^- and hadron colliders and are also involved in currently ongoing programs such as the ePIC Silicon Vertex Tracker Detector (SVT) for the Electron Ion Collider (EIC) [10, 11], including already pathways for its future upgrades. They are fully involved in the ECFA DRDs and US CPAD R&D programmes for detector developments.

The Italian groups pioneered vertex detector development at colliders, at LEP, Tevatron, PEP-II, SuperKeKB, BES, and LHC. The Frascati National Laboratory, where the first e^+e^- collider has been conceived and built, also leads the development of the interaction region layout of the FCC-ee, and in particular, the beam-pipes and the integration of the vertex detector. INFN is leading the development of the MAPS in LFoundry110 nm technology with the ARCADIA [5] project. The INFN and Italian university groups lead the integration of the vertex detectors at SuperKEKB and LHC, and they are developing the design of the lightweight mechanics for the FCC-ee vertex detectors, including air-cooling based solutions with advanced simulations and experimental setups. INFN and Italian university groups have been setting up test beam campaigns for the study of the performances of the sensors, together with international partners.

The U.S. groups, based at both universities and national laboratories, have long and expansive experience and capabilities in all areas of tracking at colliders. These groups have made leading contributions to the tracking systems at the Tevatron Collider, at PEP and the SLAC B-Factory, at CLEO, ATLAS, and CMS at the LHC. U.S. groups are also well connected with the low-mass tracking efforts at RHIC and ALICE, having developed aspects of the air-cooled supports for STAR, among others. BNL is deeply involved in the development of MAPS detectors, both by utilizing the original sensors and advancing large-area derived sensors based on those being developed for ALICE ITS3 upgrade. The team is also working on supporting infrastructure of the vertex and tracking detector, including serial powering, sensor bias, and slow control management for the MAPS-based ePIC SVT detector. BNL is conducting R&D on next-generation sensors for future ePIC SVT upgrades. Currently, the group is preparing a 1-megapixel binary readout MAPS detector for fabrication, employing an event-driven readout [12] approach using the TPSCo 65 nm process. This sensor aims to demonstrate O(100 ns) timing resolution and is dimensionally compatible with the Repeated Stitched Unit (RSU), constitutin a building block of a large area detector of ALICE ITS3, fostering future collaborative R&D efforts. Furthermore, teams at FNAL and SLAC have demonstrated significant progress through design simulations, prototypes, and test-beam characterization of MAPS devices in collaboration with international partners and are currently focused on designs with TPSCo 65 nm, SkyWater 90 nm, and LFoundry 110 nm nodes. Finally, university groups such as Brown and Stony Brook have been setting up test setups for the characterisation of new sensors and preparing test beam campaigns.

UZH, ETHZ, and PSI are leading the development, construction, and upgrade of pixel detector systems for the LHC. Key components, namely sensors, readout ASICs, mechanical structures, and cooling systems, have been conceived and built in Switzerland. UZH started R&D towards the FCC-ee VXD in 2021, focusing on detailed simulations for performance evaluation and the relation to the physics program. UZH, PSI, and ETHZ are engaging in the MAPS R&D lines in the 150 and 110 nm LFroundry processes (MoTiC [13]) and the 65 nm TPSCo process (APTS[14], CE-65 [15, 16], and OCTOPUS [17]).

2 Design and operational aspects

Vertex detectors at FCC-ee face numerous challenges, most of which are intertwined. The most challenging requirements come from the operation at the Z pole.

The very demanding hit resolution of 3 µm can be achieved either using standard MAPS technology with analog readout by exploiting charge sharing or, doing better, by a modified process with improved charge collection and combining binary readout with a smaller pixel pitch. An example of a modified process can be the TPSCo 65 nm process that is based on a standard process suited for CMOS image sensors operating in visible light, but where the substrate features increased resistivity and an arrangement of implantation assures no parasitic charge collection and provides the possibility of implementing circuits with complementary types of transistors. Process selection, operation in the analog or binary domain and readout of data have implications on the overall system designs, since, particularly smaller pitch directly may impact on the power consumption, material budget, amount of data to be transferred, extractable timing, etc.

Achieving a low material budget in the detector acceptance requires minimizing sensor thickness, carefully designing low-mass mechanical structures, and optimizing power distribution and readout strategies to reduce (typically copper-based). Requiring a small power density in the vertex sensor is connected with ability to use lightweight air- or Helium-based cooling systems, which is advantageous even if its integration needs to be carefully designed. What is particualrly challenging is that any possible induced vibrations on the low-mass structures should be kept much smaller than the single hit resolution.

Avoiding tracking ambiguity, pileup, and background accumulation requires the introduction of time-resolving detectors. When combined with the need for high granularity to achieve the required spatial resolution, this necessitates a transformational shift from framing detectors to real-time, zero-suppression, event-driven detectors. There is no viable alternative to this approach, as the expected lightweight design and the need for maximal active area coverage impose two key constraints, on the first hand, in-pixel time measurement circuitry is unfeasible due to complexity and material limitations, and on the second hand, accumulating time-stamped events for triggered readout is impractical, except possibly with vertical stacking, which is again constrained by material budget limitations. For these reasons, FCC-ee detector research must adopt an innovative approach to large-scale, high-speed readout.

The design of the machine-detector interface (MDI) region is challenging at FCC-ee, given that the first accelerator components (compensating solenoid and first quadrupole magnets) are located inside the detector [18]. In the last few years, the IDEA vertex detector has been successfully integrated into the MDI [19]. Given the key role of the beam pipe material and the first vertex layer radial position for the vertexing performance, however, further optimization of the interplay between the beam pipe and vertex detector could enhance the vertex detector capabilities.

At the Z pole, IPC dominates the hit rate in the vertex detector, far above the hit rate from the interesting physics processes. Significant uncertainties remain regarding the impact of IPC on the hit rate, which also depends, for example, on the sensor cluster multiplicity and hit digitization strategy. The capability of the vertex detector to deal with this high hit rate (and resulting data rate) can determine the global detector decision on using a trigger.

The implication of the different running conditions of FCC-ee at different center-of-mass energies have not yet been thoroughly investigated, and given the lower interaction frequency and instantaneous luminosity, may result in less stringent requirements on vertex detectors than those at the Z pole, thus allowing different solutions for each center-of-mass energy, also having implication for the beam pipe design, although some high-statistics runs at the Z may be required to calibrate the detector. For instance, for the ZH run, a couple of days run at the Z peak, for calibration purposes, could allow tens of millions of events being recorded even with a 100 times smaller luminosity than the highest one achievable at that energy, thus implying proportionally smaller backgrounds and heat loads on the beam pipe. Therefore, accommodation of the possibility to have vertex detectors and beam pipe appropriately developed for the ZH, different for those at the high-luminosity runs at the Z, is conceivable.

Another challenge yet to be addressed in detail is the design of the vertex detector forward region, where barrel geometries inherently produce a significant material budget and limited spatial resolution compared to those in the more central region. Similarly, the interplay of the vertex detector with the main tracker is still under investigation, and it inevitably determines the design choices of the vertex detector layers close to the tracker inner boundary.

The phase space to achieve the vertexing performance outlined in Section 1 is large and can be reached by several combinations of, for example, single hit resolution, geometries, and material budgets. Finding the best solutions depends on the sensor technology and electronic and mechanical designs, including service and cable routing.

Eventually, the system integration, alignment and calibration will impact the final performance and need to be carefully studied in advance.

3 Methodology

Evaluating and comparing different vertex detector layouts requires a set of meaningful performance metrics.

The first figure of merit is the impact parameter resolution, evaluated both transversely and longitudinally, for the most extensive possible momentum range. Another figure of merit is the track reconstruction efficiency, also down to low momentum tracks.

To ensure that the actual physics deliverables are considered, this project will use physics case studies of processes where vertex performance is crucial as figures of merit. One process will be $B^0 \to K^{*0}\tau^+\tau^-$ introduced in the very beginning, for which an improvement of the impact parameter resolution would enable the measurement of this process down to the branching ratio expected in the Standard Model [20]. We will also study the impact of different vertex detector layouts and resolutions on the flavor tagging performance, which is directly linked to the essential measurements of the $b-$, $c-$, and $s-$quarks Higgs Yukawa couplings.

All these studies will be performed in full simulation, for the IDEA and ALLEGRO detector concepts, using realistic models of vertex detectors and digitization of a sensor response. The simulations will also consider the systematic effects of the alignment, calibrations, and any other sources of systematics and operational aspects.

The geometry optimization will explore the locations and number of layers, as well as their pitch, including long-barrel and barrel+disks solutions for the inner part of the vertex, below a radial distance from the beam line $r \approx 5$ cm. The layouts should be compatible with the designed MDI region, which envisages a central beam pipe 18 cm long with 2 cm inner diameter that must be cooled separately. The possibility of cooling the inner vertex and the beam pipe with the same circuit will also be studied. We will finally explore, at a later stage, the feasibility of including the innermost or the inner two layers inside the beam pipe, following the proposal for ALICE3 [21]. In this case, the main challenge is to study the compatibility of the maximum achievable data rate with the expected background levels and the heat load removal induced by the beam current on the secondary vacuum.

The other side of the integration will explore the boundaries of the outer Silicon vertex detector (between ≈ 10 and 35 cm), also using the MAPS technology, with the central tracker, for which several options are proposed: gaseous drift chamber, TPC, straw tubes, and scintillating fibers. The definition of the number of layers and their boundaries with respect to the central tracker and the inner vertex will be investigated.

The work to be carried out by this EoI is well inserted in the ECFA DRD8 [22] R&D, where solutions for lightweight mechanics and cooling, as well as the integration within the interaction region, will be studied. The R&D will profit from the activity at INFN, where a mock-up of the central interaction region is currently being developed, including the mechanics of the vertex detector of IDEA.

Finally, we will explore the timing requirements needed for detector readout and track reconstruction performance, as well as to provide an inner time reference for time-of-flight measurement for particle identification

The vertex detector system design will make use of MAPS solutions based on currently known three process options: TPSCo 65 nm, LFoundry 110 nm, and SkyWater 90 nm with developments starting in DRD3 and DRD7. The former two technologies currently allow building reticle-sized, abutted, or wafer-scale sensors with thin (50 μm) silicon layers. Options exist with a hybrid digital logic layer or bending the sensors following the developments of ALICE ITS3 [23]. This leads to the following phase-space to be explored for the sensors:

- Fabrication Process Options: TPSCo 65 nm, LFoundry 110 nm and SkyWater 90 nm will be considered. If other technological options emerge, they will be evaluated and considered as potential platforms for prototype fabrication.

- Embedded On-a-Sensor Processing: Although not necessary for the innermost layers, new circuit solutions, such as Time-to-Digital Converters (TDCs) for low-power, sub-ns timing resolution for the outer vertex layers, located beyond 10 cm in radius, will be explored. These advancements are enabled by shrunk process nodes and enhanced transistor options, particularly in the TPSCo 65 nm process.

- Sensor size: Various process platforms for large-area detectors will be explored, including single reticle, side-buttable tiling, 1-D and 2-D stitching, and full-wafer-scale MAPS. Special focus will be on yield optimization and design-for-manufacturability strategies.

- Sensor shape: To optimize material budget, resource supply, and connectivity, various structural options will be explored, including flat (staves), curved (1D-stitched), and half-cylindrical (wafer-scale, self-supporting layers). Their suitability for different vertex and tracking detector regions will be assessed.

- Readout methodologies: Given that the performance of a highly granular detector depends on how data can be efficiently transmitted while preserving key information, such as time of origin, and considering that traditional frame-based readout is not suited for future FCC-ee requirements, research efforts will focus on developing in-situ, intrinsically sparsifying readout methodologies, such as event-driven readout. These methods are the most energy-efficient, effectively extracting useful data from multi-channel systems, where most channels remain inactive at a given moment.

4 Timeline

Two phases are envisioned for the work on vertex detectors:

- 2025 – 2027: Explore various kinds of vertex detector concepts and layouts, develop tools necessary to enable efficient comparison

- 2028 – 2030: Narrow down to just a couple of vertex detector concepts as input to detector CDRs, and to be studied in more detail in the TDR phase

The planned activities for the first phase (2025 – 2027) are as follows:

- **Vertex detector concepts comparison**
  - Interfacing sensor simulation (from TCAD or AllPix2) with detector full simulation to realistically evaluate final tracking and vertexing performance
  - Establishing figures of merits evaluation workflow (incl. case study designs)
  - Establish workflow for machine background study
  - → First rough exploration of vertex detector phase space
- **Engineering studies**
  - Mechanical design and fabrication of vertex detector structures, including bent sensors
  - Experimental validation of cooling possibilities, including air-cooling
  - Investigation of serial powering solutions for biasing the detectors
  - Studies of integration of power over fiber biasing
  - Studies of integration of wireless data communication
  - Integration studies of a mechanical vertex structure with beam pipes in an interaction region mock-up
- **MAPS development**
  - Design and simulation of MAPS (TPSCo 65 nm, Lfoundry 110 nm, SkyWater 90 nm)
  - Investigate the possibility of stacking wafers and/or more scaled CMOS processes (below 65 nm) to achieve improved granularity to meet the goal for future vertex detectors of 3 μm spatial resolution.

For the second phase (2028 – 2030), the following activities are foreseen:

- **Vertex detector concept comparison**
  - Narrow-down selection to only a couple of vertex detector concepts
  - Optimization of these concepts
  - → Vertex detector concepts ready for TDR phase
- **Engineering studies**
  - Mechanical design and prototypes of selected vertex detector concepts
  - Definition of cooling, powering, and readout concept of selected detector concepts
  - Engineering study of integrated cooling system of beam pipe and vertex detector
  - Engineering study of vertex layer(s) inside beam pipe
- **MAPS development**
  - Large-area demonstrators of MAPS (TPSCo 65 nm, Lfoundry 110 nm, SkyWater 90 nm) components for vertex and tracking

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