The ALCOR ASIC for the ePIC dRICH

Fabio Cossio (INFN Torino)
on behalf of the ALCOR group

Incontro ePIC con referee INFN
Torino, 25 July 2025

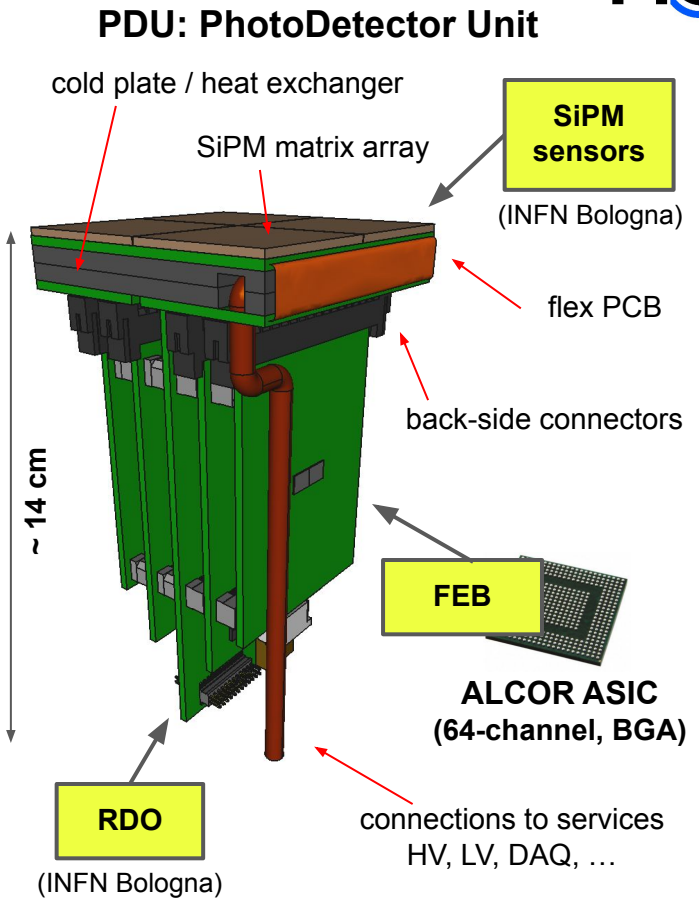
dRICH ALCOR

dRICH requirements:

- Provide **single-photon time tagging** (σ_t ≃ 150 ps) of signals from SiPM sensors
- Cope with **SiPM DCR: 300 kHz/channel** (at max SiPM radiation damage)

ALCOR main specifications:

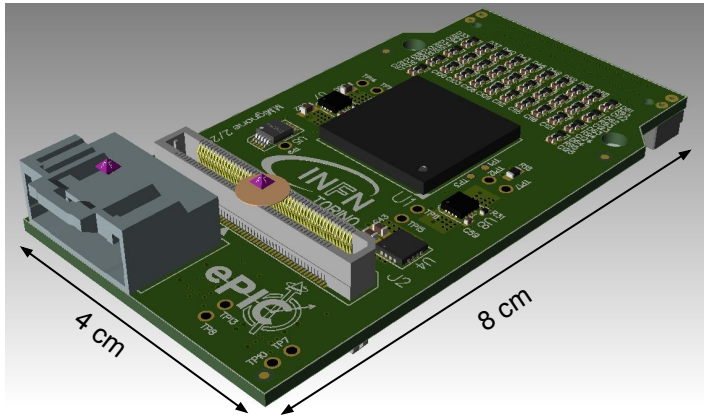
- **64-pixel** matrix (8x8) mixed-signal ASIC
- Single-photon time tagging + **Time-over-Threshold** or **Slew-Rate** measurements for **time walk correction**
- On-chip **signal amplification**, **conditioning** and **digitization**, **trigger-less** readout (+external hardware **shutter**) with fully digital output: **8 LVDS 394 MHz** DDR Tx links
- Power consumption **~12 mW/channel,** 0.11 μm CMOS technology



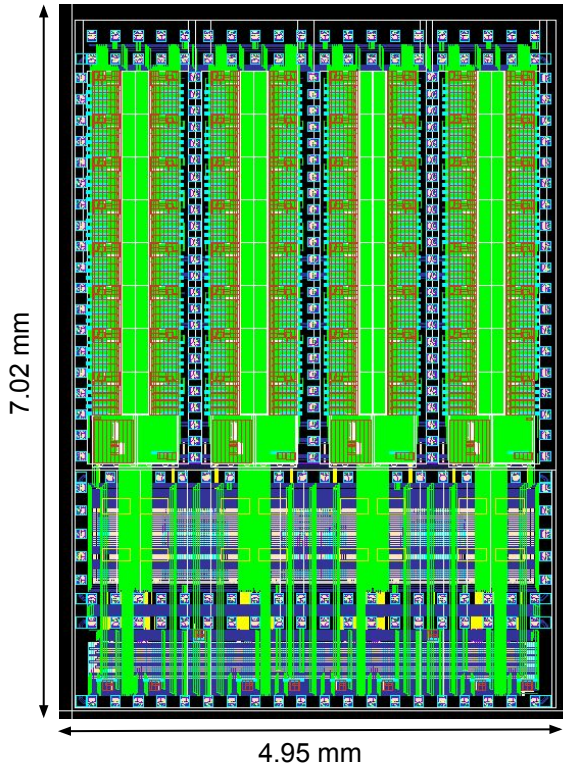
Summary of 2024-2025 activities

- **ALCOR-64** (ALCOR v3) MPW tapeout on Apr 2025
- **BGA interposer** design completed on Jan 2025
- dRICH **FEB** design completed on May 2025
  - **Fake-FEB:** received on Mar 2025 → Nov 2025 beam test with RDO and ALCOR v2.1
  - **SMA-FEB:** same design of dRICH FEB + SiPM SMA debug output → **annealing** and **temperature studies**

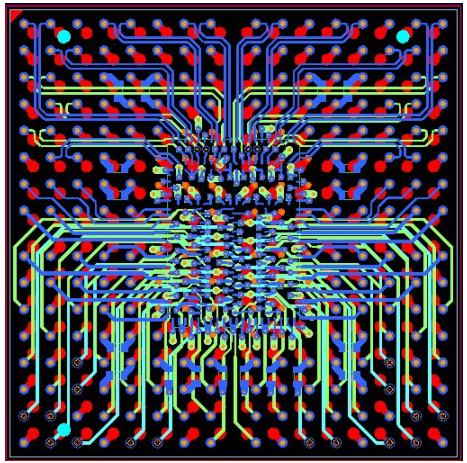
ALCOR FEB

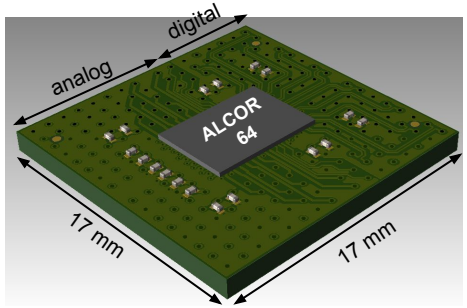


ALCOR-64



BGA interposer





Next steps (towards production)

ALCOR-64 MPW tapeout on Apr 2025, 50 singulated dies expected for Sep 2025, then packaging

ALCOR-64 testing

- End of 2025: test ALCOR-64 from MPW → first electrical characterization in Torino
- Start of 2026: tests with SiPM sensors and RDO → fully assembled PDU
- **dRICH-FEB first engineering articles** for detector box prototype → final validation

Milestone 2026: "Caratterizzazione ALCOR a 64 canali"

Preparation for production

- Mid 2026: design revision

Funding request for 2026

Start of production

- End 2026 - Start 2027: **Engineering Run (ER)**
- 2027: **ALCOR BGA-Packaging**
- 2027-28: mass production **QA tests**

Funded (partially) already in 2025 (**220 k€** vs **270 k€**)

Funding requests for 2026

This is the **best case scenario**: we have contingency time for one extra MPW run in 2026 and production during 2027

End 2025: start development of **ALCOR and FEB QA test setup**

ALCOR package

Organic Substrate

Description	Sample	Production	Remarks
NRE for design + manufacturing layout	EUR 3,700.00	-	1x charge only, unless up revision
NRE for tooling + SOP (Coining)	EUR 3,700.00	-	
Lot charge for 50 pcs	EUR 7,000.00	-	
Unit price for 5000 pcs	-	EUR 11.00	
Sub Total	EUR 14,400.00	EUR 55,000.00	

Assembly

Description	Sample	Production	Remarks
NRE for design + assembly layout	EUR 5,500.00	-	1x charge only, unless up revision
NRE for FlipChip die + Component toolup	EUR 24,100.00	-	
NRE for BGA ball attach toolup	EUR 11,000.00	-	
NRE for mold chase toolup	-	EUR 20,000.00	
Unit price for UBM/wafer		EUR 650.00	Estimated @ 9 wafers requirement for 6,000 unit production (EUR 5,850)
Lot charge for 50 pcs	EUR 24,000.00	-	BOM (18x capacitors included)
Unit price for 5000 pcs	-	EUR 31.00	Includes BOM (18x capacitors included)
Additional 1,000 pcs requirement for 2026 (Package price)*		EUR 22,000.00	1-time goodwill charge to INFN (Covers Organic substrate+Assembly costs)
Sub Total	EUR 64,600.00	EUR 202,850.00	

Costi extra rispetto a preventivo 2024:

- UBM: precedentemente era stata inclusa nei costi ER
- +1000 pezzi di spare

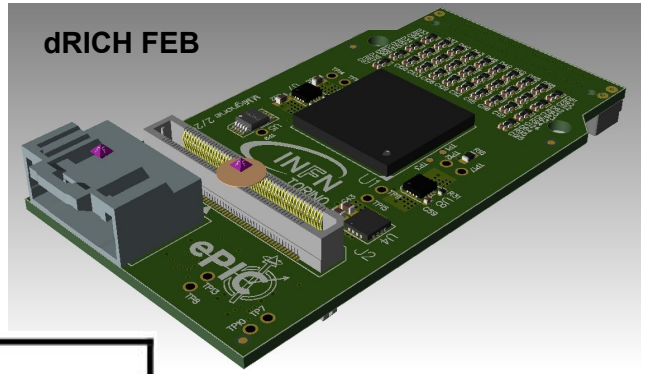
Package BGA di 6000 ALCOR chip:

Production cost: 258 kEUR + IVA = **315 kEUR**

Richiesta 320 kEUR

Include anche *2% incentivi per le funzioni tecniche ex art. 45 del d.lgs. n. 36/2023*

dRICH FEB



First engineering articles della FEB (pre-produzione, 20 coppie master-slave)

Da offerta per produzione di 7 coppie SMA-FEB:

codice: **SMA_AL64_FEB_Master-Slave**			
Attrezzatura produzione c.s.	(10 strati I-TERA M140, ENIG)	€	950,00
Startup montaggio & lamine		€	650,00
Produzione n. 7 schede assemblate (1M + 1S)	(p.zo unitario € 580,00)	€	4060,00
	TOTALE:	€	**5660,00**

Questa offerta per le SMA-FEB non include la saldatura del BGA (ALCOR) e l'ispezione raggi-X per il controllo delle connessioni sul BGA

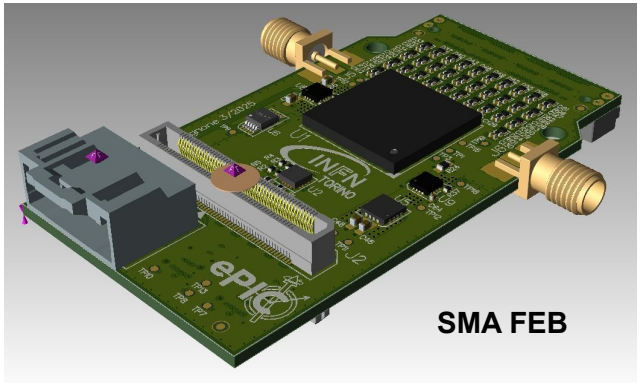
FEB necessarie alle attività di preparazione alle costruzioni e realizzazione prototipo dRICH detector box (10 PDU)

Per fare **10 PDU** servono **40 FEBs** (20 Master + 20 Slave):

- 950 € + 650 € + (20 · 580 €) = 13.2 k€ + IVA = **16.104 k€**

Richiesta 20 kEUR

Atteso leggero incremento sul costo unitario per saldatura BGA (ALCOR) e ispezione raggi-X



ALCOR QA boards (1)

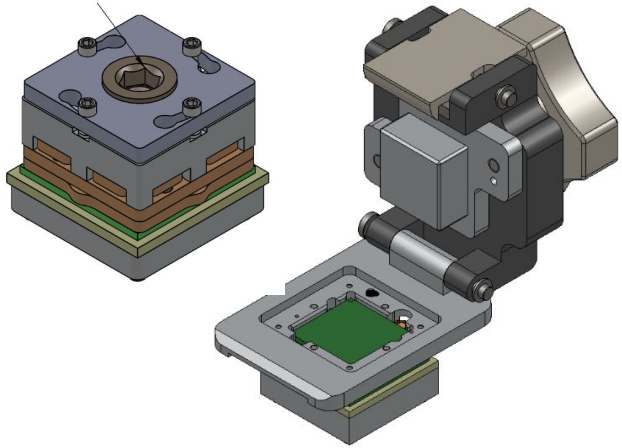
I disegni delle seguenti 2 schede di test non sono ancora pronti, verranno ultimati tra fine 2025 e inizio 2026. Per i preventivi vengono allegate offerte per l'acquisto dei componenti più rilevanti o per la produzione di schede simili precedenti

1) Scheda di test con zoccolo per BGA (2x)

Scheda di test con socket BGA, necessaria per test e validazione dei singoli device ALCOR-64 prima che vengano montati sulla FEB

Preventivo per **socket BGA** Ironwood Electronics da B.C.E. (fornitore Italia):

Ps	Ns. Codice (Our Code)	Vs. P.N. (Your P.N.)	Descrizione (Description)	Q.tà (Q.ty)	Prezzo (Unit Price)	Tot. (Extended Price)	Consegna (Delivery)
1	SBT-BGA-6006		SBT-BGA 17X17MM 1MM 16X16 ARR	2	€ 1.300,00	€ 2.600,00	5 / 6 weeks aro
2	CBT-BGA-6064		CBT-BGA/LGA256 17MM 16X16 1MM	2	€ 2.150,00	€ 4.300,00	5 / 6 weeks aro
3	Shipment cost			1	€ 60,000	€ 60,000	



Solderless socket for burn-in and test applications (https://www.ironwoodelectronics.com/)

2x schede di test con socket BGA

- Socket: 3.5-5 kEUR
- PCB: 1-2 kEUR

Richiesta 6 kEUR

Inclusa stima su costi realizzazione PCB e assemblaggio altri componenti

ALCOR QA boards (2)

I disegni delle seguenti 2 schede di test non sono ancora pronti, verranno ultimati tra fine 2025 e inizio 2026. Per i preventivi vengono allegate offerte per l'acquisto dei componenti più rilevanti o per la produzione di schede simili precedenti

2) Adattatore FEB verso FPGA commerciale (5x)

Scheda adapter per interfacciare le FEB (1 Master + 1 Slave) a FPGA commerciale per test FEB standalone

Scheda Fake-FEB (prodotta a inizio 2025) ha caratteristiche molto simili (componenti, connettori):

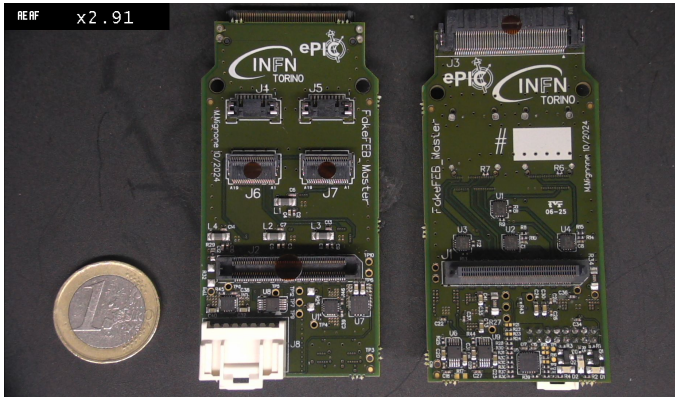
codice: **ALCOR_FAKE-FEB (KIT 1MASTER + 1SLAVE)**			
Attrezzatura produzione c.s.	(6 strati, DE104, ENIG)	€	500,00
Setup montaggio e lamine		€	650,00
Produzione n. 10 schede assemblate (1M + 1S)	(p.zo unitario € 400,00)	€	4000,00
Produzione n. 20 schede assemblate (1M + 1S)	(p.zo unitario € 380,00)	€	7600,00

	TOTALE:	€	**xxx0,00**

5x schede adapter:

➢ 500 € + 650 € + (5 · 400/2 €) = 2.15 k€ + IVA = **2.623 k€**

Richiesta 3 kEUR



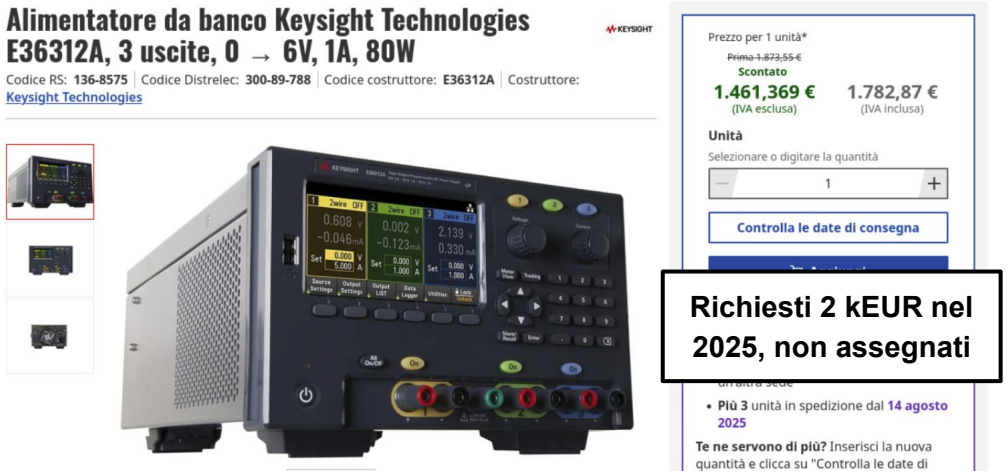
Fake-FEB attuale: *Firefly* verso ALCOR FE DUAL, *ALCOR BUS* verso RDO
Nuova adapter: *Firefly* verso scheda FPGA commerciale, *ALCOR BUS* verso dRICH FEB

Atteso incremento del costo unitario dato il minor numeri di pezzi da ordinare

QA setup instruments

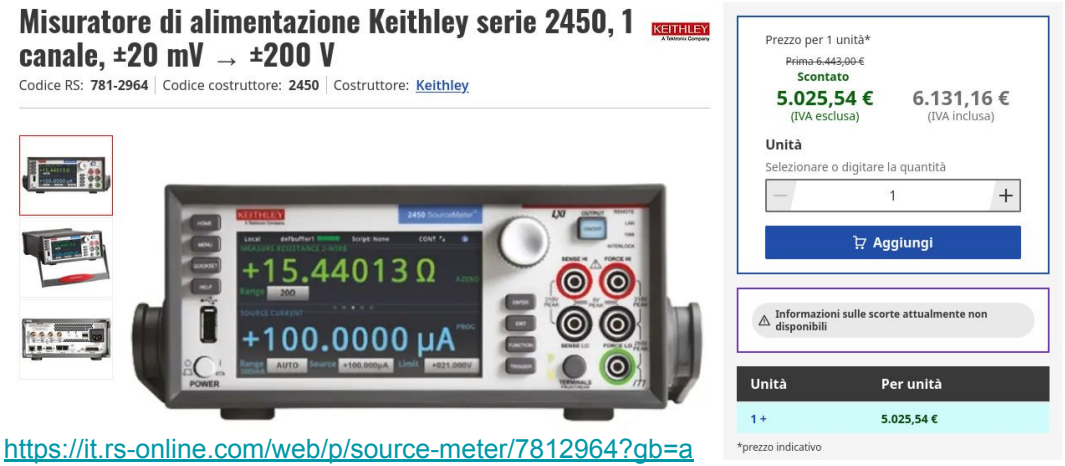
Strumentazione per sviluppo sistema di test per QA ALCOR e FEB:

- setup automatizzato con strumenti controllati da remoto (FEB-SiPM power ON/OFF, controllo consumi ALCOR)



Richiesti 2 kEUR nel 2025, non assegnati

https://it.rs-online.com/web/p/alimentatori-da-banco/1368575



https://it.rs-online.com/web/p/source-meter/7812964?gb=a

1. **ALCOR LV**: Alimentatore da banco Keysight Technologies E36312A
2. **SiPM HV**: Misuratore di alimentazione Keithley serie 2450

Richiesta 8 kEUR

Riepilogo richieste 2026

apparati

- ALCOR BGA Package **Richiesta 320 kEUR**
- First engineering articles della FEB (pre-produzione, 20 coppie master-slave) **Richiesta 20 kEUR**

consumo

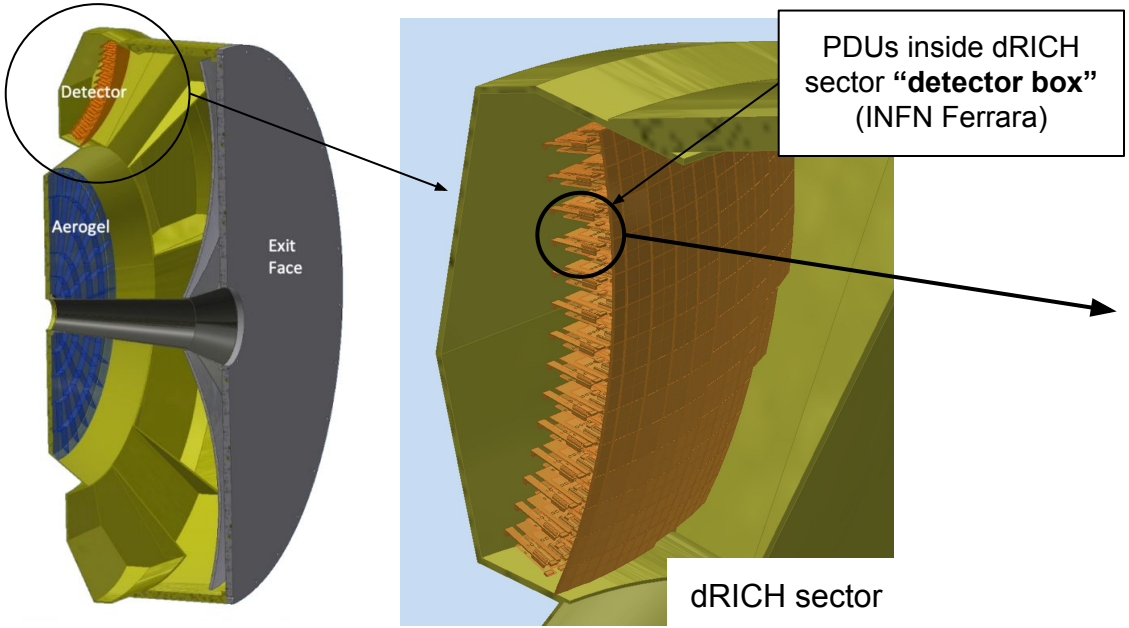
- Scheda di test con zoccolo per BGA **Richiesta 6 kEUR**
- Adattatore FEB verso FPGA commerciale **Richiesta 3 kEUR**

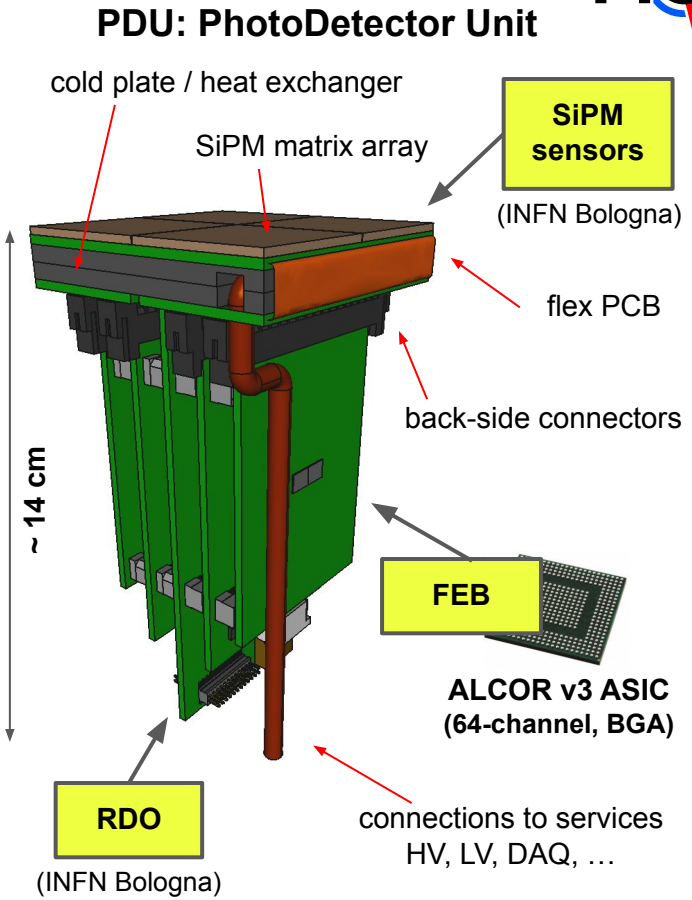
inventario

- Alimentatore da banco Keysight Technologies E36312A e Alimentatore HV Keithley serie 2450 **Richiesta 8 kEUR**

Backup Slides

dRICH electronics





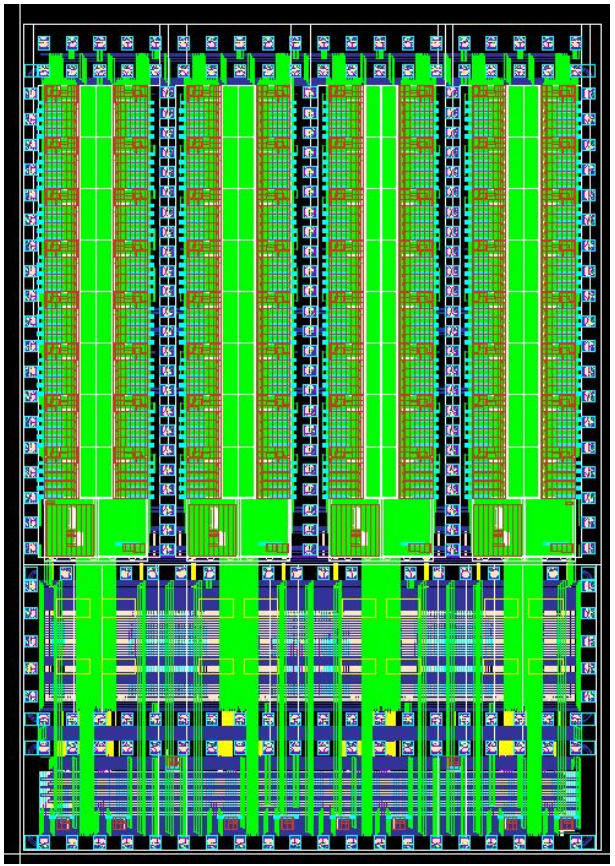
- **1 PDU**: 4x64 SiPM array device (256 channels), **4 FEBs, 1 RDO**
- **1 ALCOR** (64 channels) per **FEB:** 8x8 SiPM matrix readout
- 6 sectors: 208 PDUs/sector → 1248 PDUs for full dRICH readout
- **4992 FEBs → 4992 ALCOR v3** (64-channel)
- **319488** readout **channels**

ALCOR: **A** **L**ow Power **C**hip for **O**ptical Sensor **R**eadout

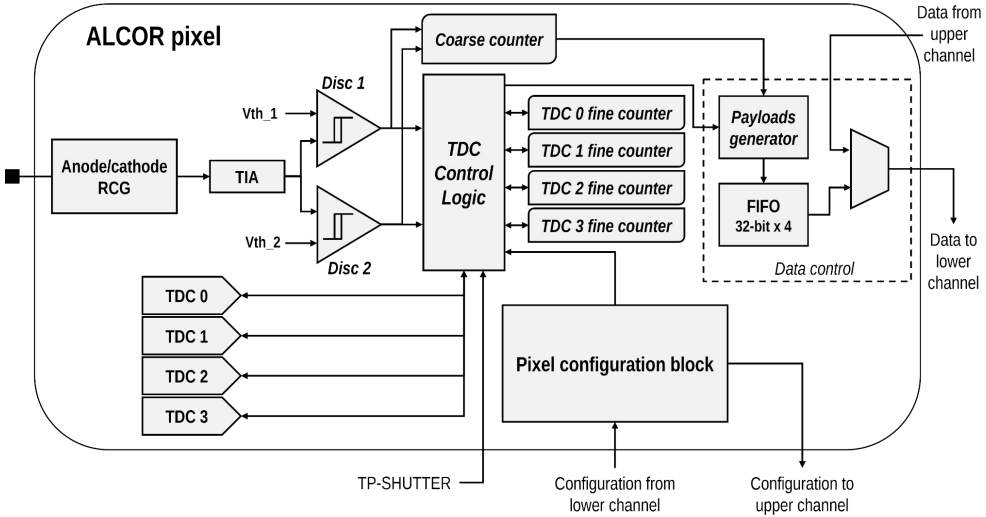
ALCOR-64 (ALCOR v3)

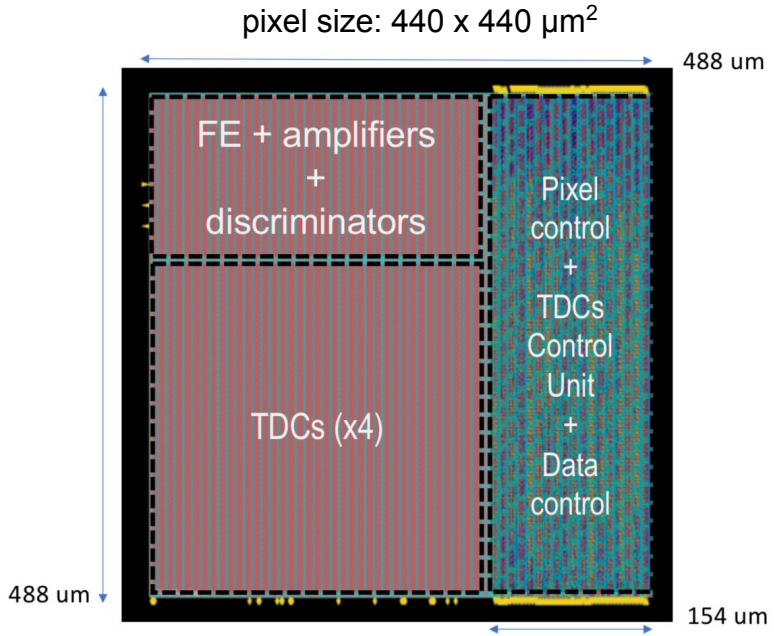
- **64-pixel** matrix (8x8) mixed-signal ASIC (4.95 × 7.02 mm^2)
- Single-photon time tagging + **Time-over-Threshold** or **Slew-Rate** measurements for **time walk correction**
- On-chip **signal amplification**, **conditioning** and **digitization**, 32-bit event word
- Trigger-less readout with fully digital output: **8 LVDS 394 MHz** DDR Tx links
- Power consumption **~12 mW/channel**
- **0.11 µm CMOS technology**

✓ **MPW tapeout on Apr 8th 2025**



Pixel architecture

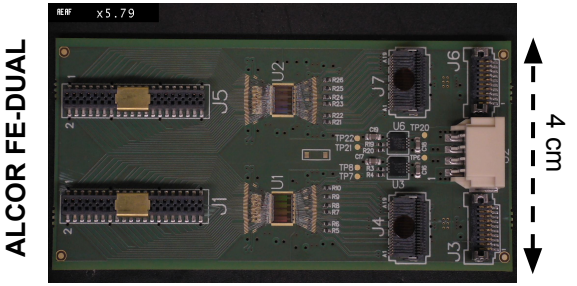




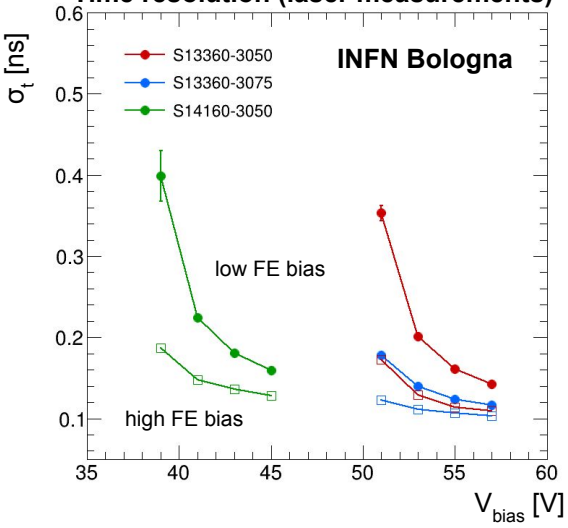
- **Dual-polarity RCG input stage** current conveyor (**Z_{in}= 10-20 Ω**) + **TIA** with 4 gain settings → **σ_t ≃ 150 ps**
- **2 leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC) → **V_{th} = 0.5 p.e.**
- **4 TDCs** based on **analogue interpolation** with **20-40 ps** time-bin (at 394 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration, operating mode and data transmission
- TP-**Shutter** to inhibit events digitization (asynchronous with ns time window in **ALCOR-64**) and suppress out-of-time SiPM DCR hits

ALCOR v2 results

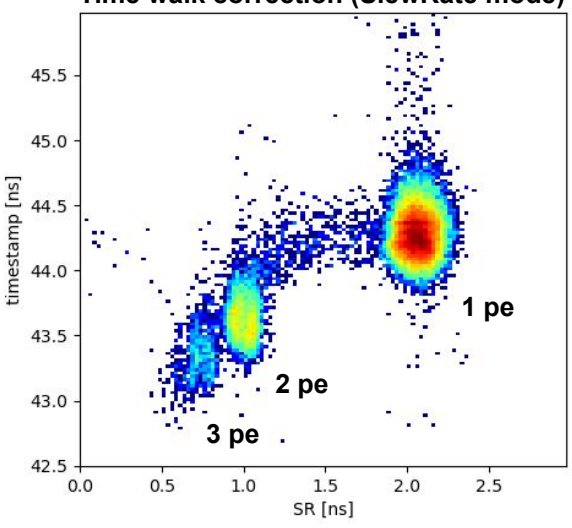
- Better **time resolution** with 75 μm SPADs, comfortably below σ_t = 150 ps also at low V_{bias}
- **Time walk correction**: SlewRate mode provides good separation between afterpulses (slow-rise time, large ToT) and cross-talk (fast rise-time, large ToT)



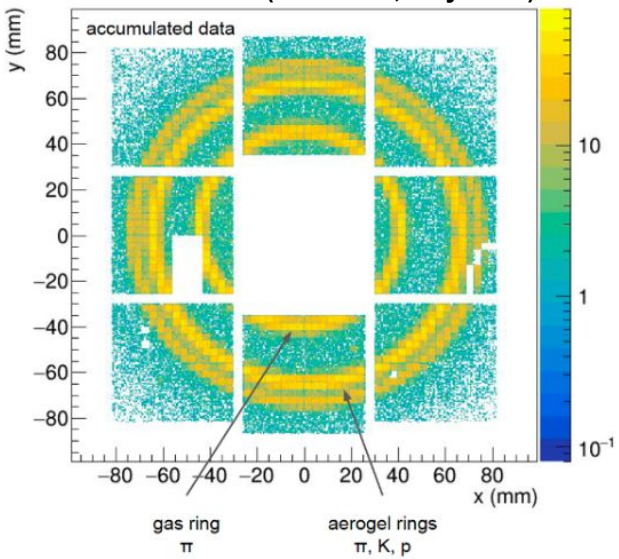
Time resolution (laser measurements)



Time walk correction (SlewRate mode)



Beam test with prototype dRICH and PDUs (CERN-PS, May 2024)

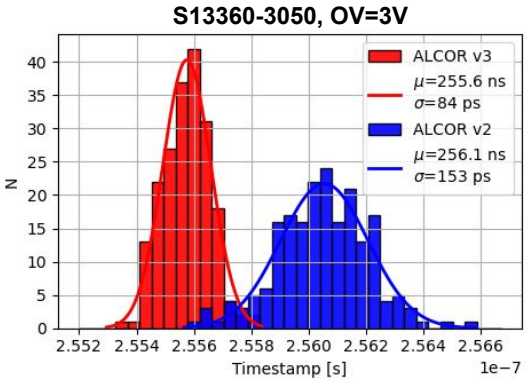


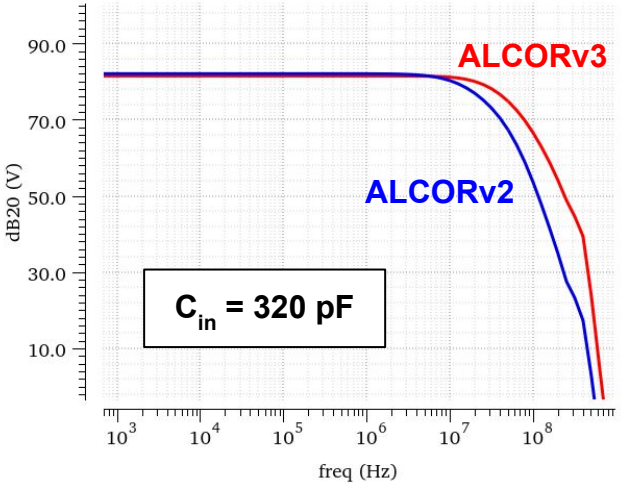
32 FE-DUAL (64 ALCOR, **2048 channels**)
SiPM: HPK **S13360-3050** and **S13360-3075** (3x3 mm^2, T = -30/-40°C)

ALCOR v3 - analogue

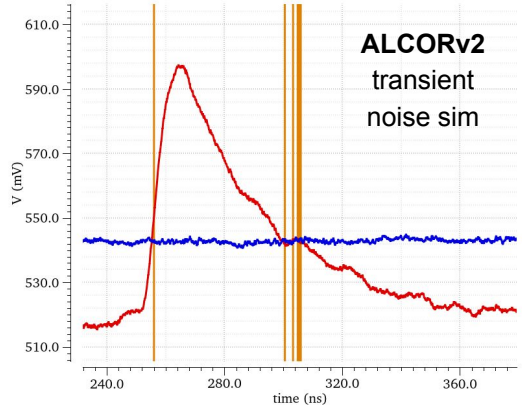
Small revisions on ALCOR FE design

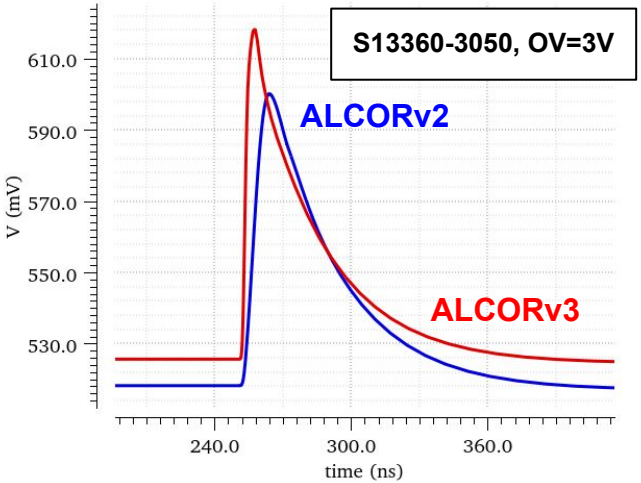
- **Increased amplifier bandwidth** to improve time resolution
  - transient noise simulations
  - Vth = 0.5 p.e.
  - **jitter: 153 ps → 84 ps**





- **Discriminator** with programmable **hysteresis** to avoid re-triggering on slow tail with low thresholds





ALCOR v3 - shutter

ePIC streaming data acquisition system (no traditional hardware trigger)

- Operation at **0.5 p.e. threshold** → DCR noise up to **300 kHz/channel** (at max SiPM radiation damage)
- **Digital shutter**: “inhibit” pixel digital logic to suppress out-of-gate DCR hits and **reduce data throughput**
- ~10.2 ns bunch crossing, ~300 ps bunch length, select **2-3 ns time window**
- Asynchronous digital shutter implemented in ALCOR v3 pixel logic using external test-pulse signal
- **Programmable delay chain**: 4 configuration bits at channel-level (LSB ≃ 350 ps) and at the chip periphery (LSB ≃ 100 ps) to adjust offsets between different pixels and columns
- Shutter needed only when DCR becomes higher due to SiPMs taking radiation damage over time → use first period of ePIC data taking to optimize **shutter calibration** (understand electronics and physics contributions)

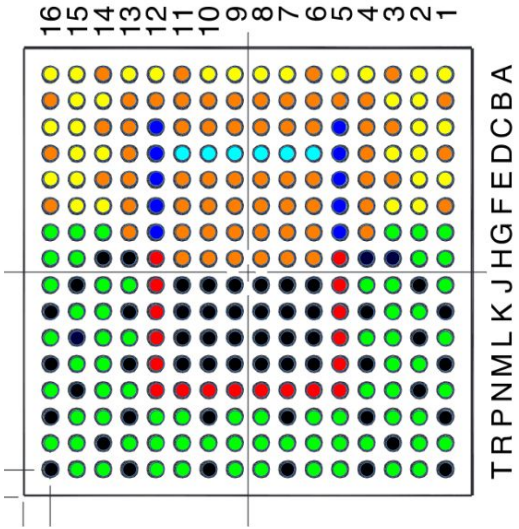
Possible problem of an **excessive data bandwidth** (**> 1 Tbps**) for the ePIC DAQ system when **DCR** approaches **300 kHz**. Two complementary approaches are being considered:

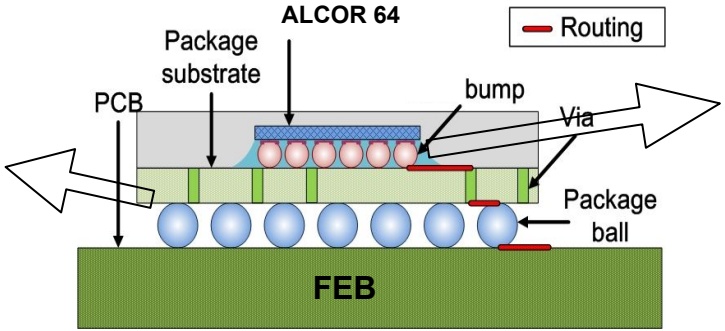
1. **dRICH interaction tagger** (INFN Genova): dedicated sub-detector (scintillating fibers + SiPM + ALCOR based readout) tagging relevant interactions
2. **ML online data filtering** (INFN Roma) at sub-detector level (FELIX DAMs) against pure dark-count event

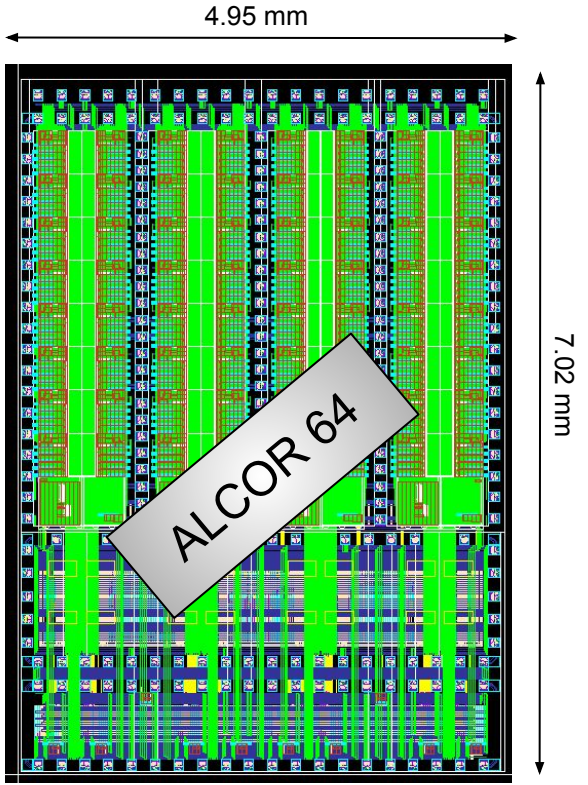
ALCOR BGA package

FC-BGA: flip-chip ball grid array

- BGA substrate designed by INFN Torino (M. Mignone)
- Substrate production, flip-chip assembly and packaging done by I-Tronics (https://www.itronics-sg.com/)







Radiation tolerance

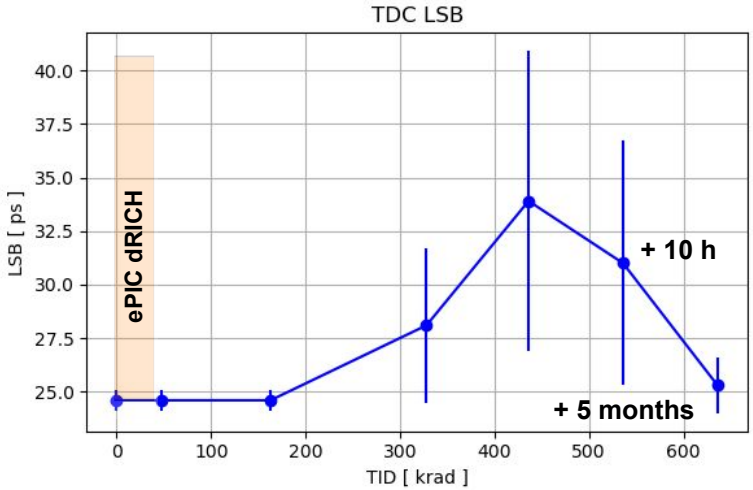
The dRICH-PDUs are in a moderately hostile radiation environment

- Φ (p+n > 20 MeV) = 200 Hz/cm^2
- TID ≅ 2.3 krad (for 1000 fb^{-1})

} safety factor of 5 included

➢ Irradiation tests campaign: SEU/SEL and TID tests at Centro of Proton-Therapy in Trento with ALCOR-32 in Jul 2024 and Dec 2024

- **Technology is sufficiently radiation tolerant** to be used in the ePIC dRICH environment
- **SEU rate is within the expected manageable levels**: in ALCOR v3 TMR SEU protection added also for periphery registers, Hamming code SEU protection for FSMs
- **Other FEB components need be tested and validated**



Detailed results presented at the 29th Jan 2025 dRICH Meeting: https://indico.bnl.gov/event/26313/