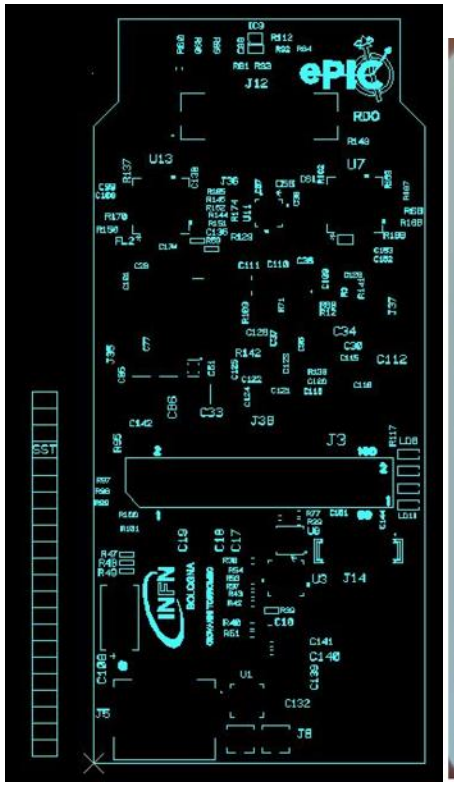
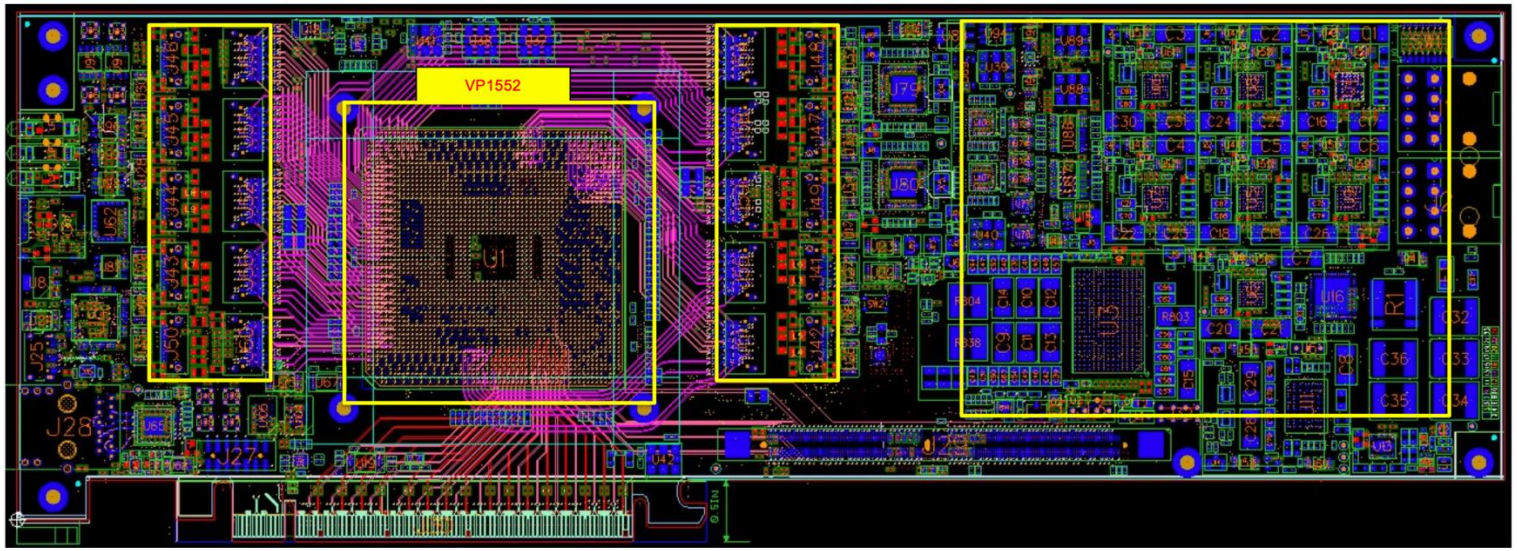
dRICH RDO and DAQ
(frontend and backend DAQ)



P. Antonioli (INFN Bologna), A. Lonardo (INFN Roma1)



meeting with CSN3 referees
Turin, 25 July 2025

dRICH: frontend and backend DAQ

INFN BOLOGNA
Istituto Nazionale di Fisica Nucleare

INFN ROMA
Istituto Nazionale di Fisica Nucleare

dRICH RDO
- 2025 update
- plannning and 2026 activities

FELIX card and dRICH data reduction
- 2025 update
- planning and 2026 activities

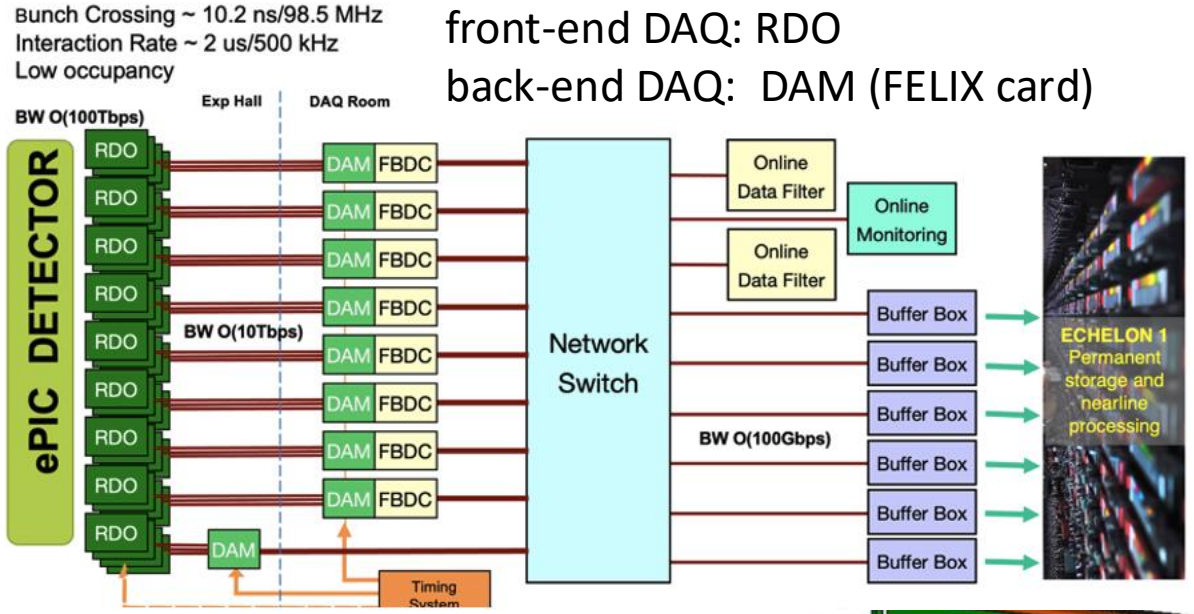
26/27 July

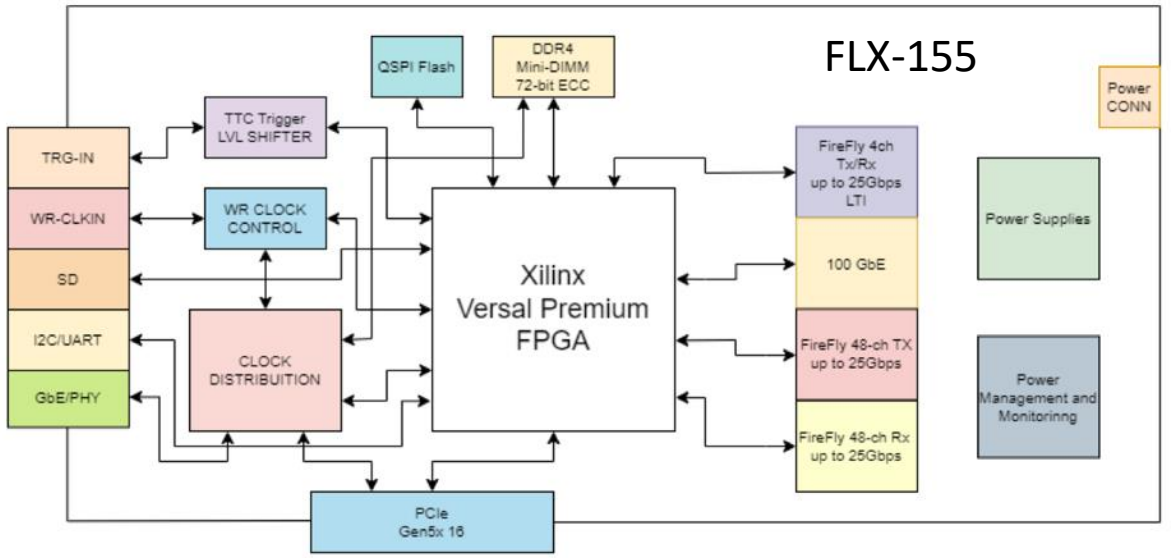
More space to frontend (last year referees had talk about backend)

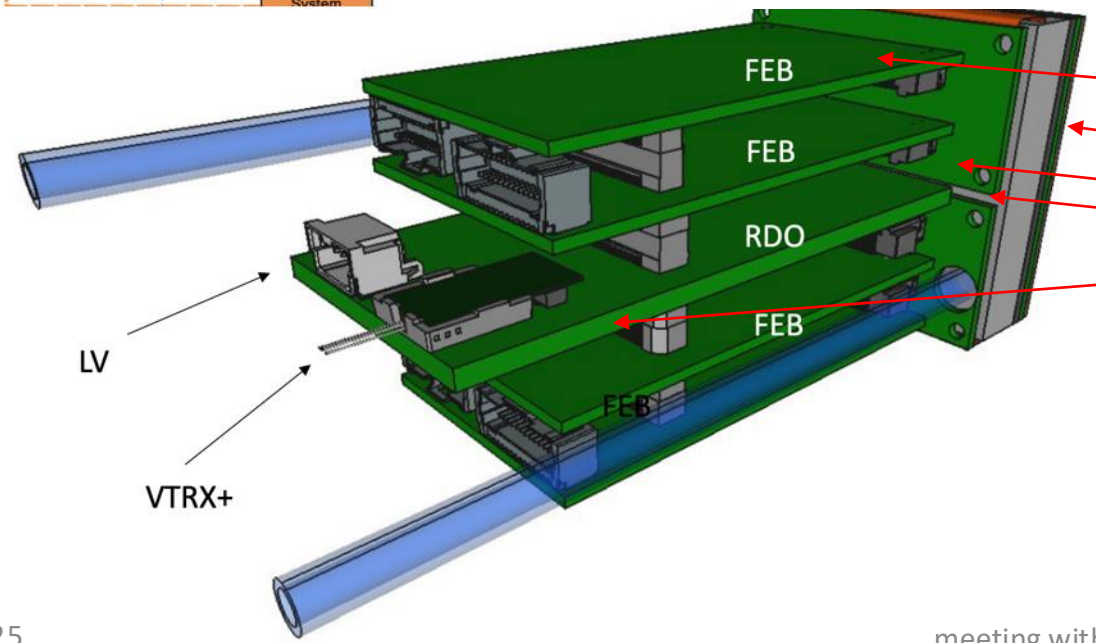
RDO/DAM role in ePIC and dRICH PDU

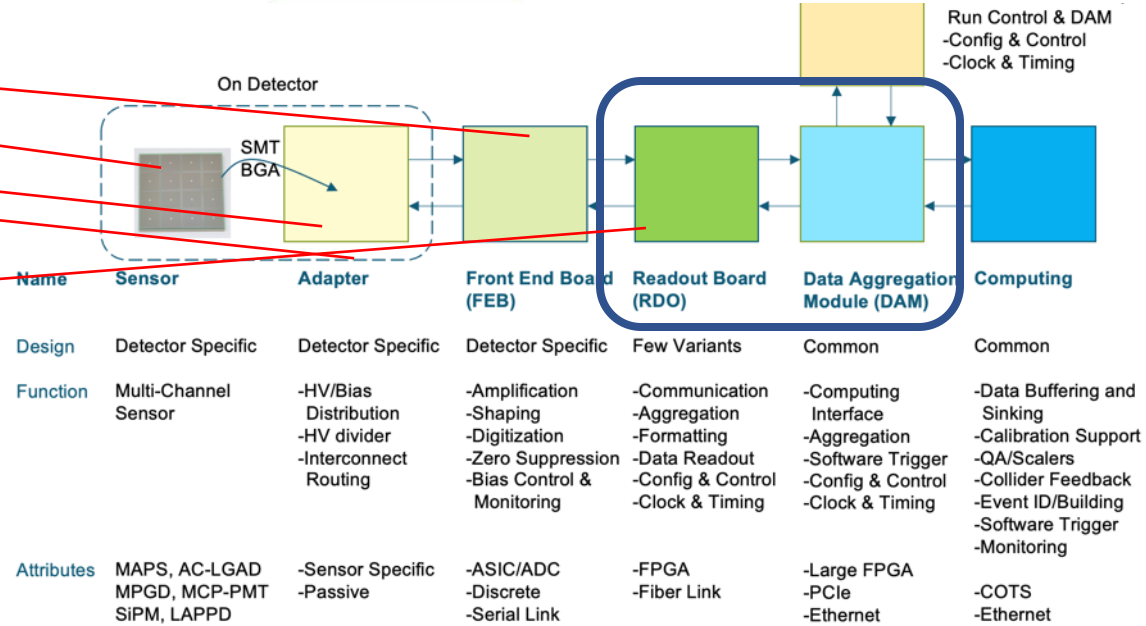
Bunch Crossing ~ 10.2 ns/98.5 MHz
Interaction Rate ~ 2 us/500 kHz
Low occupancy

front-end DAQ: RDO
back-end DAQ: DAM (FELIX card)





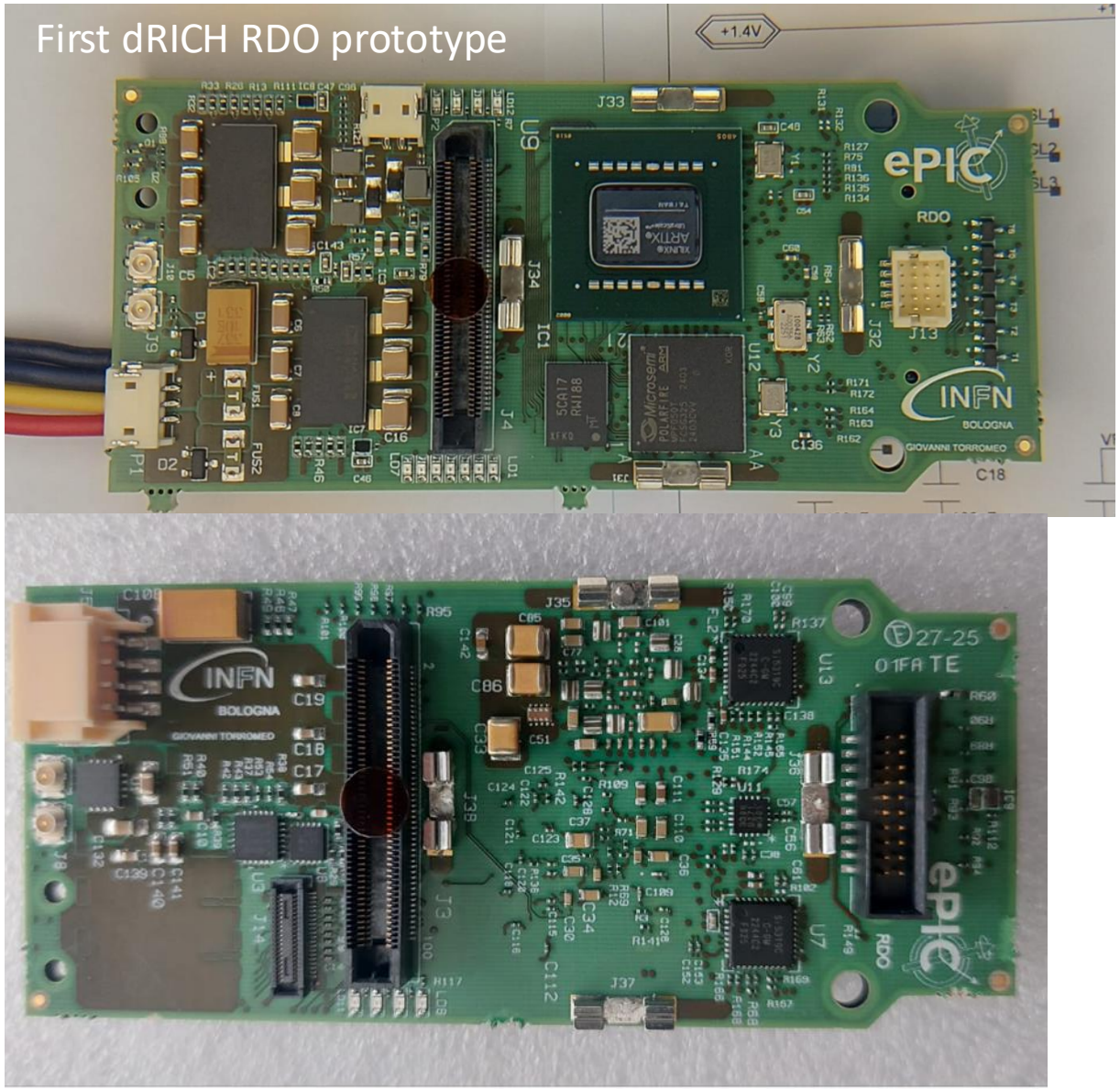




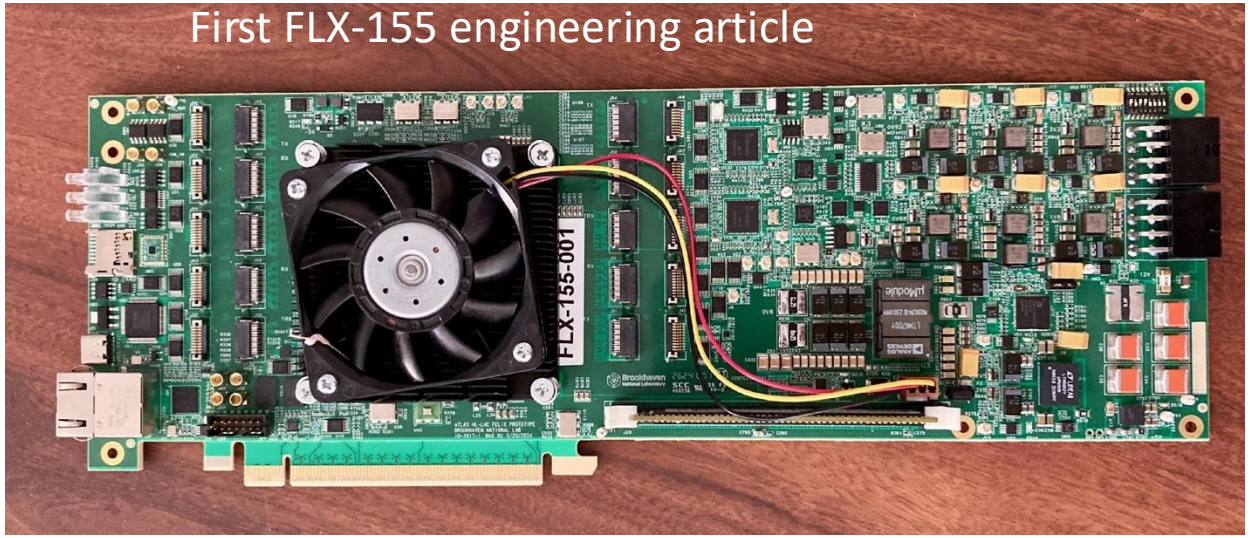
Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Design	Detector Specific	Detector Specific	Detector Specific	Few Variants	Common	Common
Function	Multi-Channel Sensor	-HV/Bias Distribution -HV divider -Interconnect Routing	-Amplification -Shaping -Digitization -Zero Suppression -Bias Control & Monitoring	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock & Timing	-Computing Interface -Aggregation -Software Trigger -Config & Control -Clock & Timing	-Data Buffering and Sinking -Calibration Support -QA/Scalers -Collider Feedback -Event ID/Building -Software Trigger -Monitoring
Attributes	MAPS, AC-LGAD MPGD, MCP-PMT SiPM, LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Ethernet	-COTS -Ethernet

RDOs and DAMs are getting real!

First dRICH RDO prototype



First FLX-155 engineering article



requirements & design choices for dRICH RDO

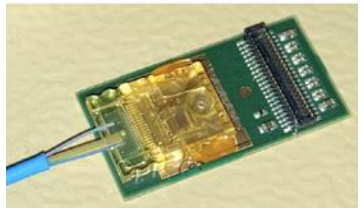
dRICH RDO requirements (from DAQ PDR review June 2024)

- **space**: 40 x 90 mm area
- RDO not accessible: **remote firmware upgrade** must be possible

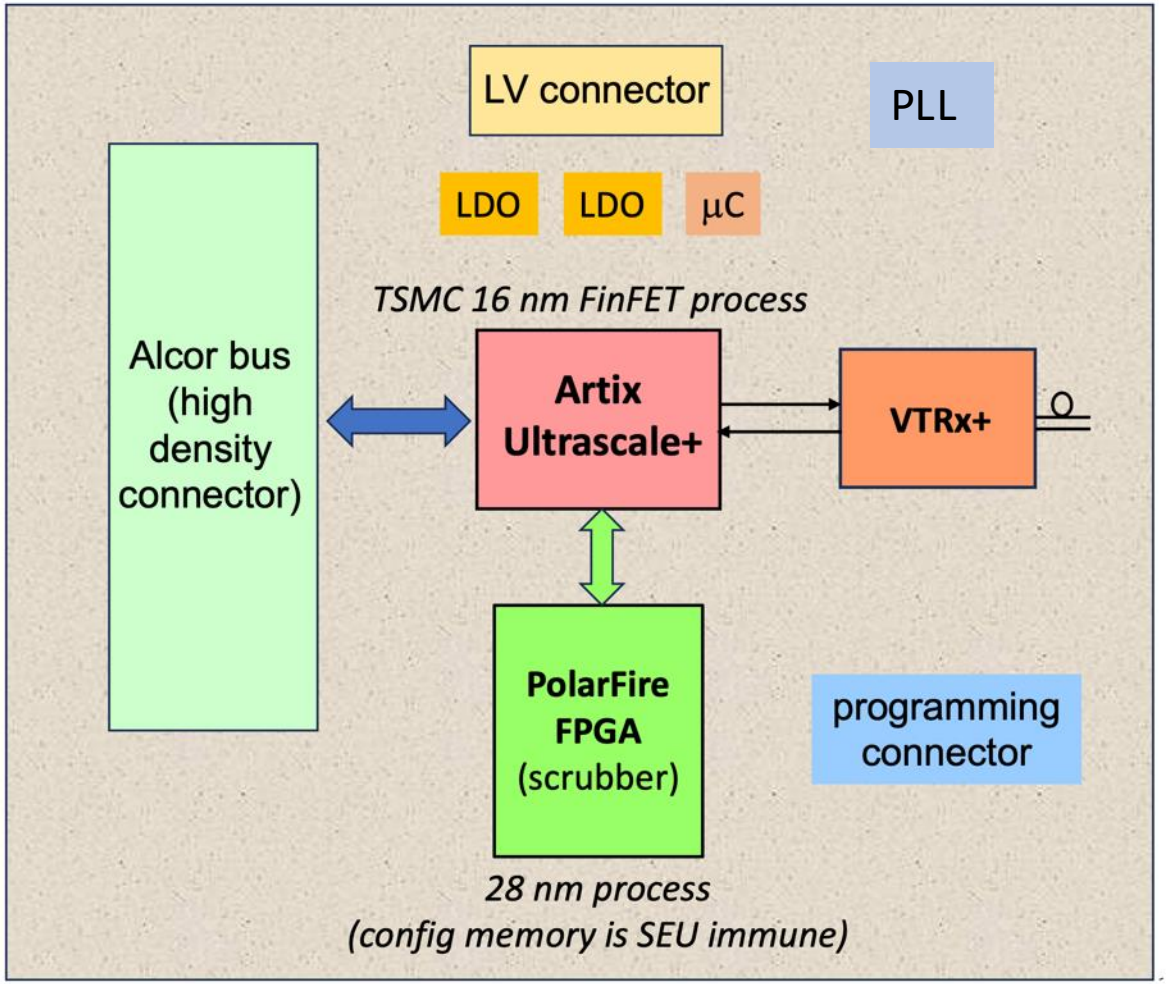
- RDO FPGA need **high speed** (“high performance”) 120 I/O pins to implement ALCOR bus (for TOP/BOTTOM FEB)
- RDO connector need high speed specs. and (minimum) 60 I/O pins each

- RDO must implement clean **clock** multiplication by factor 4 (ALCOR@394 MHz, EIC clock 98.5 MHz)
- RDO must reconstruct clock via optical link
- RDO must produce clean clock (minimize jitter)

- opt. tranceiver must minimize space/power consumption + “rad hard” and bandwitdh up to 10 Gbps (we have been the first pointing to VTRX+ in ePIC!)



requirements and design choices for dRICH RDO



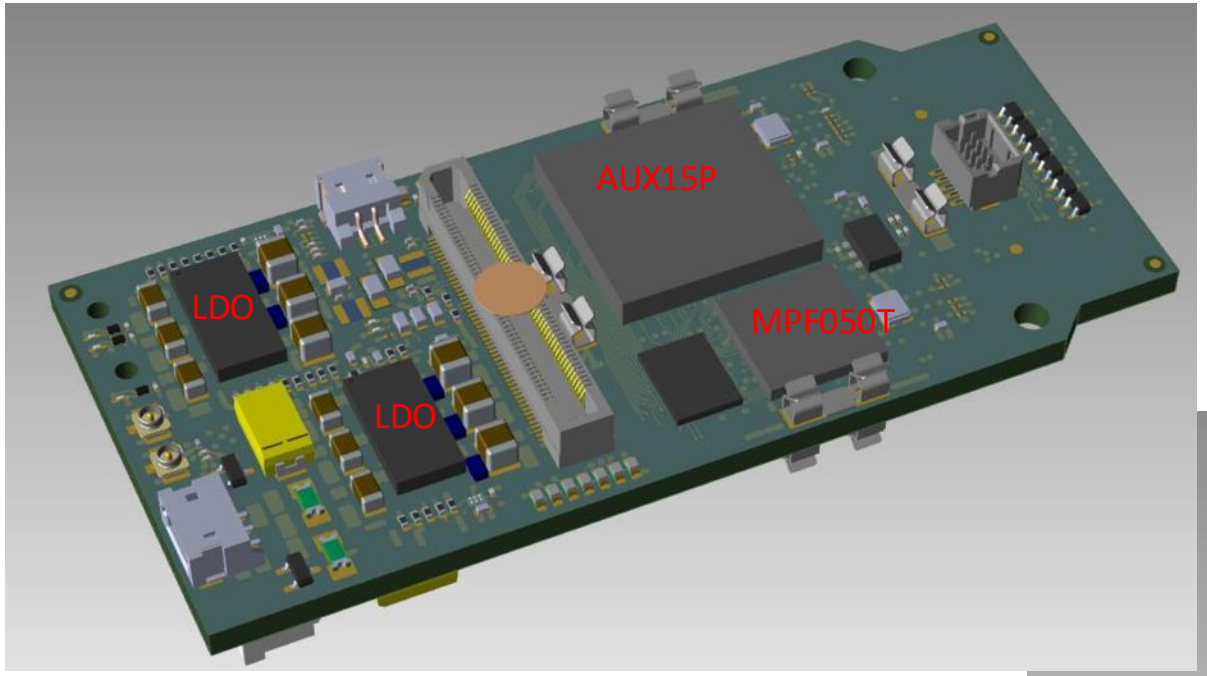
- a performing new generation FPGA (US+) + scrubbing
- devoted PLL to manage clock (SkyWorks 5319 / 5326)
- VTRX+ as optical tranceiver

Long and painful elaboration of exact RDO requirements + detailing project + components selection + layout time

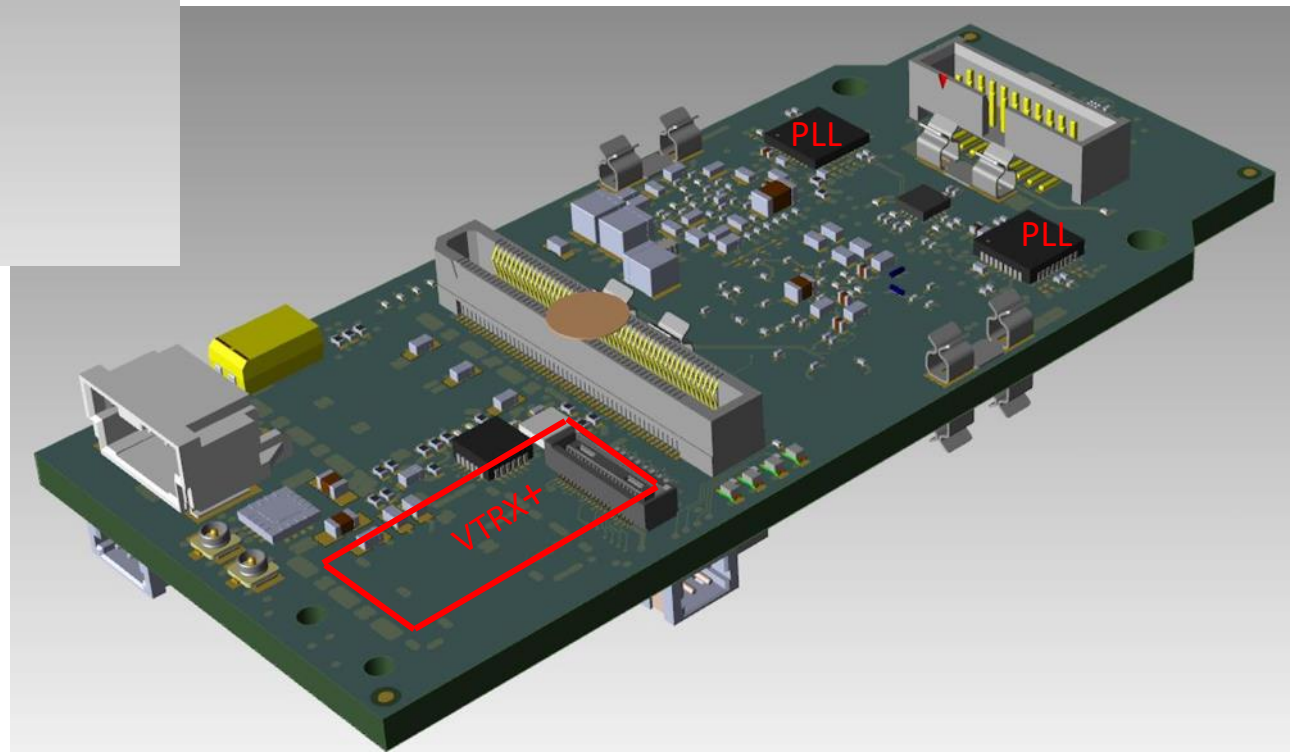
We got first 2 prototypes **yesterday!**
(1.5 year after starting the design)

Much more details on D. Falchieri's talk at Workshop on Electronics for Physics Experiment and Applications @INFN (March 2025)

dRICH RDO: layout



Complex and small card, 16 layers layout

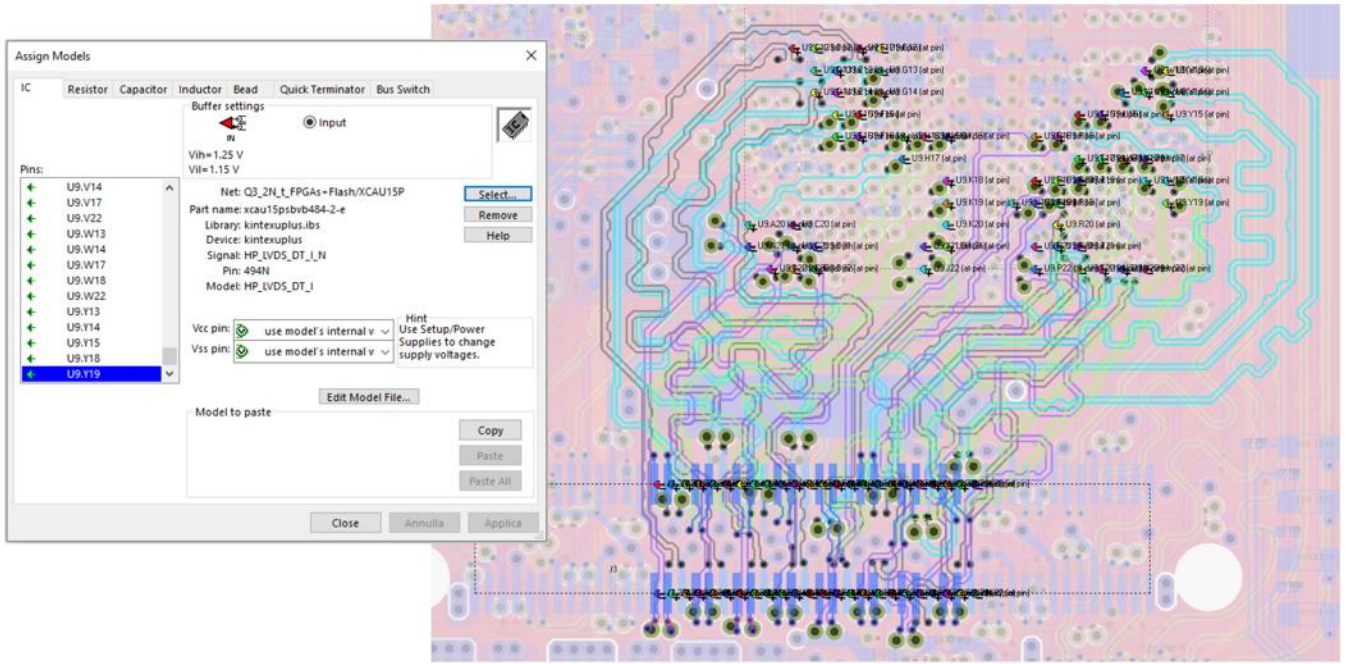


A small uC (ATTiny 417) acts as RDO power manager controlling LDOs

2025 update: a lot of work on layout and cross-checks

optimization of FPGA pin assignment vs layout

Routing of 32 lanes ALCOR bus

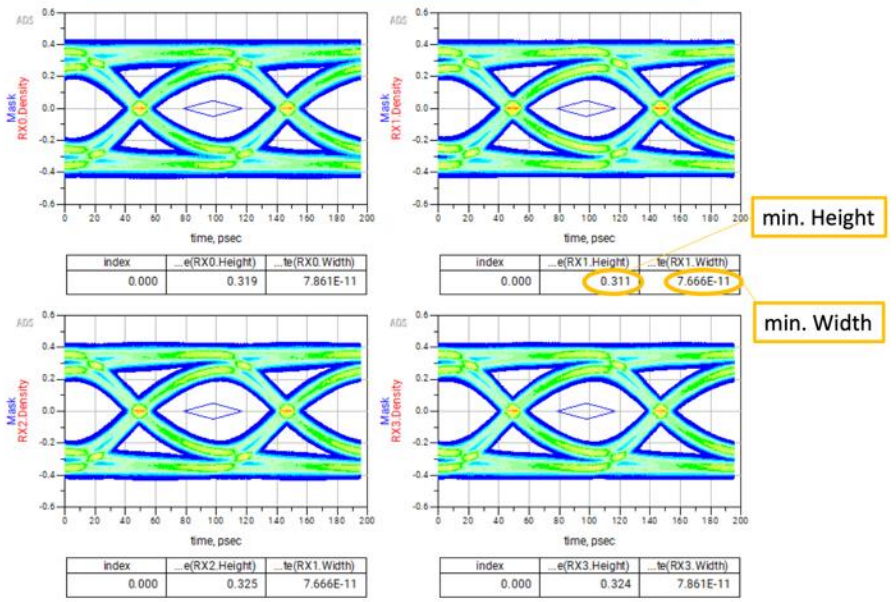


high-speed differential line modeling

ARTEL S.r.l. PCB ENGINEERING

4 Channels TX ARTIX Ultrascale+ GTH to VTRX+ receiver
AC coupling termination 100 Ω dielectric FR408HR

ADS Keysight



Much more details in D. Falchieri's presentation at WG Electronics and DAQ/eRD109 (April 2025)

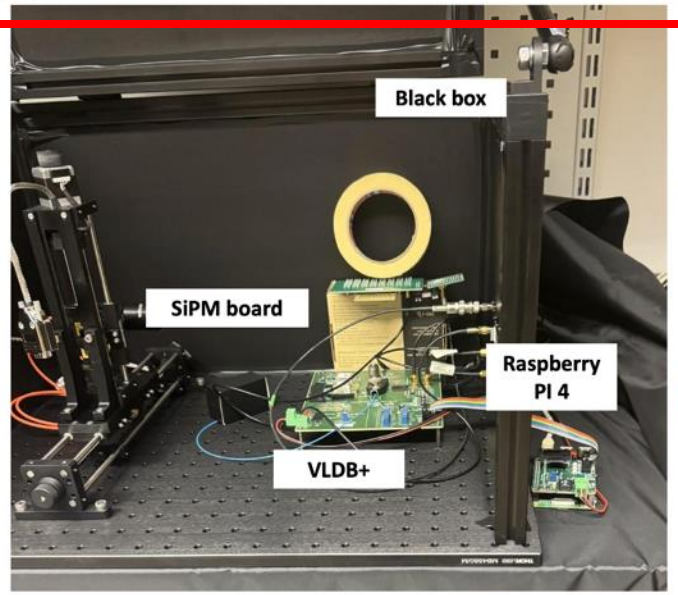
D. Falchieri, G. Torromeo

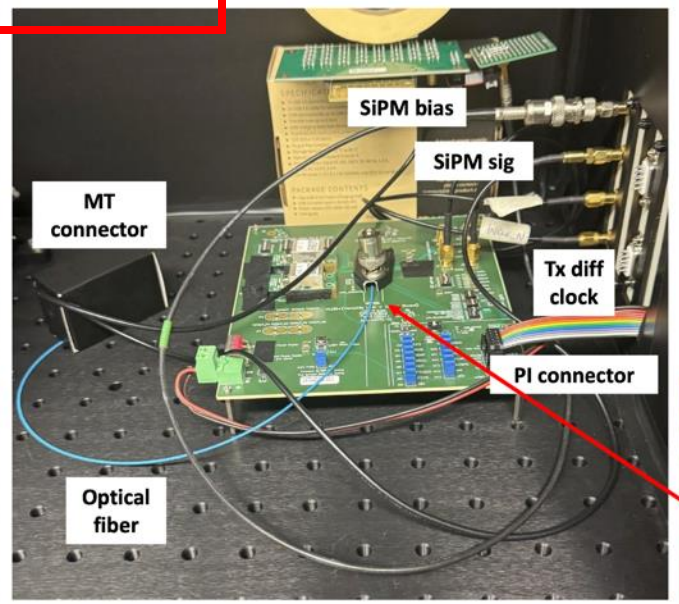
VTRx+ light + pigtail saga

VTRX+ light leakage tests

Context: LHCb colleagues told us VTRx+ has significant light leakage (from the transceiver + fiber)

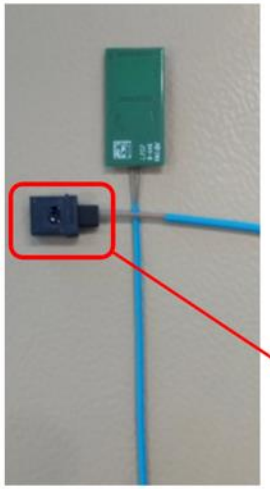
Test bench: black box + 1 SIPM

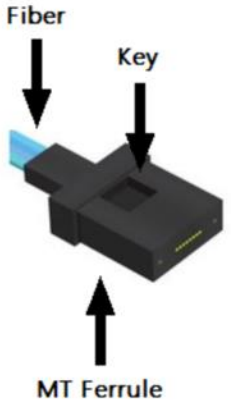


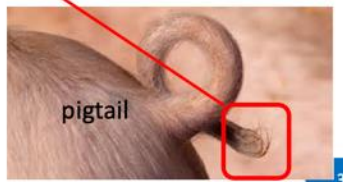


no cover of the fiber
SIPM in front of VTRX+ (not as PDU case, see next slide)
all leds of VLDB+ shielded with dark tape

"minimal" cover of VTRx+
(+ BNC adapter ;-) to keep it "tight"



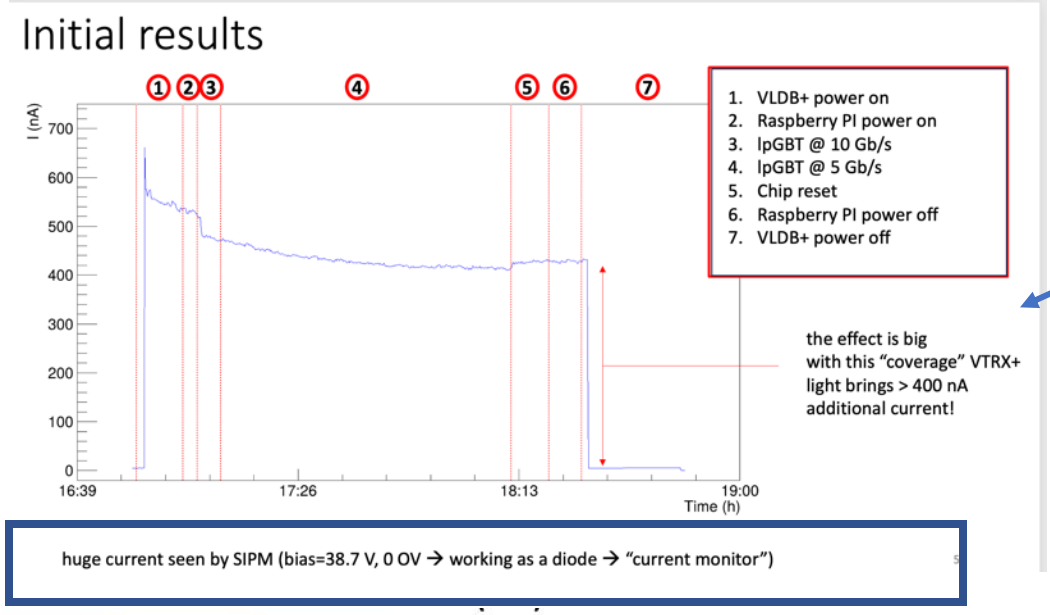




R. Preghenella/S.Geminiani/A. Paladino

More details on PA's talk at DAQ-Electronics WG/eRD109 (March 2025)

VTRx+ light + pigtail saga



Long story short:

- huge leak of light from VTRx+
- we will need to design effective shield
- initial results (room temperature only) encouraging
- and note after long debate we opted **for 20 cm pigtail length**

Additional VTRX+ plastic box + Thorlabs masking tape

→ No measurable extra-current: just 5 nA!

→ moved to 2.7 OV

With oscilloscope and measuring DCR (VLDB+ ON/OFF) we finally see:

(400.0 +- 1.8) kHz. VLDB+ ON
(398.4 +- 2.7) kHz VLDB+ OFF

(ON-OFF) = (1.9 +- 3.3) kHz

→ compatible with zero. Note that some kHz is however close to DCR @ - 30 C
→ need to move to -30 C to check

additional home-made "full VTRX+ plastic box"

Going shorter and avoid dangling?
We considered several options but for each of them the number of cons largely exceeds the pros. And if too short we can't come back. We don't have any convincing option for such scheme.

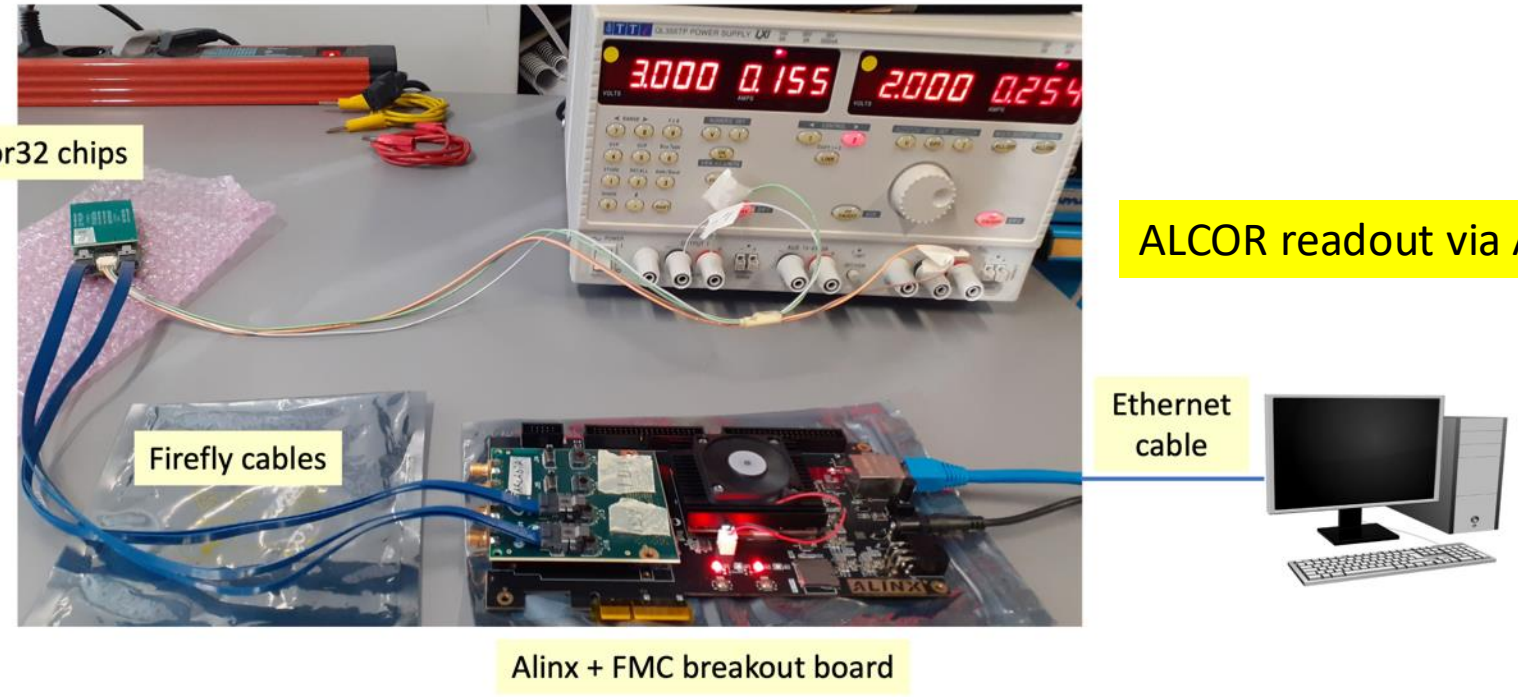
How to proceed? We go baseline
We select a 20 cm dangling pigtail
Design needs to be carefully followed up to setup proper access, secure maintenance etc. (but this is valid for almost what we are doing ;-)

dRICH option: 1500 VTRX+ with total length 20 cm

See PA's presentation at eRD109 (Feb. 2025)

RDO firmware progresses (I)

- intense use of ALINX AUX15P evb card (same FPGA) as RDO GYM (waiting for real cards!)



ALCOR readout via AUX15P

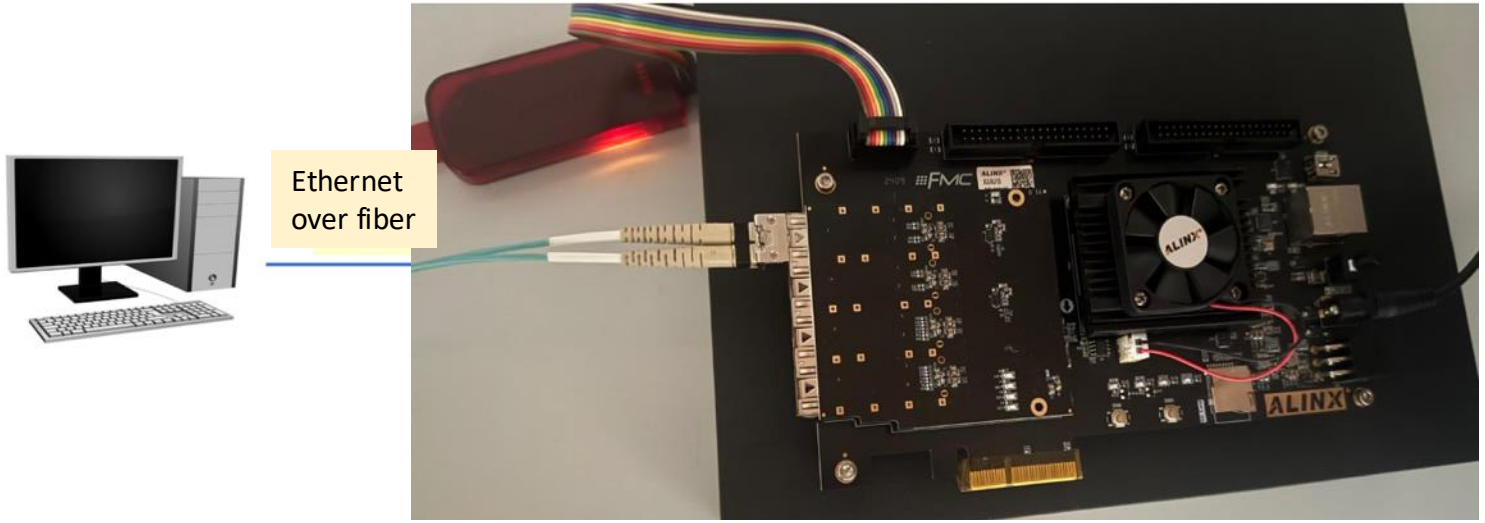
In order to test the Artix – Alcor interface, we implemented the IPbus firmware on the FPGA. Now we can program the Alcor registers via SPI and we can correctly receive the data

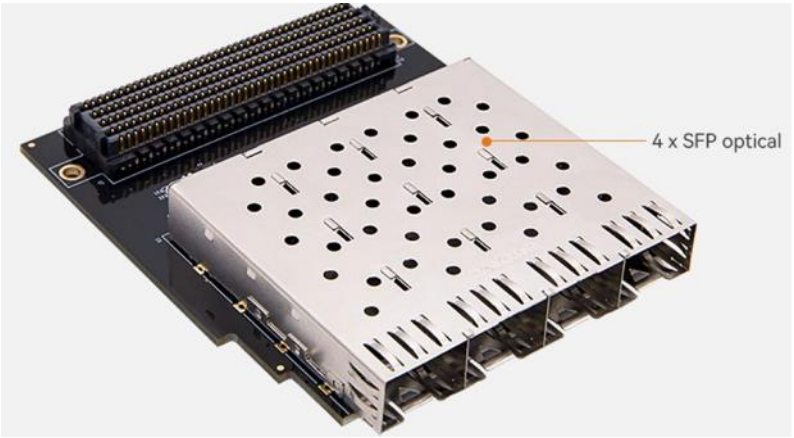
successfully ported KC705 FW (reading ALCOR) to AUX15P including SERDES
More details in D. Falchieri's talk at Electronics and DAQ WG/eRD109 (May 2025)

D. Falchieri, S. Geminiani

RDO firmware progresses (II)

- pin placement for layout design
- intense use of ALINX AUX15P evb card (same FPGA) as RDO GYM (waiting for real cards!)





successfully implemented IPBUS communication over optical link (commercial SFP), first with GBIC SFP then with fiber:
→ configuration foreseen for test beam

More details in D. Falchieri's talk at Electronics and DAQ WG/eRD109 (July 2025)

"collecting pieces of the firmware needed on RDO"

D. Falchieri, S. Geminiani

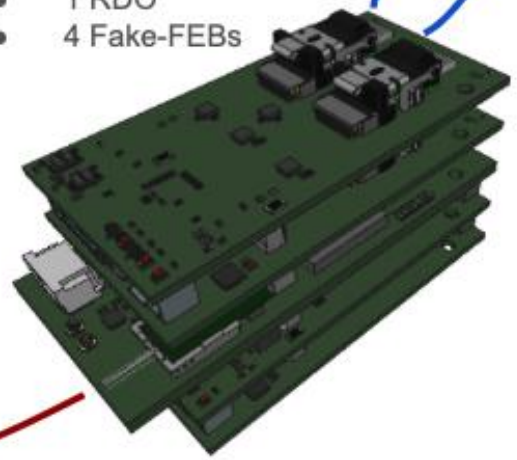
(shown last year at INFN referees)

Beam-test 2025 RDO readout architecture

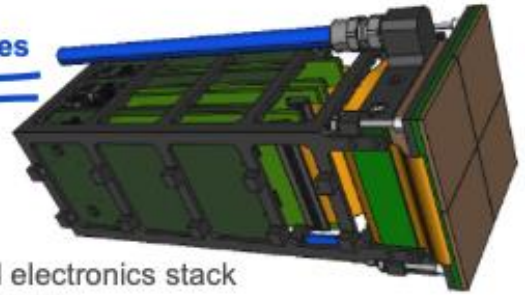
use IPbus protocol (already used) via Ethernet (SFP) to access RDO FPGA and readout ALCOR data on a **high-performance computer system**

the simplest (and likely also cheapest) way to readout RDO and 2K ALCOR SiPM channels in 2025

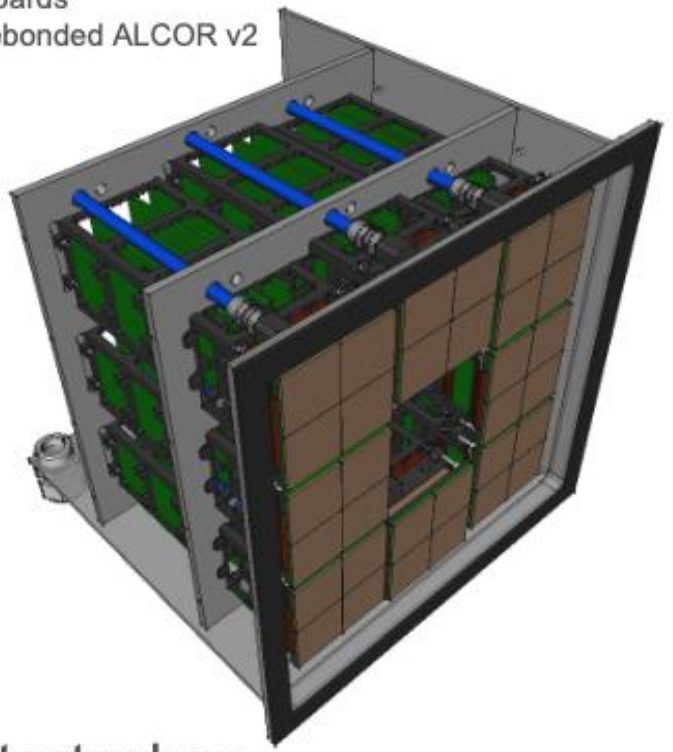
8x front-end electronics stacks each with
- 1 RDO
- 4 Fake-FEBs



8x FireFly cables



existing front-end electronics stack
4 ALCOR-dual boards
each with 2x wirebonded ALCOR v2



VTRX+ optical link to SFP

(missing! it was NDB…)

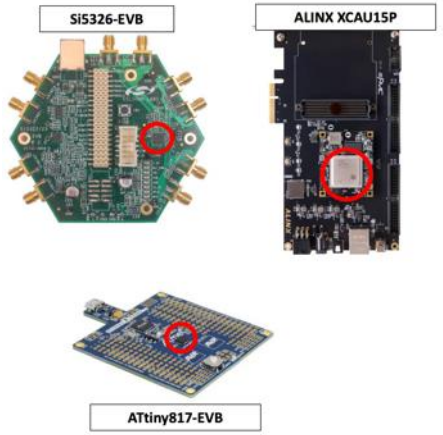
server bi-processore prestazionale con 8 link ottici SFP

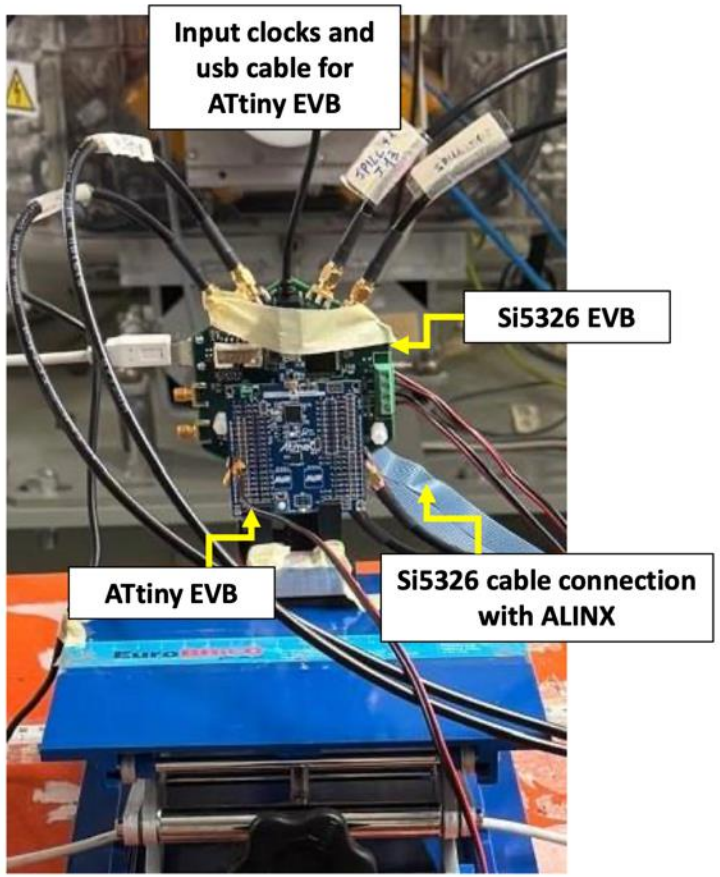
outside | inside detector box

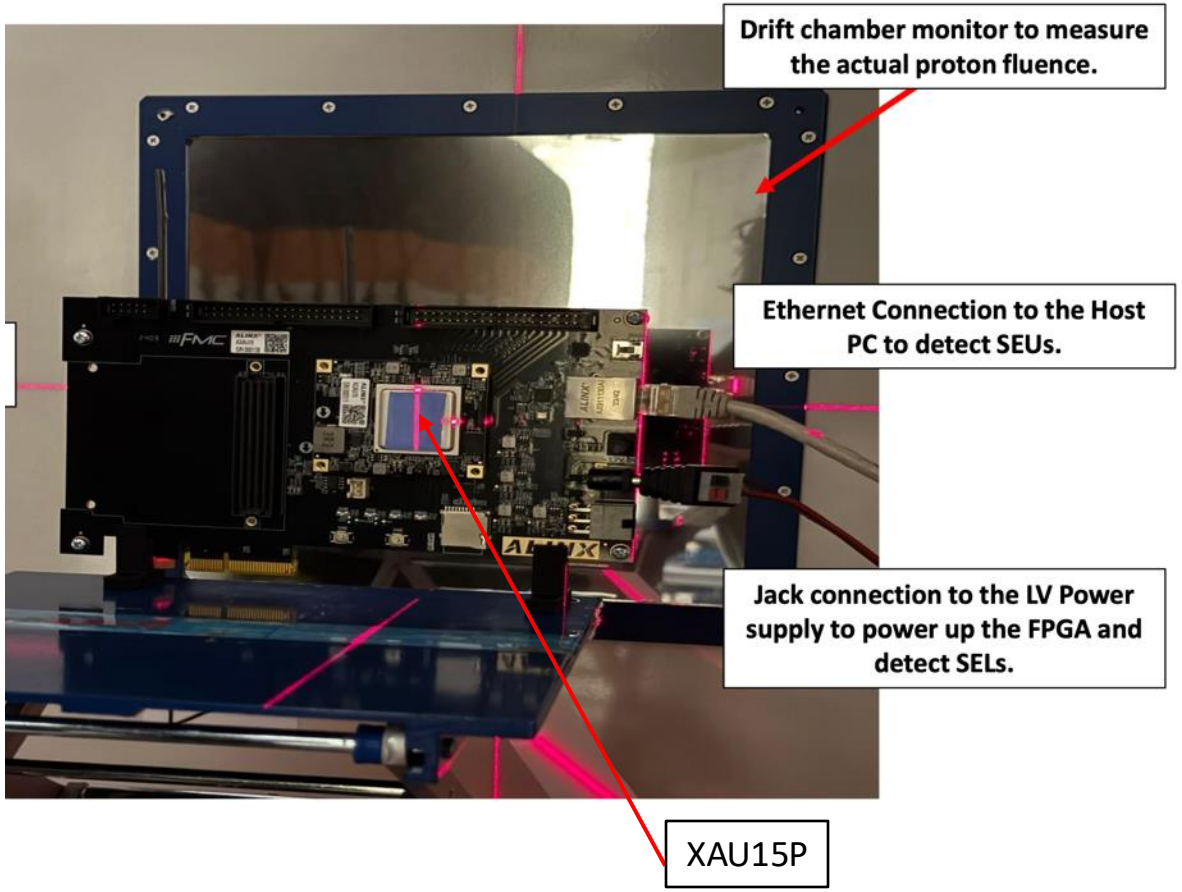
6

Irradiation tests (Dec 2024)

- Waiting for full RDO we tested several key components: PLL (Si5326), uC (ATtiny417) and AMD FPGA (AUX15P)
- irradiation with a proton beam at Centro di Protonterapia in Trento / December 2024
- TID ≅2.3 krad (1000 fb^{-1}) and Φ(h>20 MeV) ≅700 Hz/cm2 (including a safety factor 5)



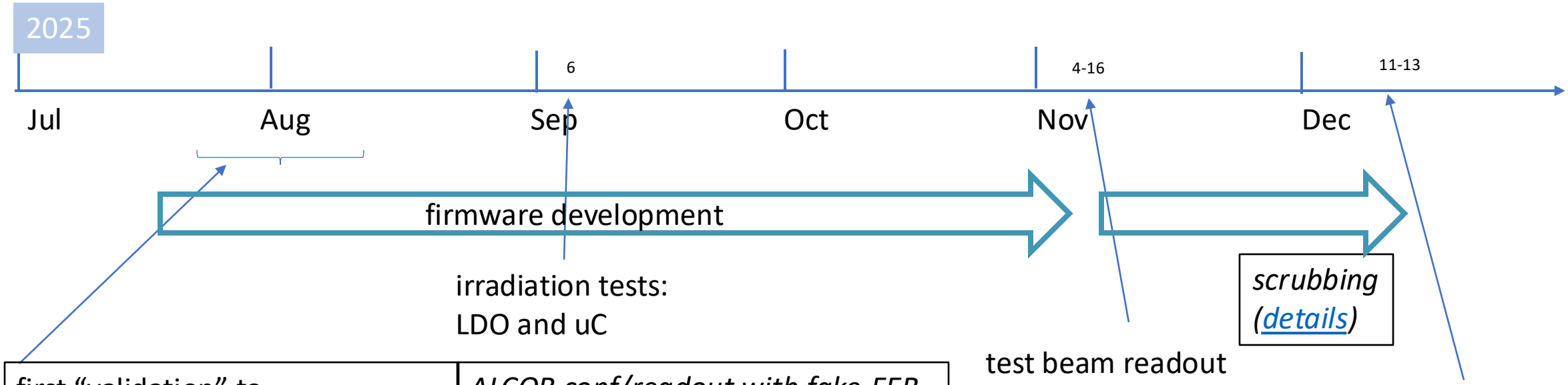




See presentation by S.Geminiani @ePIC Collaboration meeting (Jan 2025) + results in backup

investigation addendum for ATtiny + LDO test → Trento – September 2025

Plannning and validation tests (2025)



Next steps/challenges for RDO

During 2026 we need:

- full validation of current prototypes

- fix any mistake found

- design adaptations due to integration challenges that may arise (cooling, space, FPGA resources, ...)
- prove communication with DAM (implementing a FELIX-supported comm. protocol)

Irradiations (for RDO, components, SiPM…)

Why we still need irradiation tests?

- first full RDO irradiation test (Dec. 2025) will be learning exercise: it is first scrubbing test
- with firmware more advanced we need to check behaviour of the card – link stability etc.
- we will not go to CHARM in 2025 (we will free s.j. or ask to use for test beam…) but 2026 is the year to test whole PDU
- need to test ALCOR64 !
- need to irradiate a whole SiPM matrix to test then annealing in a true PDU

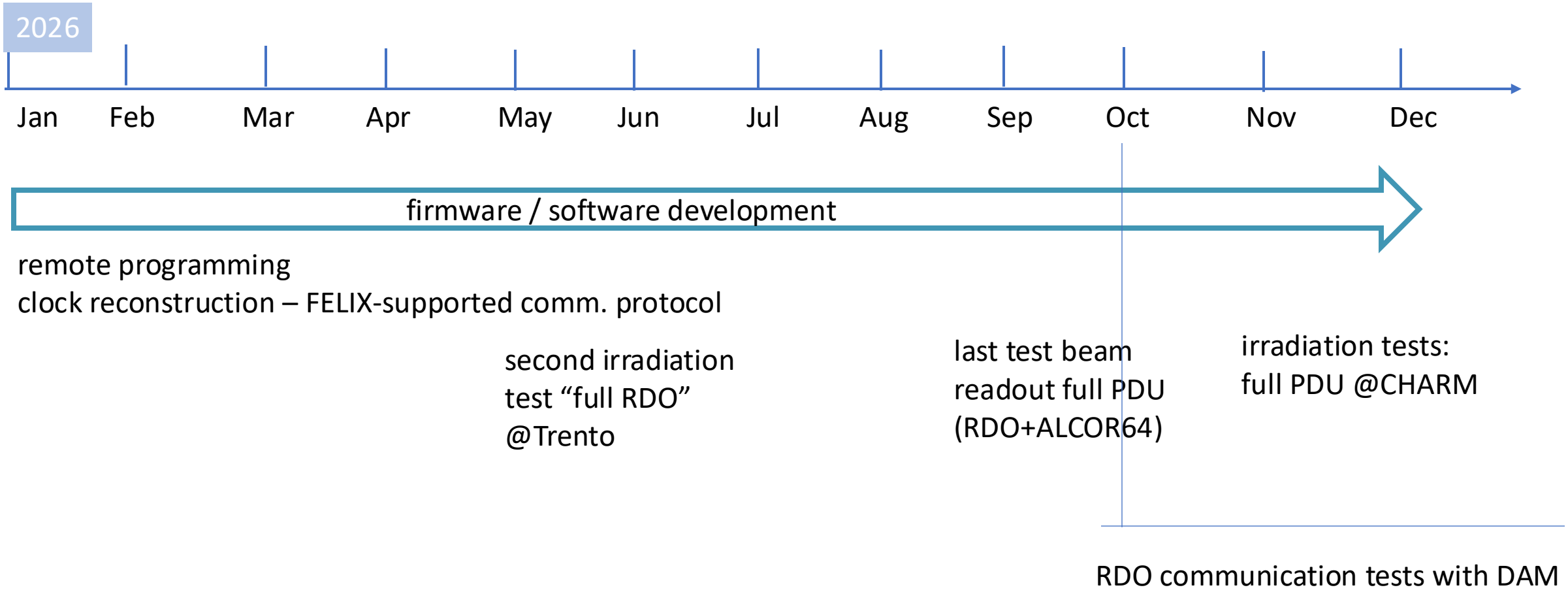
Requests

- TIFPA, 3 sessions (or 2 but extending one to three days): RDO, ALCOR64 (FEB) → **7.5 k€ (sp.servizi) + 2.5 k€ (missioni) [BO]**
- LNL, 1 session → SiPM matrix → **1.5 k€ (missioni) [BO]**
- CHARM, 1 session ("whole PDU). → **3 k€ (missioni) [BO}**
  - check "everything" plus we use a realistic mix of hadrons
  - whole PDU → we test all materials (glues, screws, connectors, etc.)
- altre sezioni → **(missioni) 2.0 k€ [FE], 3 k€ (CT), 2 k€ (CS) 2 k€ (SA)**

all requests "sub-judice"

Note: irradiation requests not covered in R. Preghenella talk, but note they are also for all the other PDU components)

Plannning and validation tests (2026)



test board to test RDO production

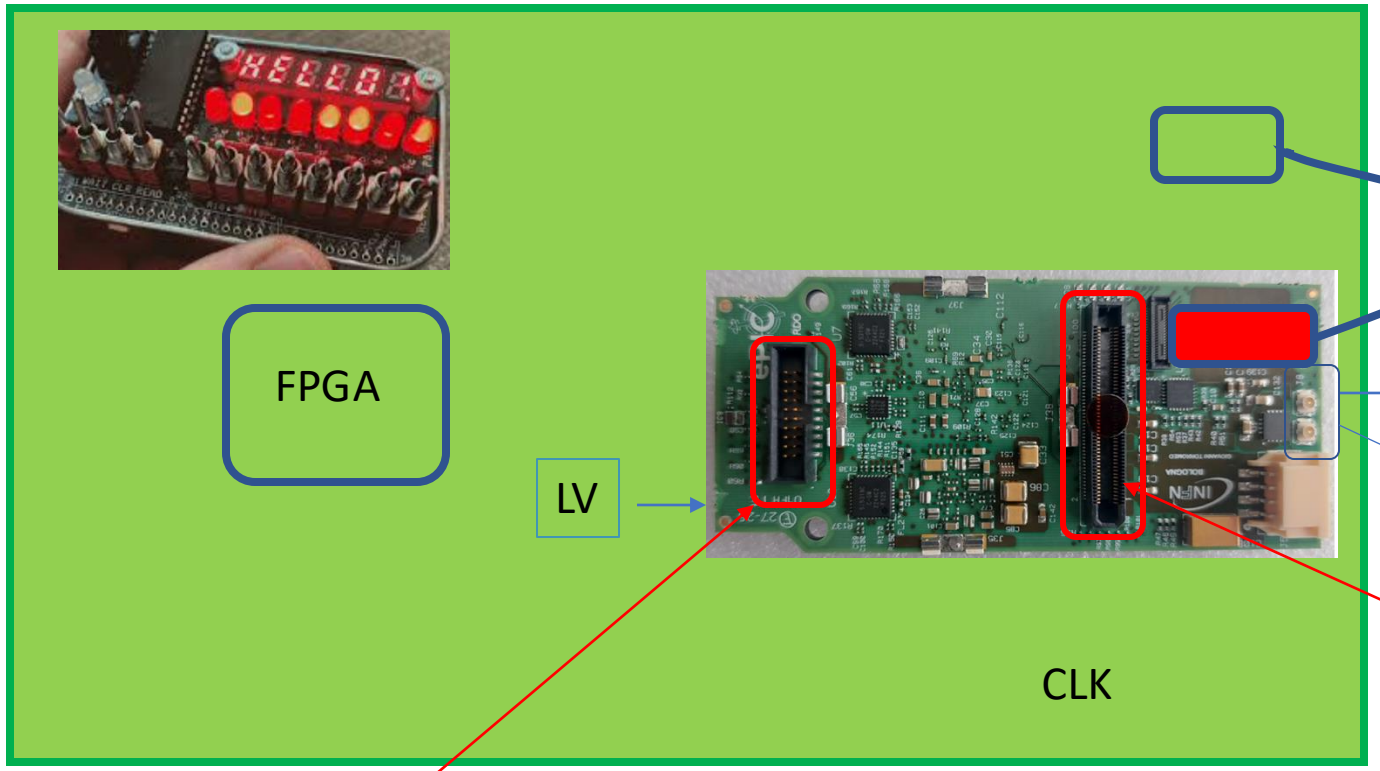
requirements | specs | design | layout and production | validation

RDO production: a RDO testbed for 1500 cards

preparing for RDO production in 2027 we will invest time preparing carefully budgeting (currently cost foreseen 680 k€ + VAT) and a **RDO testbed card** to test thoroughly, quickly and effectively the 1500 boards (and load the firmware)

display + switches to run specific tests

Request → **15 k€ (apparati)**



Basic idea:
the TB FPGA FW verifies all RDO I/Os are ok before moving to
a) VTRX+ installation – link check
b) testing with FEB
c) testing in a PDU

RDO is plugged on TB using ALCOR BUS botttom connector

EXT CLK (UFL to SMA)

a flat cable connected to (ALCOR BUS top connection)

a flat cable connected for FPGAs/atTiny programming

2026 requests (BO → frontend DAQ)

10 RDO pre-production 10 RDO → see R. Preghenella talk → **16 k€**
DAQ infrastructure DAQ (server/DAQ + pulse gen) → vedi talk R. Preghenella → **12 k€**

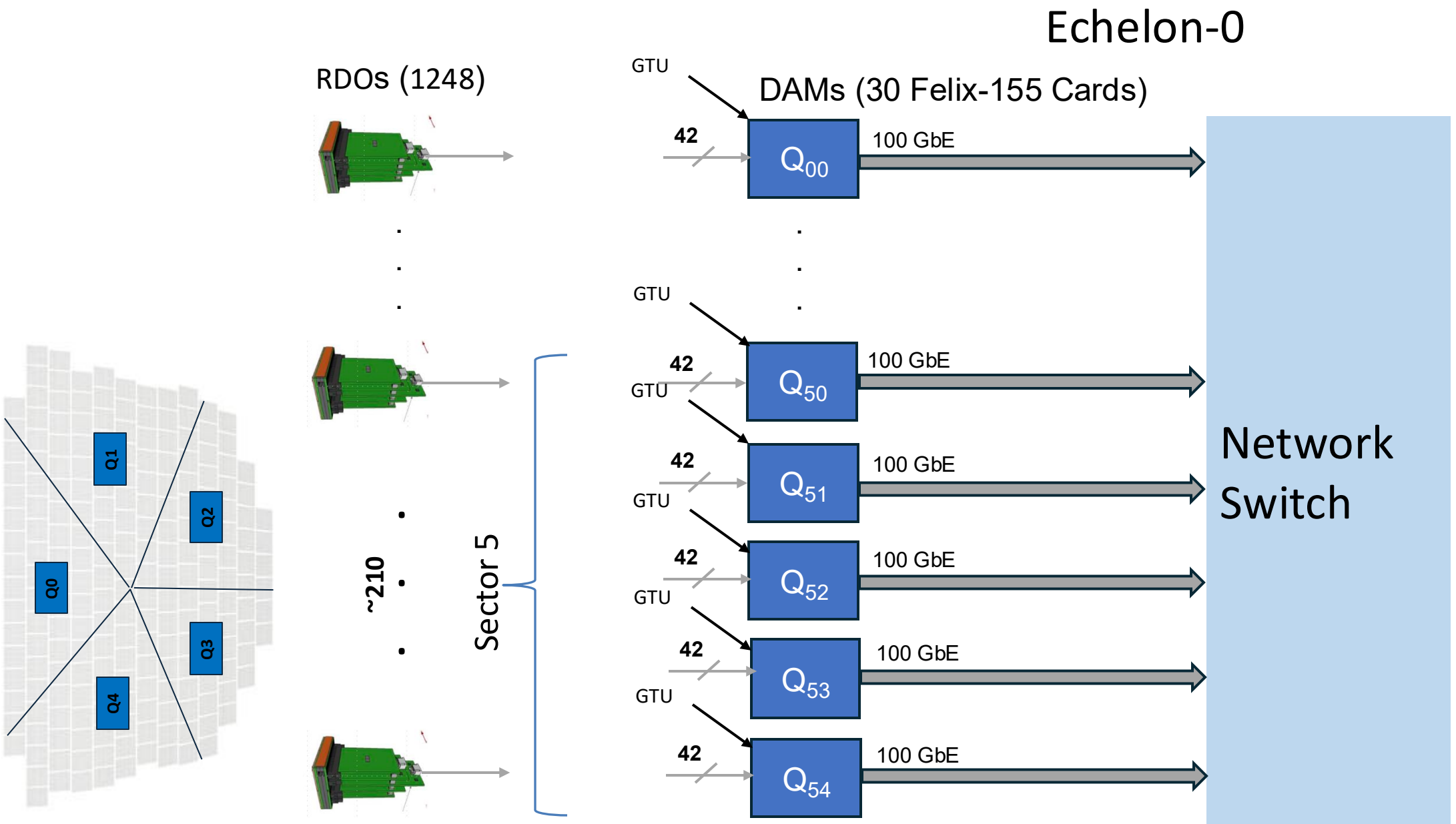
} part of PDU pre-production!

Microchip Libero Licence for PolarFire FPGA → **1 k€**
testbed for RDO (QA production validation) → **16 k€**

note part of BO missions requests for mobility in Italy is to support meetings BO-RM1

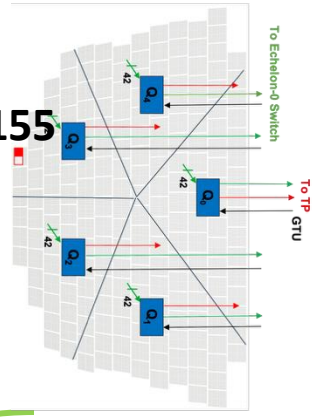
Milestone: 31/12/2026 Verifica funzionalità RDO e sviluppo firmware lettura chip ALCOR

dRICH DAQ: the backend



dRICH Data Reduction integrated in the DAQ Backend

Neural network distributed over 31 Felix-155



From PDU

Sector 0

Sector 5

To Echelon-0 switch

GTU

Trigger to DAMs

TP

Q_0 To TP 100 GbE

Q_1 To TP 100 GbE

Q_2 To TP 100 GbE

Q_3 To TP 100 GbE

Q_4 To TP 100 GbE

$Q_{0,0}$ $Q_{1,0}$ $Q_{2,0}$ $Q_{3,0}$ $Q_{4,0}$ ... $Q_{4,5}$ GTU

Trigger to DAM

TP

Communication IP

FSM

S_0 S_1 S_2 S_3 S_4 S_5

Sec NN

Sec NN

Sec NN

Sec NN

Sec NN

Aggregation MLP layer

Aggregated Sector Features

Trigger Evaluation

To TP

GTU

$Q_{0,1,2,3,}$

Communication IP

FSM

4

DAM NN

Flush

FIFo

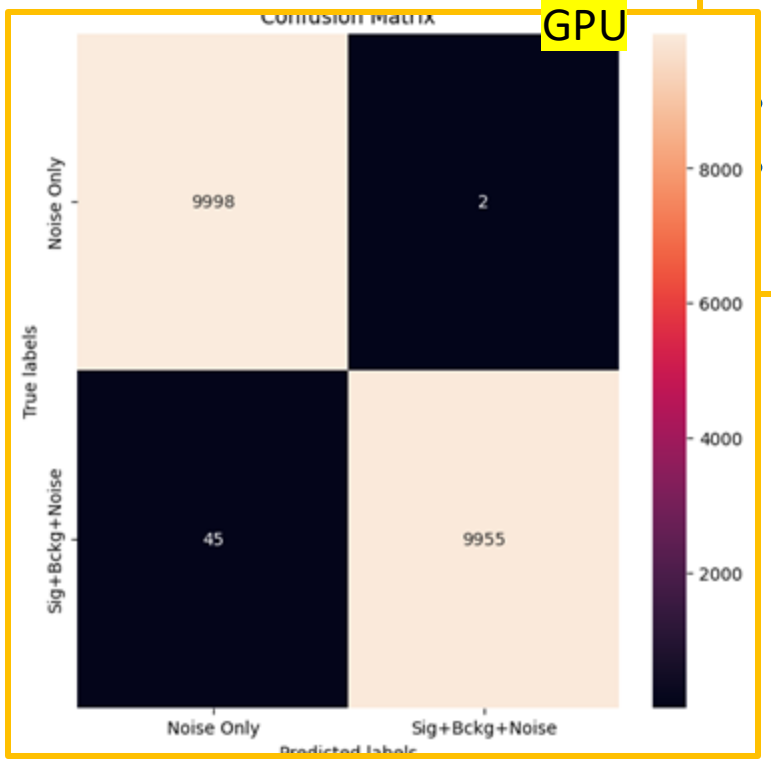
To Echelon-0 Switch

Simulation of NN performance includes parameterization of DCR background

Data Reduction performance @ luminosity = 100fb-1, time window = 10 ns

Keras model

GPU



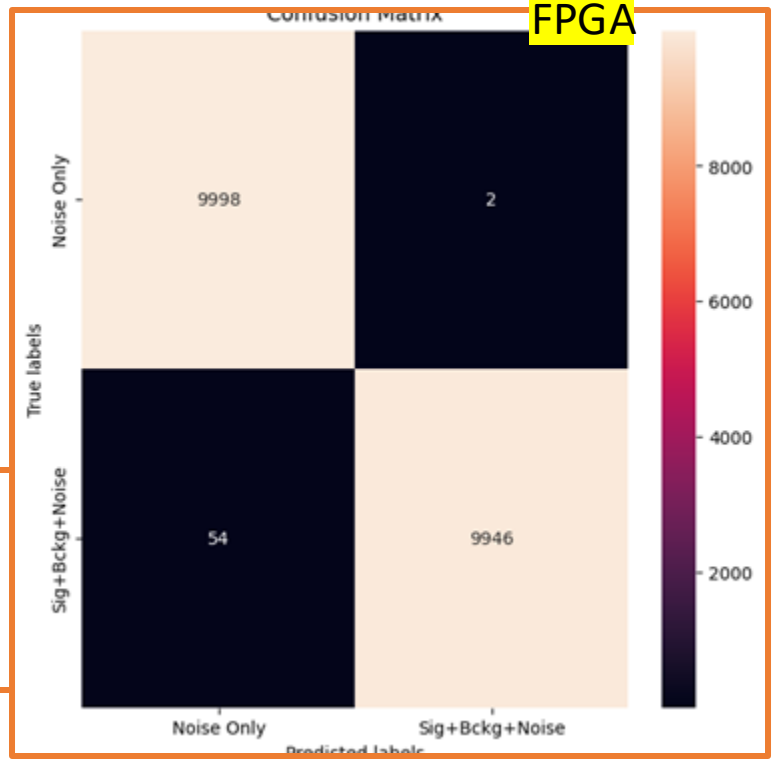
- Accuracy = (TP+TN)/(TP+TN+FP+FN) = 0.997
- Purity = TP/(TP+FP) = 0.995
- Sensitivity = TP/(TP+FN) = 0.999

Performance similar --> NN best deployed on FPGA

Model Quantization

- Inputs, Activations: fixed point<16,6>
- Weights, Biases: fixed point<8,1>

FPGA



- Accuracy = (TP+TN)/(TP+TN+FP+FN) = 0.997
- Purity = TP/(TP+FP) = 0.994
- Sensitivity = TP/(TP+FN) = 0.999

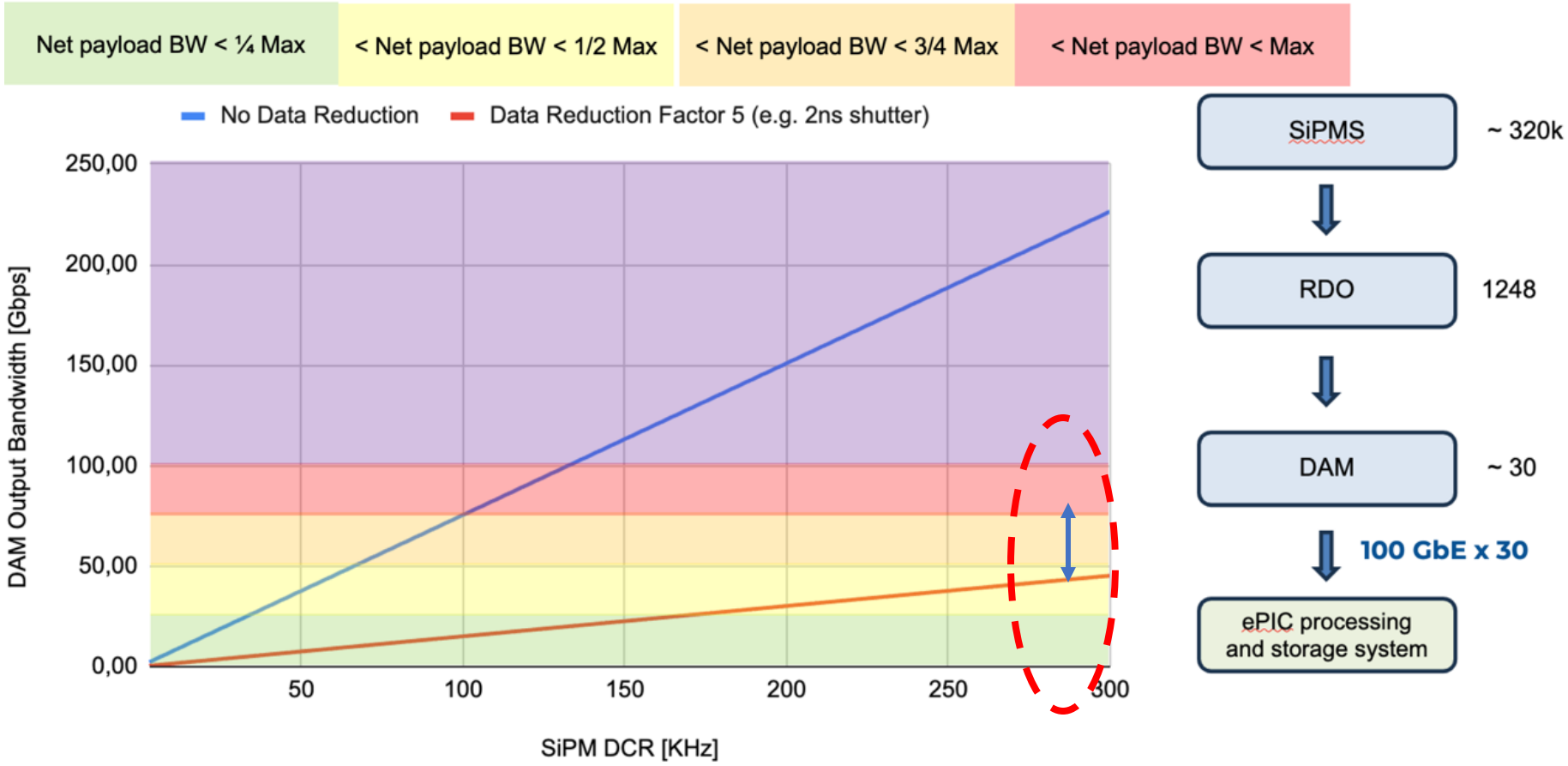
dRICH backend: data reduction (II)

→ dRICH aims to use FLX-155 resources also for data reduction

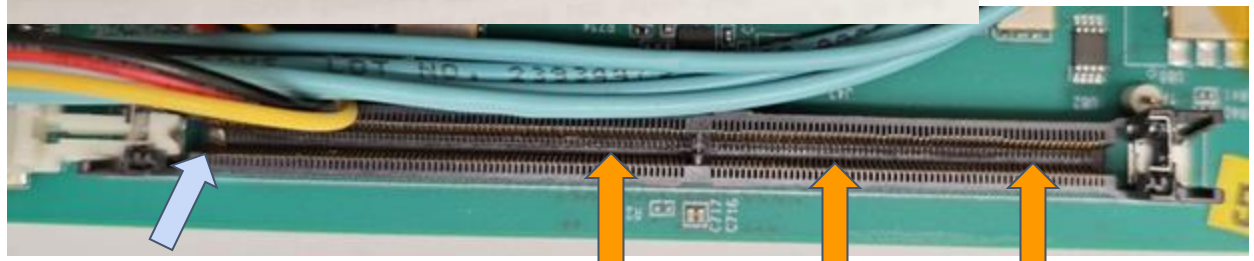
→ this will greatly help to stay away from DAM bandwidth limit

See A. Lonardo talk at ePIC Jan 2025 meeting (+ last year with referees)

Analysis of dRICH Output Bandwidth



Procurement and installation of a FLX-182

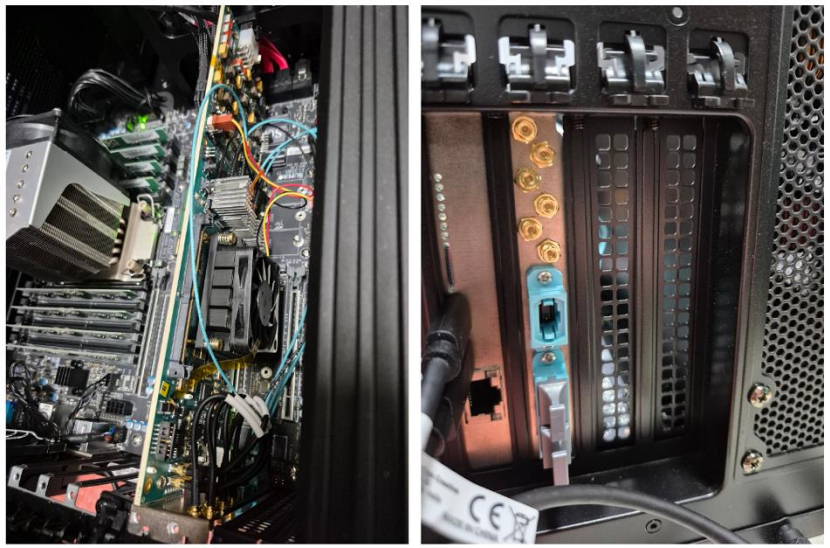


Felix-182 board on loan from Jlab arrived in Rome end of December ’24

Unfortunately it showed damages to the DRAM slot:

- **torn contact pins**
- **a crack along the inner side of the slot**

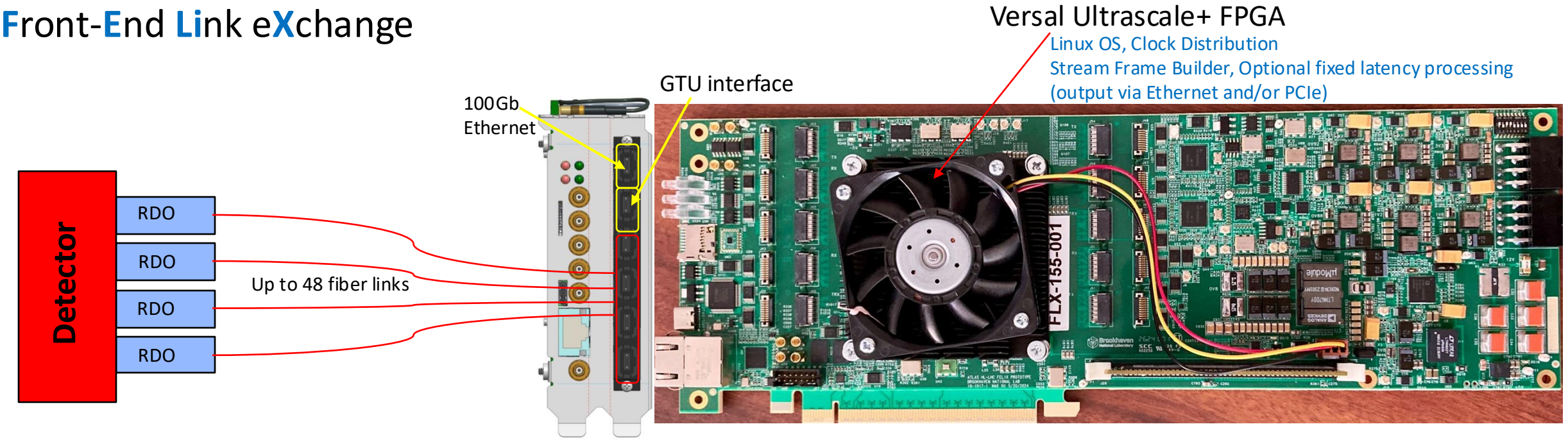
They likely occurred due to the pressure of a DRAM module left in the slot during the delivery.



Repair not possible and card didn't boot (failed DDRMC)
After many tests, workaround found: modified FW to bypass DDRMC and exclusion of ARM SoC (the one actually using DRAM)
-→ FLX-182 operational @RM1

dRICH DAQ Backend: Felix-155 Card

Front-**E**nd **L**ink e**X**change



FELIX hardware for future ATLAS experiments at HL-LHC is being developed at BNL (Omega Group)

ePIC is collaborating with Omega to use this design as our DAM board.

Initial engineering articles were tested in early 2025. Updated PCB design sent out for fabrication/population

Final design board will be tested this Fall (2025).

BNL expects to produce at least 4 boards for ePIC use after testing in Q1 2026 (for their use).

We contacted the Omega Group for the procurement, they strongly suggested us to refer to CERN (faster/easier).

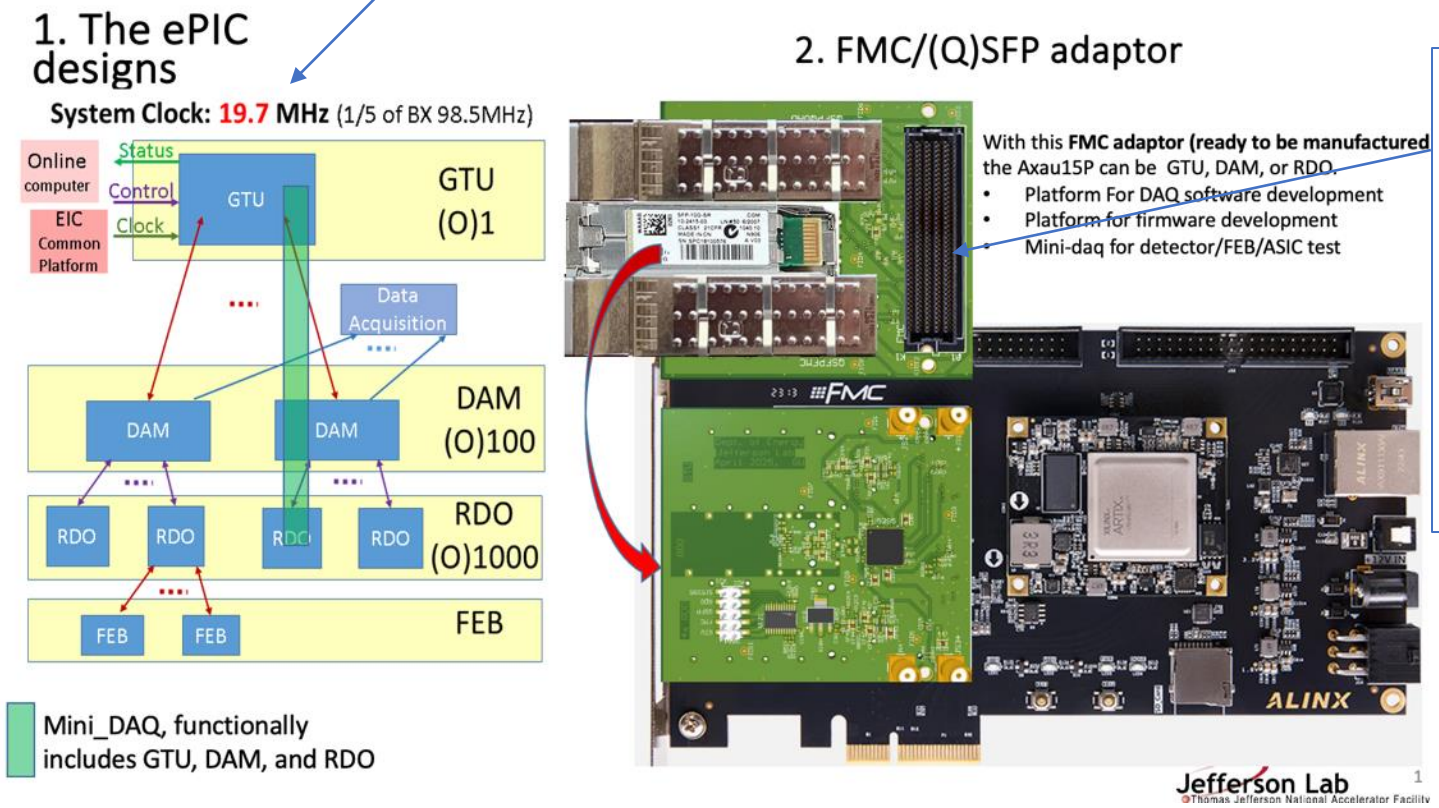
We had planned to procure one FLX-155 (and its hosting server) in 2025, CERN pre-production cards will be available only around Q2 2026 (8.5 k€ estimated cost).

Until then, we will use a Felix-182 card (previous generation) that we borrowed from JLab.

which protocol as EIC link protocol for dRICH?

this is to support detectors with lpGBT, but per se we could consider to receive a 39.4 MHz clock - close to 40.08 MHz à la LHC. This would be instead of 98.5 MHz.

This could make life easier with FELIX: we plan to use **FULL protocol (GBT on host)**



This piggy back card is produced (by JLab), this would allow us (BO/RM1) to use a pair of ALINX/AUX15P to mimic a "RDO" and a "FELIX" link

Second step: FLX-182 (Rome1) ⟷ RDO (Bo)

Third step: FLX-155 ⟷ RDO

dRICH DAQ Backend: Activity Plan & Financial Requests for 2026

PicoDAQ (Dec 2025)
Definition of the RDO-DAM communication protocol and preliminary validation tests on a dedicated testbed integrating RDO/Alinx AXAU15/FLX-182.

MicroDAQ (Sep 2026)
Demonstrate the integration of RDO and DAM (FLX-182 and possibly FLX-155 version) and GTU (if available or use emulator).

INFN – RM1

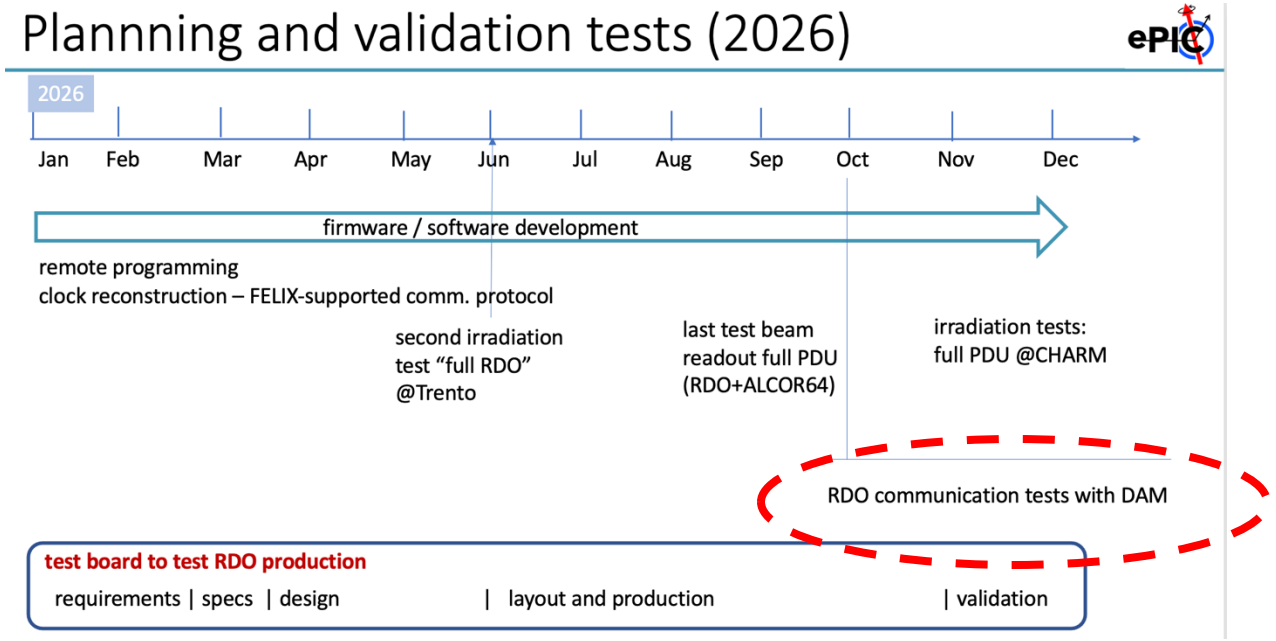
In 2025 budget we got 24k€ SJ to procure one Felix-155 and its hosting server (the expected cost of the card was overestimated compared to the actual one that was communicated to us from CERN in April)
We propose to use this budget to acquire 3 servers (1 for the Felix-182 borrowed from JLAB and 2 for the Felix-155 we would acquire in 2026), cost is about 8.5k€ for each server (we will add external funding).
In this scenario, the financial requests for 2026 regarding the DAQ backend are

- Core: 2 Felix-155 cards (**17 k€**)
- Consumable: 8 break-out cassettes MTP-LC OM4 Type A from MTP-24 to 12 LC Duplex (4x2 felix-155), 8 8 MTP-24 2mt optical cables (4x2 felix-155), LC OM4 optical cables (**4.5 k€**)

a minimum number of FLX-155 is needed to test/deploy NN on real hardware

Summary

Bologna is following frontend DAQ (RDO) and Roma1 backend DAQ (FLX-155): hardware is finally available!
dRICH frontend DAQ and backend DAQ are much closer to finally meet



Backup

which firmware flavour in ePIC FELIX ?

Flavour	Link Wrapper	Decoders	Encoders	Remarks
0: GBT	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The GBT mode flavour is available in 8 and 24 channel versions, with a complete set of encoders / decoders, and a so called SemiStatic configuration where some decoders/encoders are left out. FELIX aims to provide a 24 channel fully configurable version for FLX712, it has been demonstrated to work but with high resource count (78% LUTs)
1: FULL	ToHost FULL, FromHost GBT or LTI	FULL 8.4.15 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14 LTI-tx 8.6	The FULL mode flavour is available in 24 channels for FLX712 and FLX128. The ToHost side/decoding is using 9.6Gb/s 8b10b data without logical links. FromHost/encoding is identical to GBT, with an option to transmit a copy of the LTI-TTC link data at 9.6Gb 8b10b with additional fields for XOFF
2: LTDB	GBT	8b10b 8.4.13 HDLC 8.4.14 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	LTDB mode is a 48 channel version of GBT mode, but with reduced e-link configurability. This flavour only includes the EC and IC e-links, as well as an AUX e-link (Egroup 4, link 7) with HDLC/8b10b/Direct configuration. Additionally TTC distribution is available on all FromHost/ToFrontend e-links.
4: PIXEL	lpGBT	HDLC (EC/IC) 8.4.14 Aurora 8.4.11 TTCToHost 8.4.17 BusyToHost 8.4.18	RD53A/B 8.5.8 TTC 8.5.14 HDLC (IC/EC) 8.5.12	The Pixel flavour was designed to read out the ITk Pixel detector over lpGBT with Aurora e-links. The encoder uses a custom protocol for RD53 and includes a trigger and command state machine.
5: STRIP	lpGBT	HDLC (IC) 8.4.14 Endeavour (EC) 8.4.10 8b10b 8.4.13, 8.4.9 TTCToHost 8.4.17 BusyToHost 8.4.18	HDLC (EC) 8.5.12 Endeavour (EC) 8.5.7 LCB 8.5.9 R3L1 8.5.10	The Strip flavour was designed to read out the ITk Strip detector over lpGBT with 8b10b e-links. The encoder uses a strip custom protocol with so called trickle merge.
9: LPGBT	lpGBT	HDLC (EC/IC) 8.4.14 8b10b 8.4.13 Direct 8.4.16 TTCToHost 8.4.17 BusyToHost 8.4.18	8b10b 8.5.11 HDLC 8.5.12 Direct 8.5.13 TTC 8.5.14	The lpGBT Flavour is the lpGBT equivalent of the GBT flavour. It involves 8b10b, HDLC and TTC protocols and the aim is to have a fully configurable 24 channel build available. The LPGBT flavour will include encoding and decoding schemes for the HGTD
10: INTERLAKEN	64b67b	ToHost Interlaken, FromHost LTI 8.4.19	LTI-tx 8.6	The Interlaken Flavour has 24x 25.78125 Gb/s Interlaken links in ToHost direction. Note that no more than 12 links can be fully occupied as otherwise the PCIe Gen4 bandwidth will be saturated. As encoders, the Interlaken flavour implements the TTC-LTI encoder, a copy of the received LTI frame but with additional XOFF bits.

Table of available link “flavours” in FELIX cards and FPGA resources usage (courtesy by A. Lonardo)

FELIX FPGA resource usage

		KU115	VM1802	VP1552
GBT 24 channel	LUT	80.65%	69.60%	35.71%
	FF	77.03%	50.94%	26.13%
	BRAM	70.00%	89.45%	34.04%
	URAM		62.20%	22.14%
FULL 24 channel	LUT	52.59%	44.35%	22.75%
	FF	38.40%	33.21%	17.03%
	BRAM	40.46%	20.99%	7.99%
	URAM		62.20%	22.14%
LPGBT 24 channel	LUT	112.51%	82.94%	42.55%
	FF	52.39%	38.62%	19.81%
	BRAM	68.94%	79.52%	30.26%
	URAM		62.20%	22.14%
PIXEL 24 channel	LUT	82.40%	60.75%	31.17%
	FF	62.04%	45.74%	23.46%
	BRAM	61.20%	62.25%	23.69%
	URAM		62.20%	22.14%
STRIP 24 channel	LUT	67.04%	49.42%	25.35%
	FF	49.94%	36.81%	18.88%
	BRAM	121.43%	104.45%	39.75%
	URAM		145.14%	51.65%
INTERLAKEN 8 channel	LUT		9.15%	4.69%
	FF		7.89%	4.05%
	BRAM		40.43%	15.39%
	URAM		0.00%	0.00%

Table 5.2: Resource utilization for all firmware flavours estimated for the

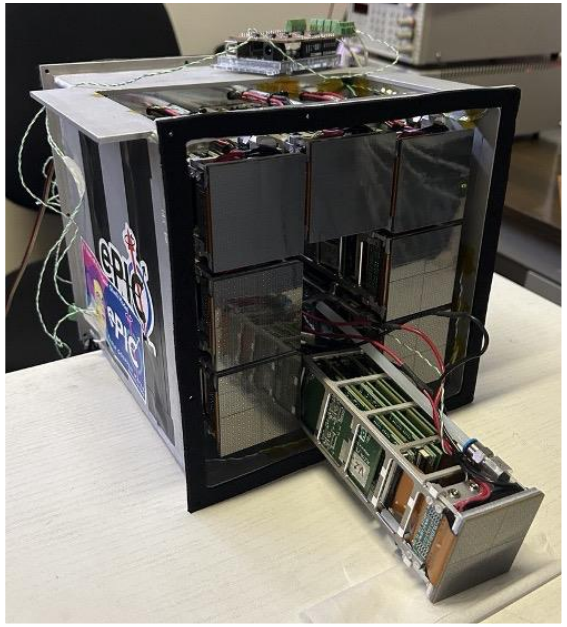
Note dRICH aims to use FLX-155 resources too for data reduction!

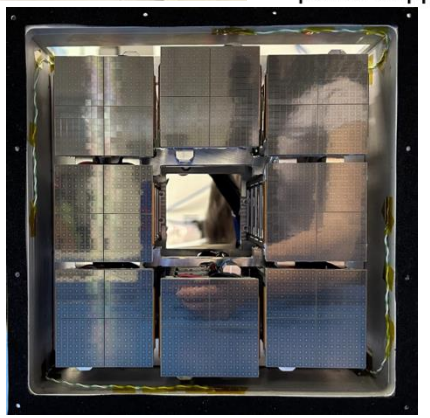
See A. Lonardo talk at ePIC Jan 2025 meeting

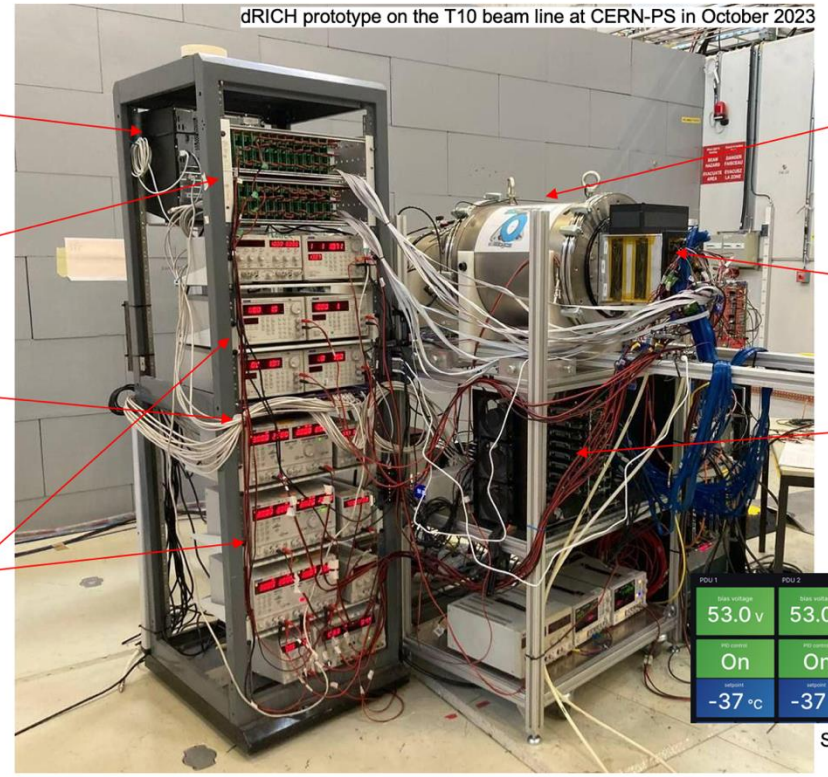
Update:
Rome1/2 has now the FLX-182 sent by BNL up and running!

- scale up to 48 lpGBT links might be a problem for FLX-155?
- as dRICH we use just the VTRX+ tranceiver not the lpGBT ASIC so lpGBT protocol not strictly needed but we would recommend to use anyway one of the existing flavour. FULL will be tested, agreement within ePIC

scale up to a test beam up to 2 kchannels







11 KC705 FPGA boards in parallel ➔ 64 AlCOR chips ➔2048 SiPMs

next step is bringing readout inside the PDU (RDO comes after)

Irradiation tests

MTBF= Mean Time Between Failure
SEU = Single Event Upset
SEL = Single Event Latchup

from conclusions presented in January:

1. We integrated $\mathbf{TID \sim 2.8 \cdot TID_5}$ for the AU15P, $\mathbf{TID \sim 10 \cdot TID_5}$ for the ATtiny and $\mathbf{TID \sim 18 \cdot TID_5}$ for the Si5326.

   No significative cumulative effect or SEL for Si5326 and AU15P, while the **ATtiny stopped working at TID = 23 krad**.

   → **Devices tested up to a TID largely exceeding expected TID @dRICH: no destructive effects seen for $\mathbf{TID \leq TID_5}$**

2. **Si5326: MTBF = 3.8 h (for 1248 RDOs)** and the jitter analysis showed the **output clock is very stable.**

   → **The RDO AU15P will control the chip configuration every t ≪ 3.8 h.**

3. **ATtiny: SRAM MTBF = 4 h** and **FLASH MTBF > 43 h (for 1248 RDOs)** .

   → **The FLASH MTBF is a safety limit and key RAM registers will be implemented with TMR checks.**

Comments: investigation addendum for ATtiny + first measurements of this kind in ePIC AFAIK

RDO next steps for go for production (8 RDOs)

1. Mechanical pairing with fake-FEB
2. Power-up : 2.5 / 1.4 jumper to avoid power to other sections
3. Prg uC via external connector
4. Power-up with uC (post-programming uC): check Vout LDO
5. Prg Artix via external connector
6. Prg Polarfire via external connector
7. Prg Artix → SkyWorks (programming 125 MHz of Si5319)
8. Check consumptions
9. Check UFL I/Os
10. Link IPBUS via VTRX+ [MT-MPO adapter + "polipo"]
11. Prg ALCOR via fake-FEB (via IPBUS → VTRX+)
12. ALCOR readout (via IPBUS → VTRX+)

Note: we can't test everything before give the "go" for next 8 RDOs...

RDO next steps for test beam

1. External clock processed by SI5326 (note: we need 16 SMA-UFL cables)
2. Readout of all I2C sensors
3. I2C programming of regulators on fake-FEB
4. Manage different IP (without jumpers)
5. Cooling ?!
6. A mini rack: 8 RDO + fake-feb on both sides etc...

Optional (bonus):

1. IPBUS + UDP streaming

RDO next steps for test @TIFPA

1. Writing QSPI Flash via SPI (writing via JTAG)
2. Scrubbing
3. Comunication between PolarFire and Artix
4. Current monitor via uC
5. Communication between uC and ARTIX

Optional (bonus):

1. Polarfire program ARTIX at boot
2. QSPI Flash writing via IPBUS (Remote Programming!)
3. During the test: one fake-feb connected and we read 2 ALCOR32? (note: ALCOR not exposed to radiation)

RDO next steps towards full ePIC DAQ

- Check noise from charged pump
- Check noise (light) from VTRX+ / engineer “shield”
- Link EIC → clock reconstruction (need project input)
- Clock at 394 MHz/ ALCOR@394 MHz
- Polarfire program Artix at boot
- Remote programming (writing PolarFire via VTRX+)
- Remote programming (writing Flash memory via VTRX+)
- IPBUS —> EIC link over VC709/707
- Data format // buffering // “frame”
- Test with ALCOR64 + FEB
- Test with FELIX
- test in magnetic field (PDU)
- PDU in detector box etc…

TB2026: dismount leds!!

- **pre-production** during 2026 (if we don't need it before) “RDO26”
- test card for testing RDO