Sviluppi di elettronica presso l'INFN di Pisa

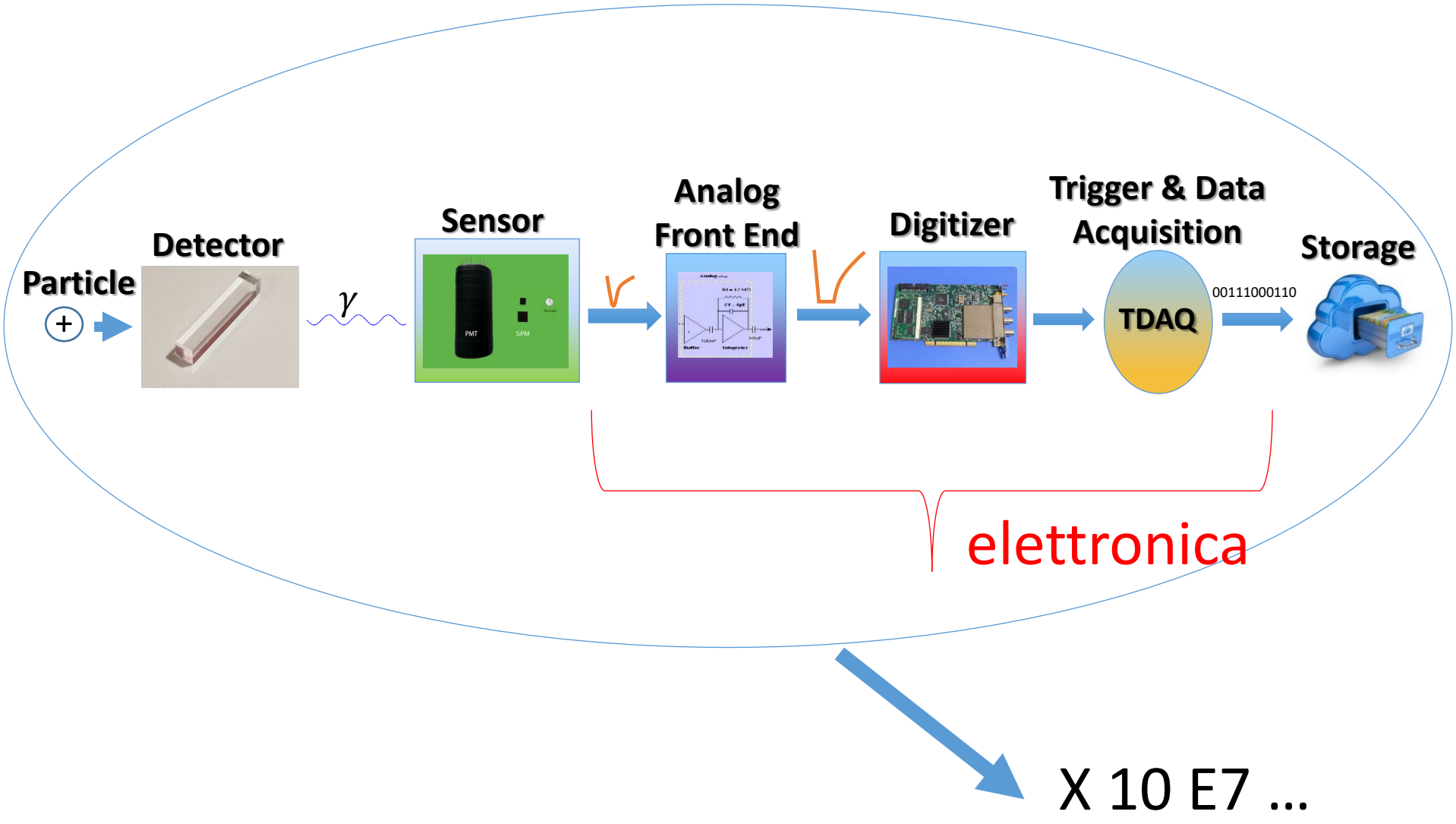
Franco Spinella

INFN Pisa

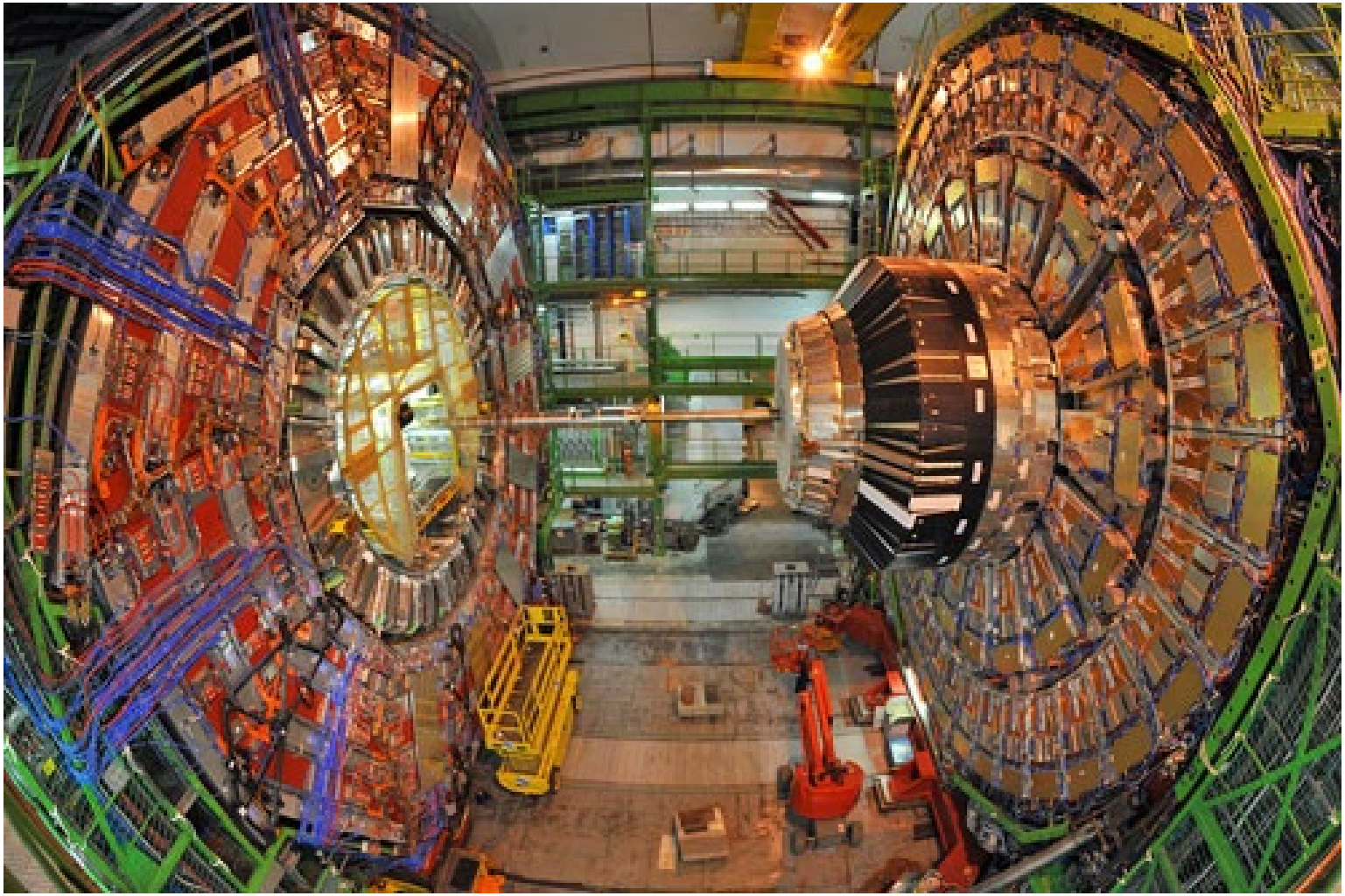
Introduzione

- L'attivita' principale dell'INFN e' lo sviluppo di rivelatori di particelle
- Implicazioni:
  - Meccanica
  - Alta tecnologia, camere pulite
  - Elettronica:
    - componenti commerciali
    - VLSI

Readout chain



CMS



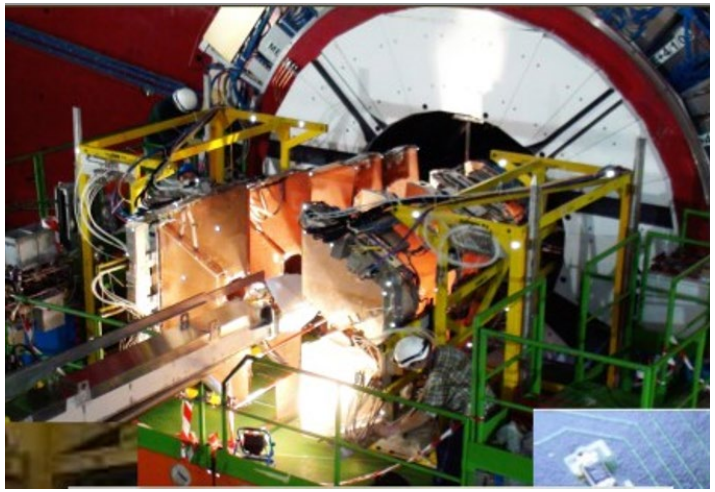
E' un mondo complicato ...

- I segnali che arrivano dai rivelatori sono piccoli e brevi
  - Elettronica analogica veloce e a bassissimo rumore (VLSI)
- Sono anche molto frequenti (es. CMS 1 ogni 25 ns)
  - Bisogna acquisirli in digitale con dispositivi velocissimi e di grande risoluzione
  - Grande flusso dati (es calorimetro di Mu2e 1 Tb/sec di dati digitalizzati in ingresso, per 3 anni di presa dati ... 100 milioni di Tb ...)
- Questi dati devono essere spostati
  - Si utilizzano gli standard delle telecomunicazioni piu' recenti (100 Gbit/sec o next-gen ethernet 400 Gbit/s)
- Lo spazio su disco e' limitato
  - Servono dispositivi e algoritmi di compressione digitale sofisticati
  - Utilizzo di FPGA allo stato dell'arte

Anzi complicatissimo …

- Elettronica e’ spesso posizionata in ambienti estremi

Spazio

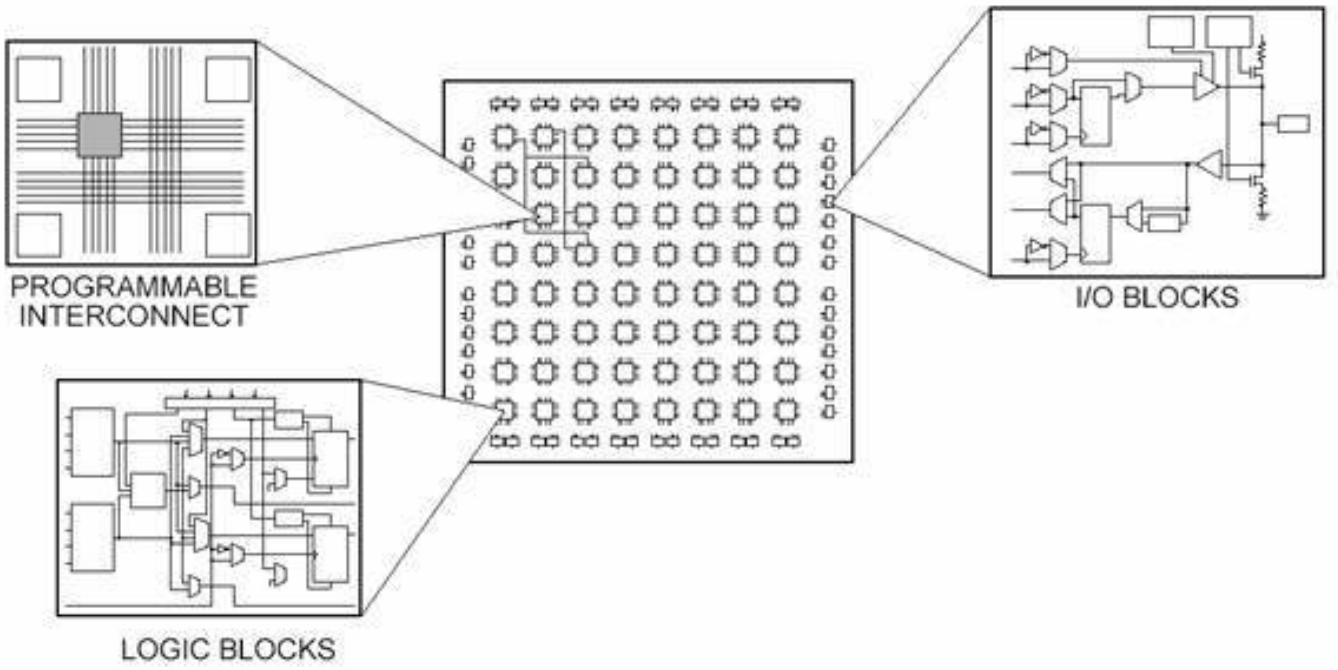


Acceleratori

- Radiazione ionizzante e non (100 Krad – 100 Mrad)
- Ioni cosmici super energetici
- Campo magnetico (1 T -> 4 T)
- Operazione in vuoto (dissipazione termica)
- Progettazione in alta affidabilita’

Field Programmable Gate Array

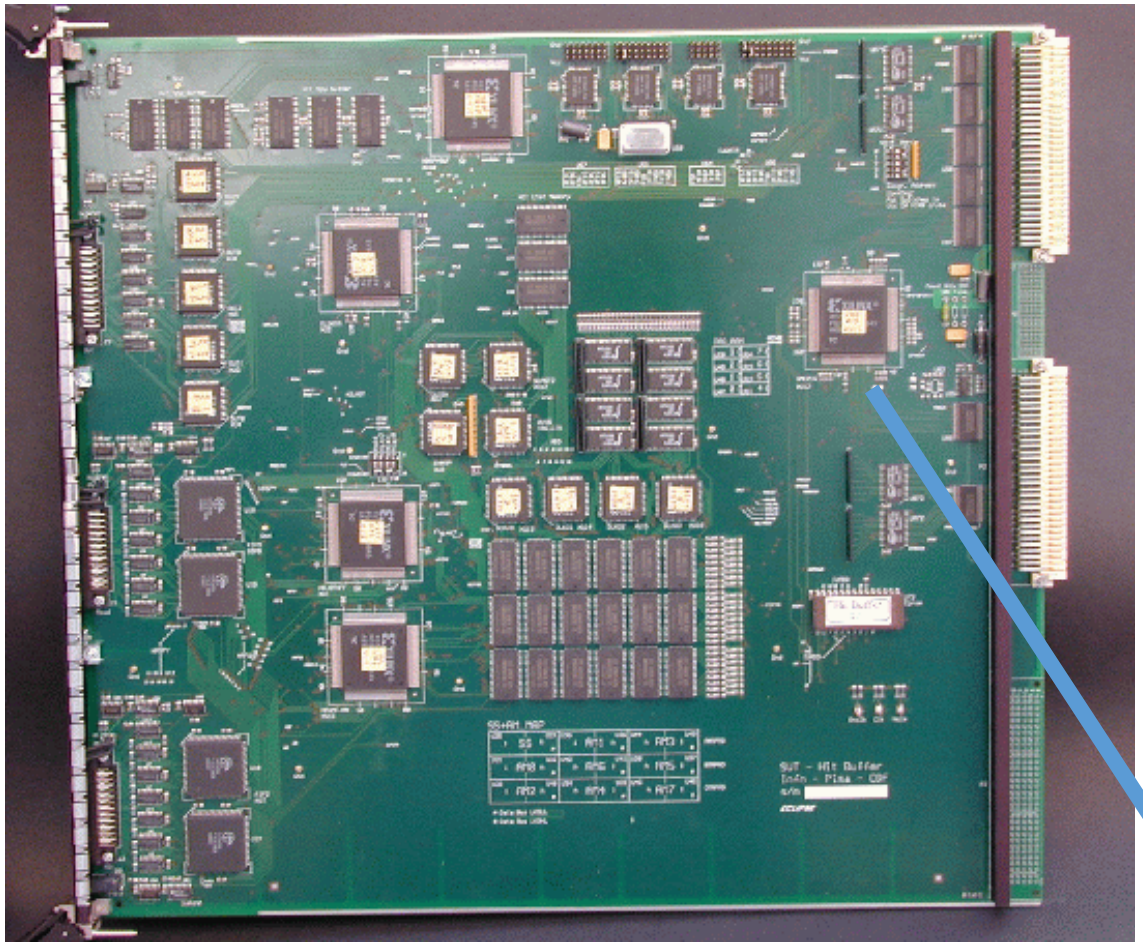
- Dispositivi di logica programmabile ... L'INFN e' stato fra i primi ad utilizzarle in Italia (1990)



Vari vendors (tutti utilizzati da INFN-Pisa):
Altera (Intel), Xilinx, Microsemi – Actel

Radiation Tolerant

FPGA 1994



Esperimento CDF , scheda Hit Buffer

Università degli Studi di Pisa

Facoltà di
Scienze Matematiche Fisiche e Naturali
Corso di Laurea in Fisica

Anno Accademico 1994/1995

Tesi di Laurea:

Progetto e simulazione di un dispositivo di tracciatura in tempo reale per un rivelatore di vertice ad un collider protone-antiprotone

Relatore:
Dott. S.Belforte

Candidato:
Franco Spinella

Controrelatori:

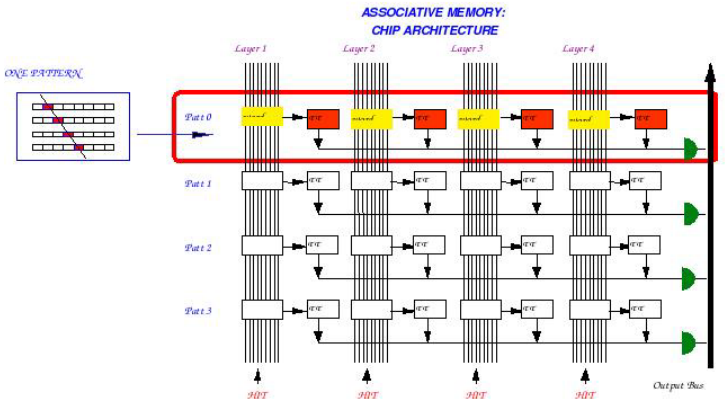
Prof. F.Forti

Prof. M.Morganti

128 gate equivalenti …

Trigger ATLAS PRM:

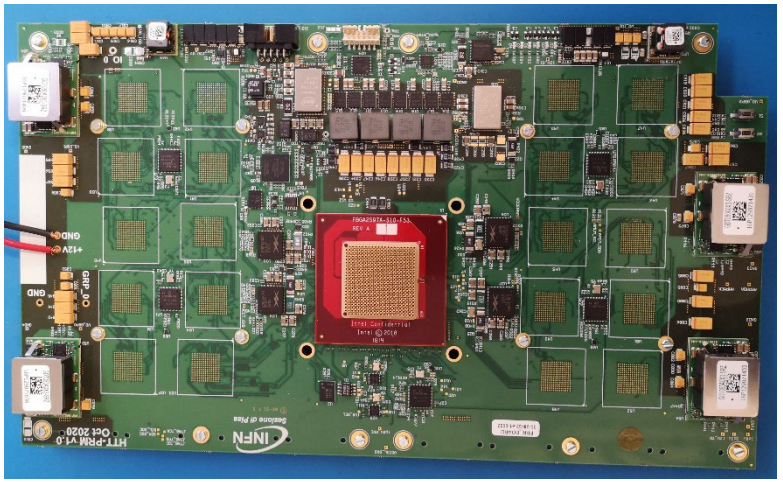
- La piu' moderna applicazione delle memorie associative...
- Utilizzata a Pisa per la prima volta oltre 30 anni fa ...
- Si basa sul riconoscimento di tracce (pattern) a partire da banche dati pre-calcolate (apprendimento) -> e' una applicazione di IA



1995

- 16384 pattern, 40 MHz clock
- 1 AM chip VLSI 128 pattern
- 1 FPGA xlinx 7000, 128 celle

2025



- 7.7 M pattern
- 1 AM chip VLSI 400000 pattern
- FPGA, Intel Stratix 10, 10°6 cells
- Throughput 140 Gbit/sec

Esperimento Meg

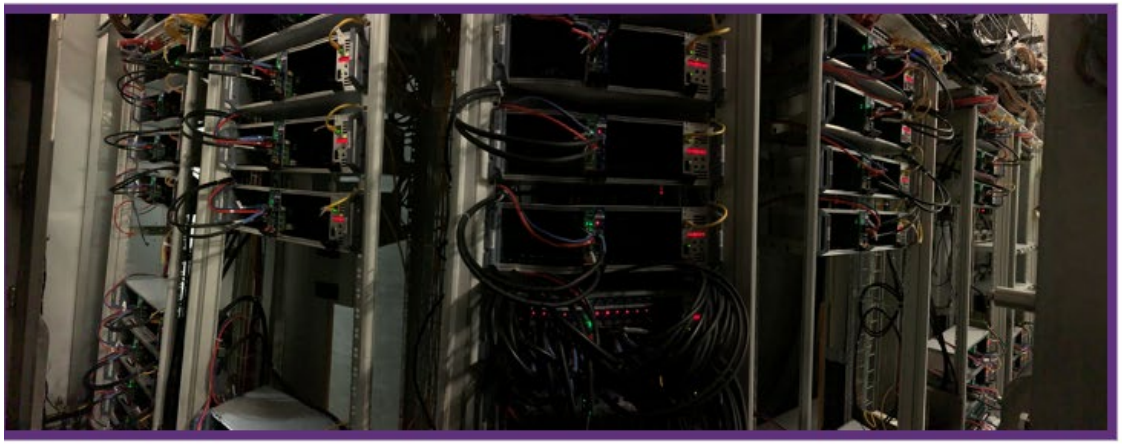
WaveDAQ

Disegnato per MEG @PSI, adottato anche da FOOT
Sistema TDAQ completamente integrato e custom
40 crate, 18 schede per crate
DAQ: digitiser a 5 GSPS
Trigger: latenza <500ns per digerire ~2TB/s su link seriali a 1 GB/s

Istituto Nazionale di Fisica Nucleare

PAUL SCHERRER INSTITUT

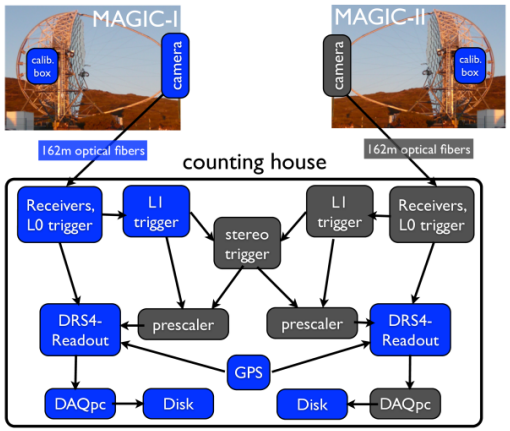
Sistema in allestimento Trigger DAQ Readout

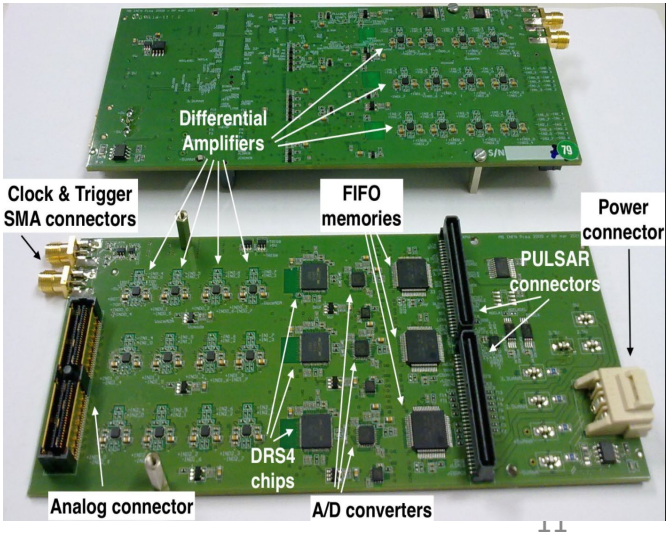


Esperimento Magic: reusable FPGA mother board

Telescopi Imaging Cherenkov a terra

- Readout con campionatori analogici DRS4 (1-2 GSPS)
  - 2048 canali
  - motherboard Pulsar (da esp. CDF)
  - mezzanina con DRS4 (24 canali)



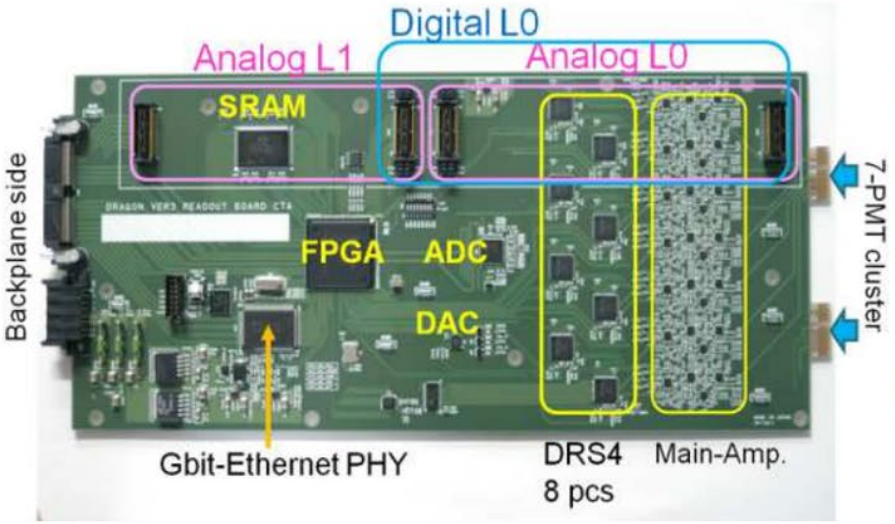


Esperimento CTA

Large Size Telescope

Elettronica di readout basata su campionatore DRS4

- 8192 celle di memoria
- campionamento 1 GSPS
- maximum buffer 8μs

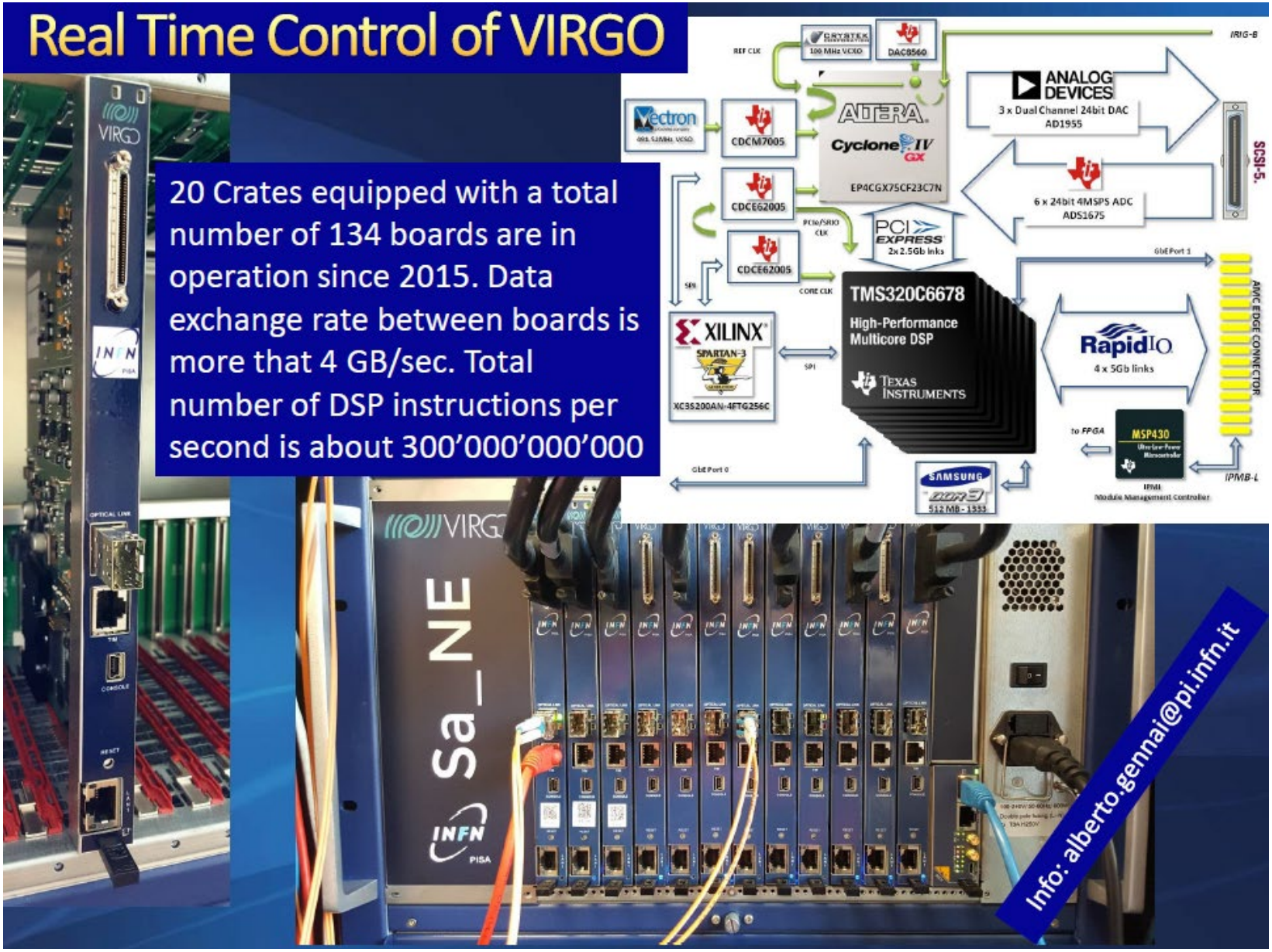


Schwarzschild-Couder Telescope

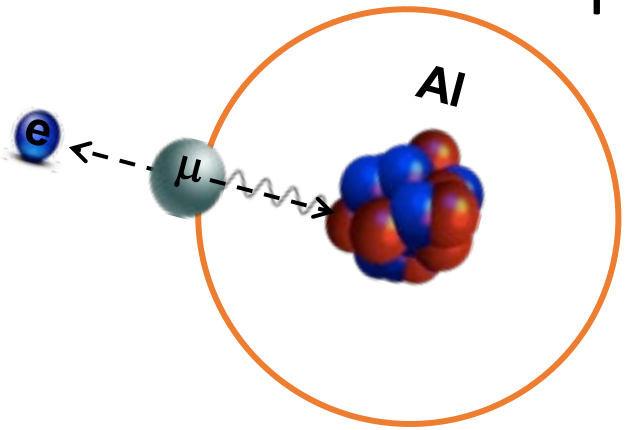
Elettronica di readout basata su campionatore Target-C

- 16384 celle di memoria
- campionamento 1 GSPS
- maximum buffer 16μs

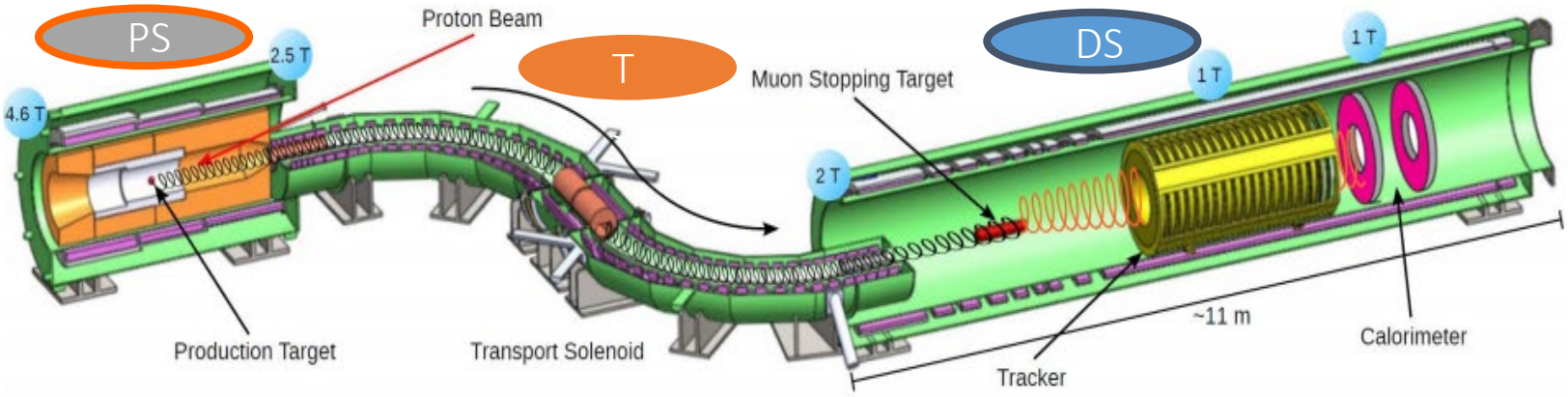
Real time DSP algorithms; Virgo



Ambiente ostile agli acceleratori: Esperimento Mu2e

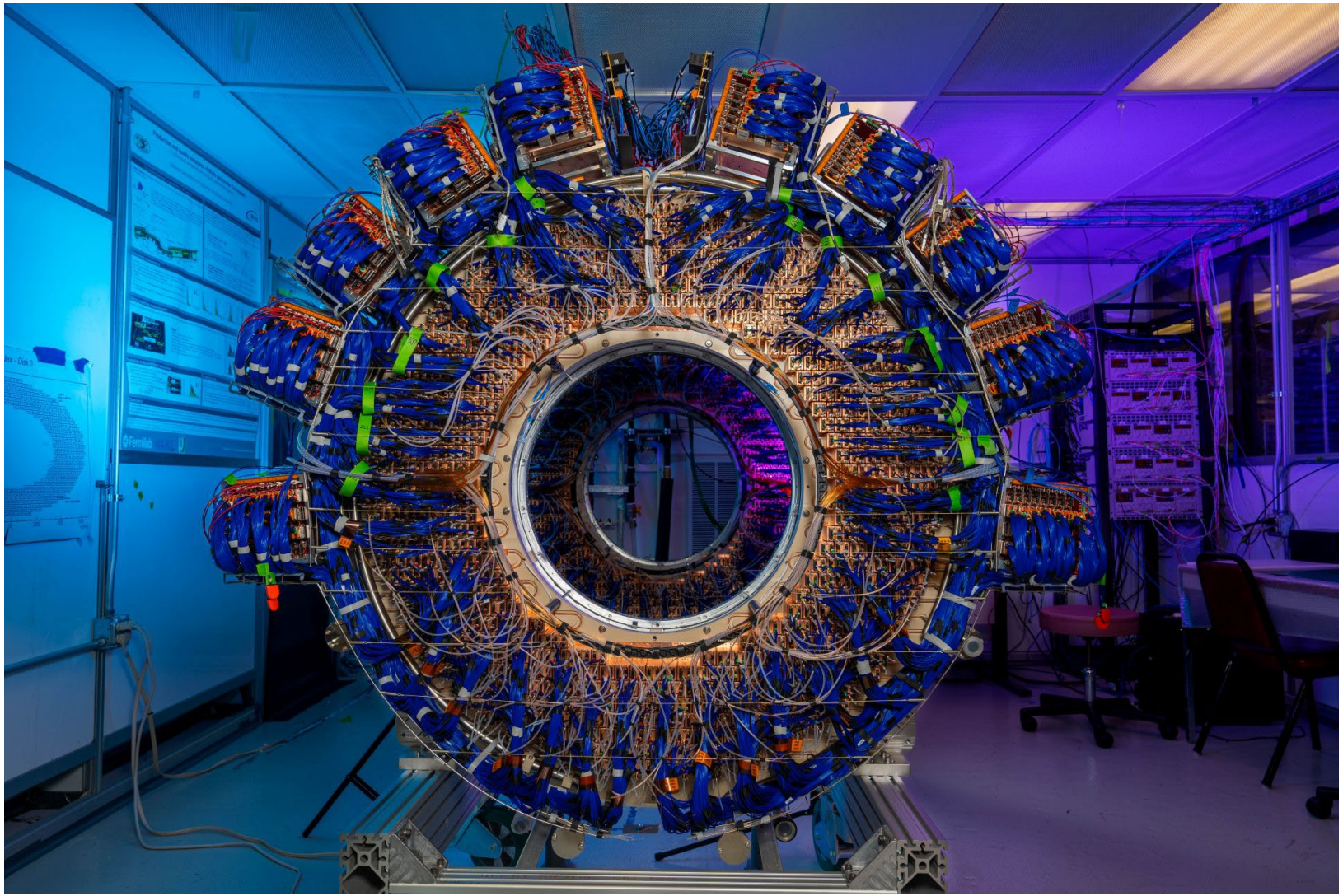


Cerca eventi di conversione diretta di Mu in e (soppressi dal Modello Standard)

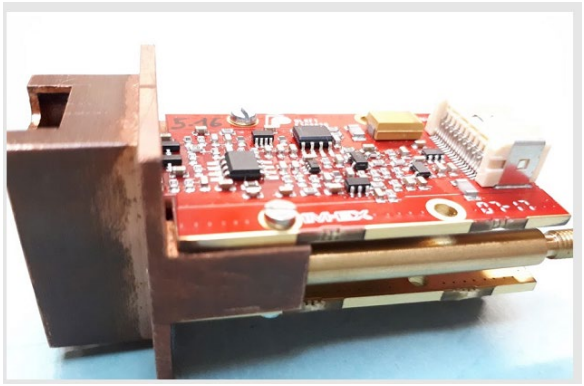


- A Pisa sviluppiamo l'elettronica di lettura del calorimetro ...
- «Copre tutto» : analogico, digitale,alto flusso, ambiente estremo

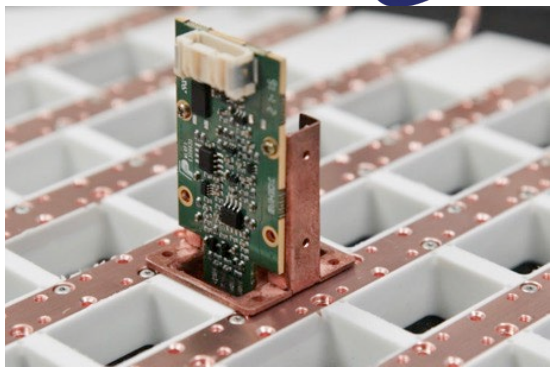
Calorimetro Mu2e

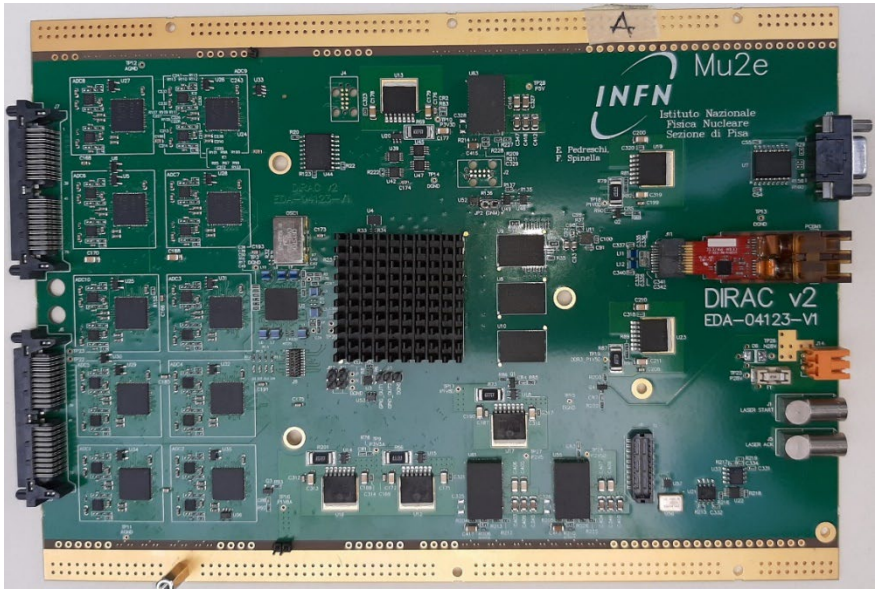


Elettronica Mu2e



- Front End Analogico
- Foto rivelatori SiPM
- Amplificatore a basso rumore
- Dose 100 Krad
- Dissipazione termica



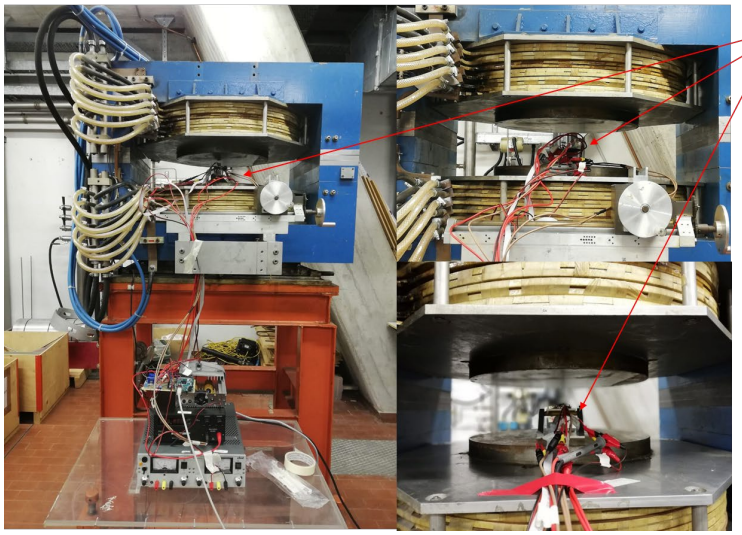


200 Msample, 12 bit, 20 canali
200 boards sincrone -> oscilloscopio da 4000 canali

Radiazione 30 Krad, 10 E 11 neutroni 1 mev eq
Campo magnetico 1T
Vuoto
Non accedibile

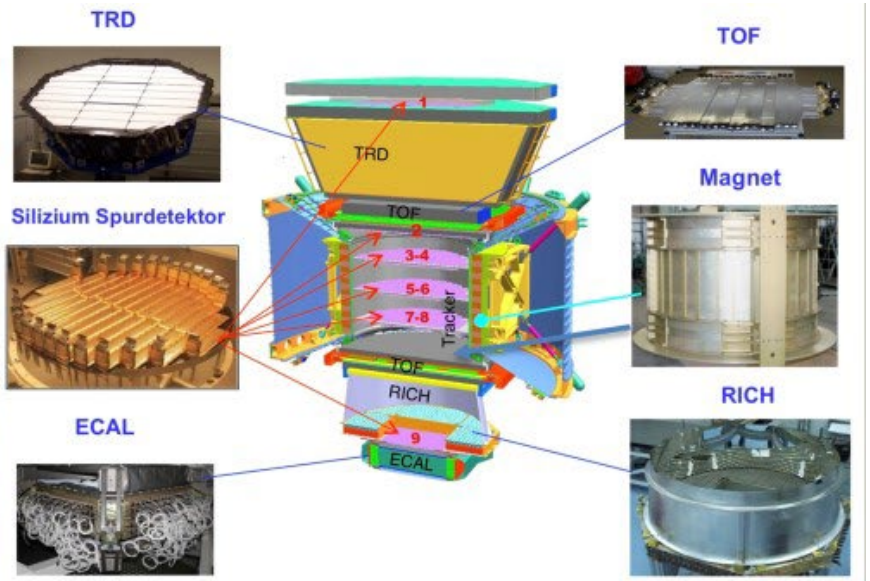
Interesse industria (CAEN)
Progetto PRIMIS
Progetto HAMLET

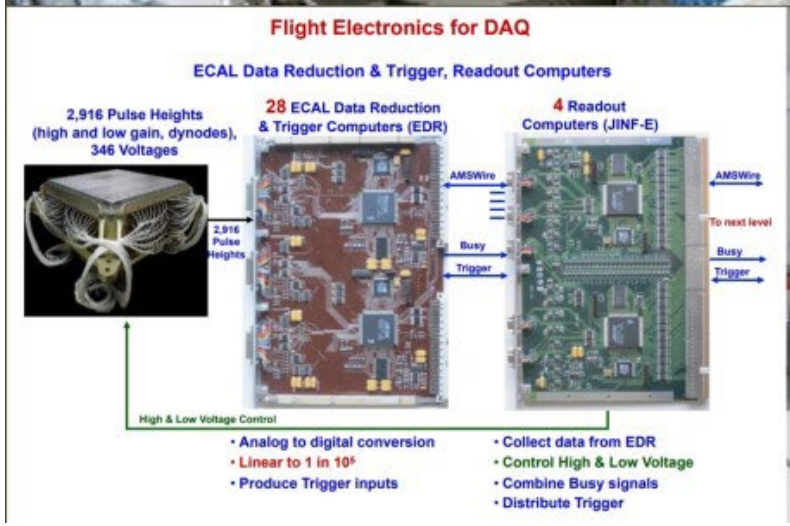
Qualifica

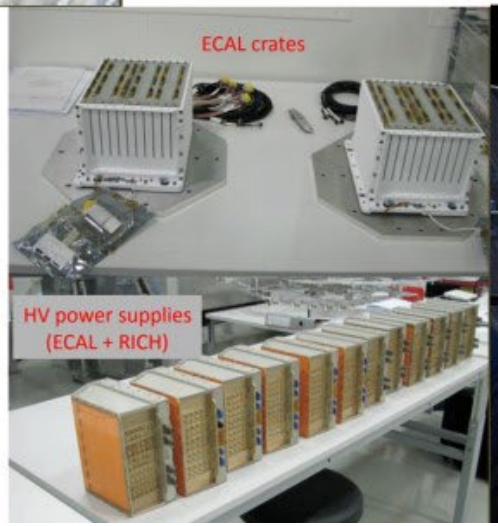


Interesse industria (CAEN)
Progetto PRIMIS

Ambiente ostile nello spazio: AMS-02

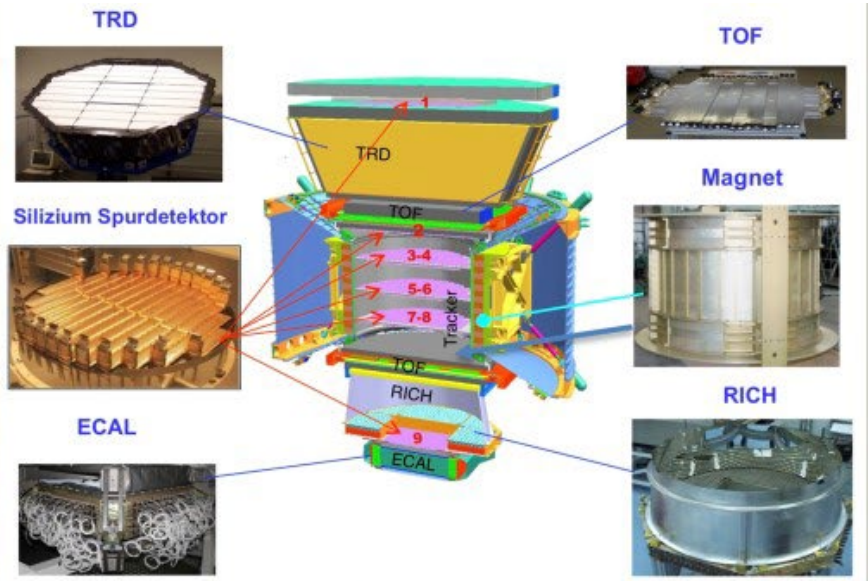


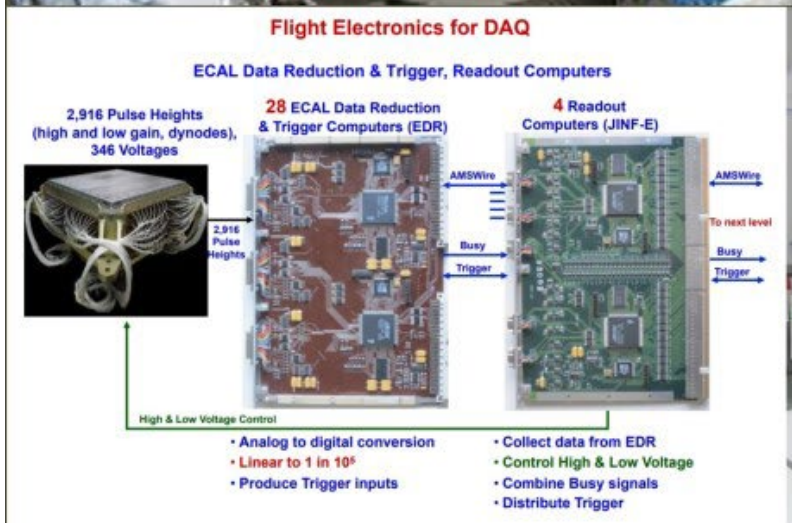


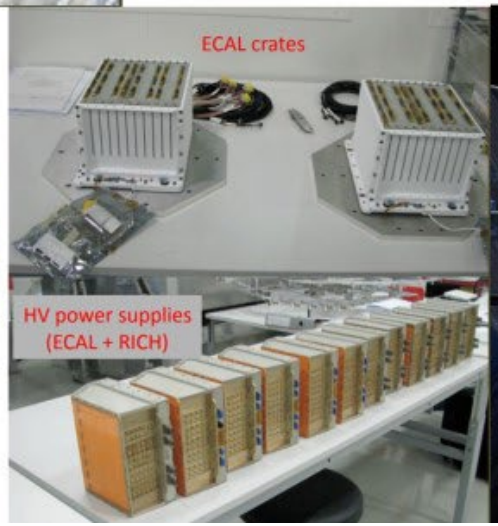


Harsh environment: Radiation, Vacuum, Temperature and Vibration

Ambiente ostile nello spazio: AMS-02





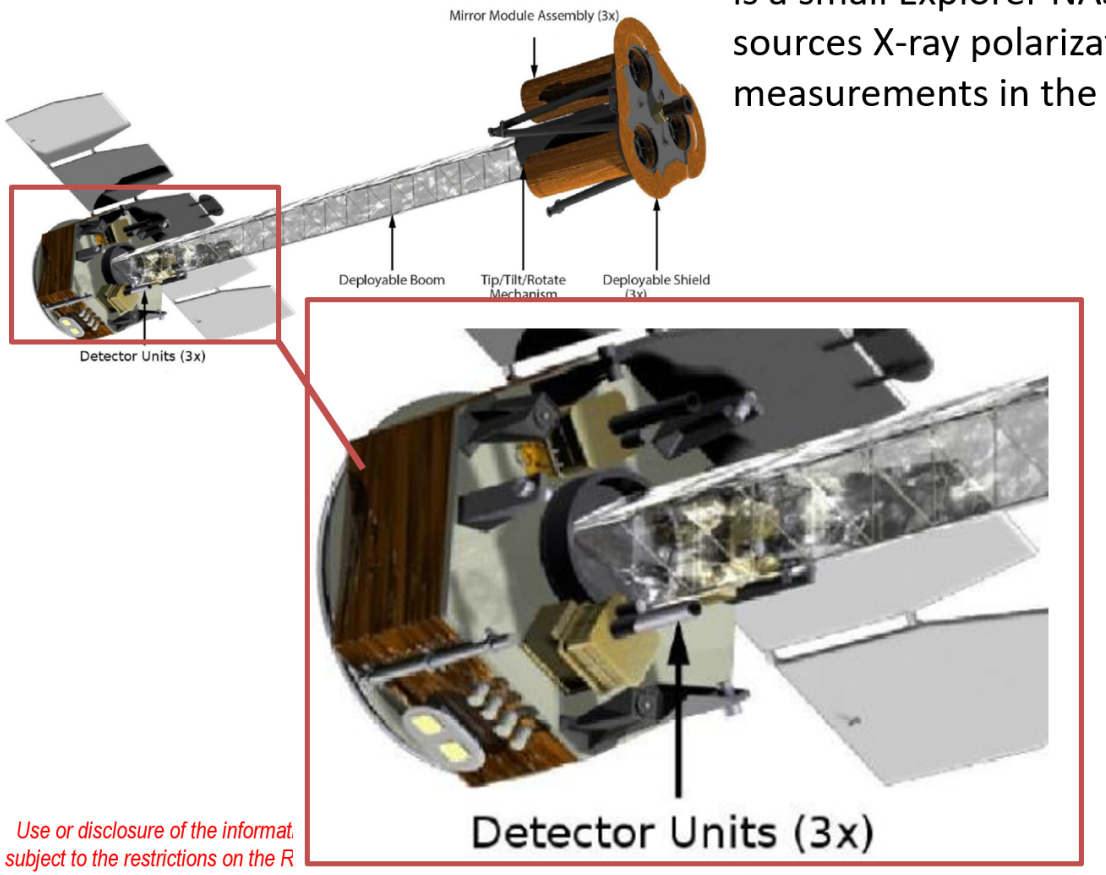


Harsh environment: Radiation, Vacuum, Temperature and Vibration

Spazio: Esperimento IXPE 1/2

IXPE
Imaging
X-Ray
Polarimetry
Explorer

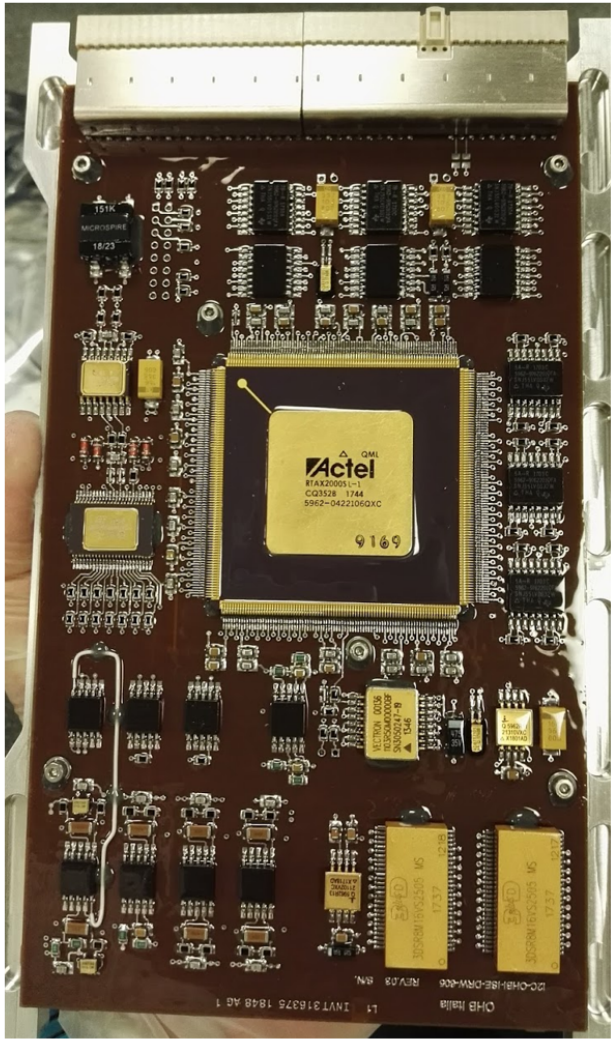
IXPE Product Tree



IXPE (Imaging X-Ray Polarimetry Explorer) is a small Explorer NASA mission for celestial sources X-ray polarization and Imaging measurements in the 2-8 keV energy band.

The Heart of IXPE is the Gas Pixel Detector invented and developed at INFN Pisa.
INFN Pisa succesfully delivered to NASA the complete Detector Unit set (X3),a self-sufficient electromechanical system including the X-ray detector, the readout and control Electronics (BEE)

Esperimento IXPE 2/2



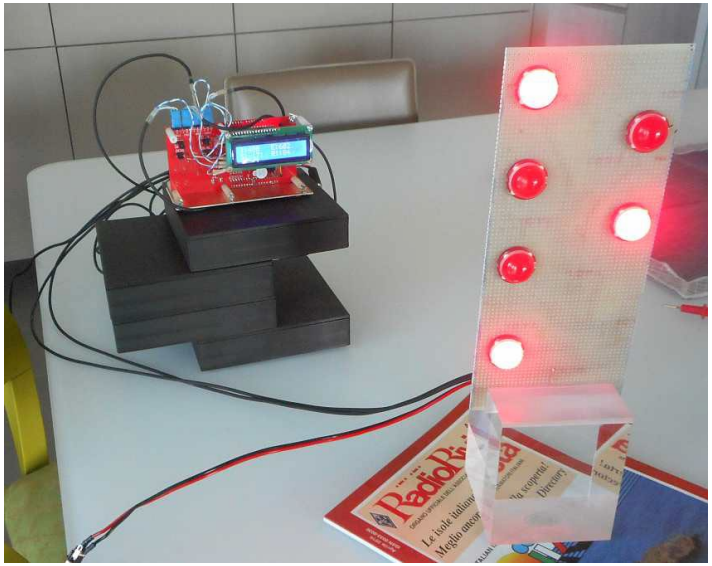
The IXPE BEE is a set of 4 electronics boards in charge to bias, control and readout the Gas Pixel Detector.

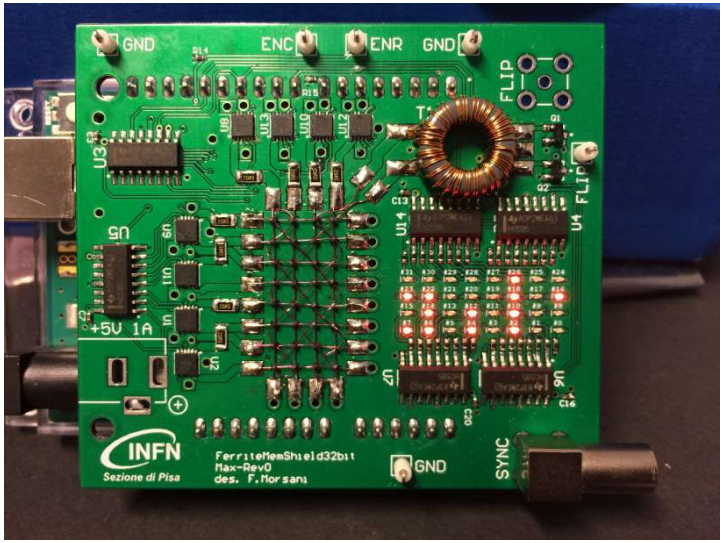
While at the BEE standpoint the IXPE environmental radiation levels are considerably low (TID < 2krad), SEE effects still need to be contained. For this reason we decided to use a Microsemi RTAX2000 device, a rad-tolerant anti-fuse FPGA.

This devices implement Radiation Hardened register to guarantee a <10E-10 SEU/day estimated at the worst case scenario

RTAX 2000 FPGA Firmware Development at INFN Pisa, required intensive Timing Analysys and post layout simulations to cope with the use of One Time Programmable expensive devices, making the FW development process very similar to that of digital IC.

Outreach




GND
ENC
ENR
GND
FLIP
+5V 1A
INFN
Sezione di Pisa
FerriteMemShield32bit
Max-Rev0
des. F.Morsani
GND
SYNC


RELE E PORTE LOGICHE

Notte del Ricercatore