RD_FCC – Silicon Detectors

Stato 2025 e richieste 2026

Riunione Referee CSN1, 18/07/2025

Attilio Andreazza Università di Milano and INFN
Fabrizio Palla INFN Pisa
Contributi da E. Robutti (GE), L. Fanò (PG), P. Azzi (PD), M. Da Rocha Solo (TO)

UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

Attività

- Sviluppo di rivelatori
  - Pixel Monolitici
  - Resistive Silicon Detectors
- Integrazione
  - Meccanica
  - Low mass PCBs
  - Serial Powering
- Fortemente integrate
  - in DRD3, DRD7 e DRD8
  - in MDI del WP di acceleratore

- Sottomesse 2 EOI alla European Strategy Update
- Incluse nel documento inviato dal PED di FCC
- Riflettono gli interessi e gli R&D in corso nelle sezioni coinvolte

Expression of Interest for a
lightweight vertex detector for FCC-ee

Involved Laboratories:
Italy: INFN - Genova, Frascati, Milano, Padova, Perugia, Pisa, Torino, Trieste-Udine
Switzerland: ETH Zurich, Paul Scherrer Institute, University of Zurich
United States of America: Brown University, BNL, FNAL, LBNL, MIT, SLAC, Stony Brook University

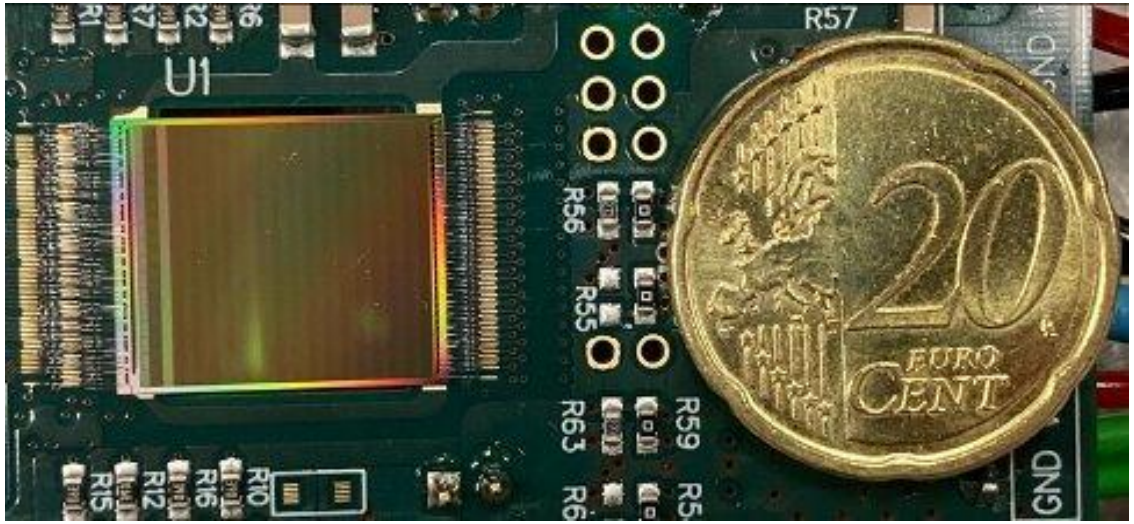
Expression of Interest for the development of modules for Vertex detector and Silicon Wrapper with combined tracking and timing capability in LFoundry 110nm technology

Involved Laboratories:
Italy: INFN - Bologna, Milano, Padova, Pavia, Perugia, Pisa, Torino, TIFPA
United States: FNAL

ARCADIA MD3

The **ARCADIA** collaboration (2019-2022) has developed a full-chip prototype targeting requirements for different applications (future colliders, space, medical)

- Sensors for application at **vertex detector** at FCC-ee
- **Low power**→ O(20 mW cm^{-2}) in high-rate mode
- Scale down to O(10 mW cm^{-2}) in low-rate mode for space applications
- **Small pixel** pitch → 25 × 25 μm^2
- Active thickness **50–200 μm fully depleted** (with backside bias HV = -90 V)
- Scalability to large area → up to 4 × 4 cm^2
- **High particle rate**→ up to 100 MHz cm^{-2}
- Timing resolution → O(1 μs)
- Investigating more advanced solutions for O(10 ns) timing
- **Digital readout** and data-push architecture



TO, PD, MI

ARCADIA MD3

Activities 2024/2025

- Lab characterization:
  - Threshold and noise characterization with monochromatic sources, e.g. Fe55 and fluorescence X-rays, and with test pulse injection
  - Study of the rate capability with X-ray tube
- Commissioning of the telescope setup for test beam
- In-beam characterization: test beam measurements at Fermilab Test Beam Facility (June-July 2024)
- Ongoing activity: paper preparation

Driven by PD group:
Sabrina Ciarlantini, Caterina Pantouvakis, Michele Rignanese, Alessandra Zingaretti, Davide Chiappara, Chiara Bonini, Patrizia Azzi, Piero Giubilato, Serena Mattiazzo, Devis Pantano, Jeffery Wyss

Activities 2026

- Lab characterization:
  - Study of the sensor performances for low energy X-ray and visible radiation PD
  - Characterization of 50 mm active area sensor for tracker MI
- Testbeam with low energy protons (Trento) and electrons (BTF Frascati) PD
- Yield studies on wafers (25 wafers available from various split) TO

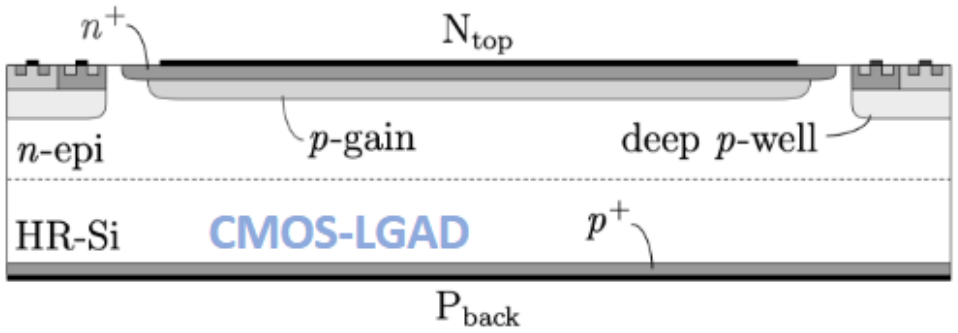
RSD Developments (TO)

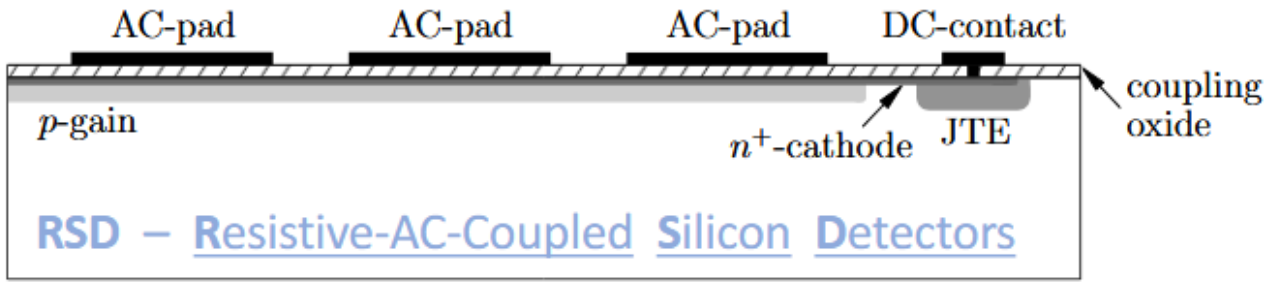
M. Mandurrino
FCC-ee Tracking WS

CMOS integration of the **LGAD technology** already demonstrated (in LF11is)

Spatial resolution **~3% of sensor pitch** (allowing to relax the channel density)

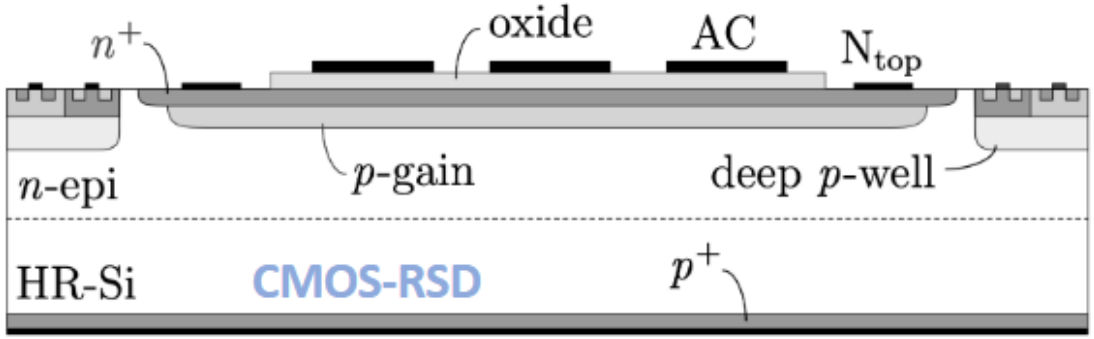
Time resolution similar to standard LGADs: **30-40 ps**





Plausible concurrent targets:

- **σ_t = 10-20 ps**
- **µm-level σ_x**
- **100% FF**

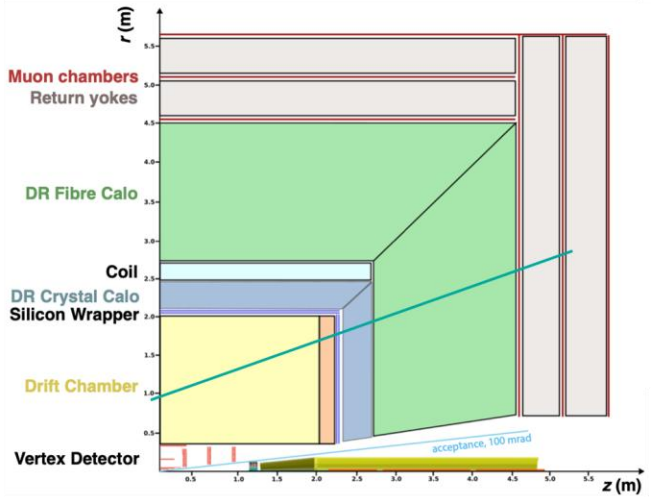


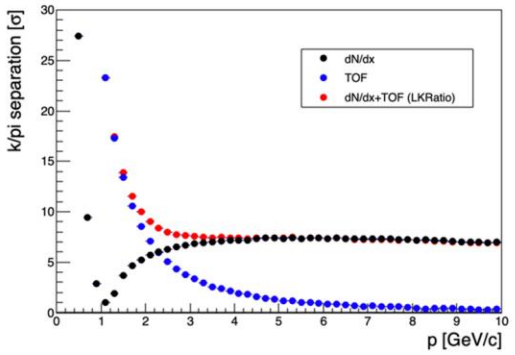
pending patent and extent of protection

Detector layout and process flow design activities are ongoing

First prototypes in next silicon production runs (std. CMOS process)

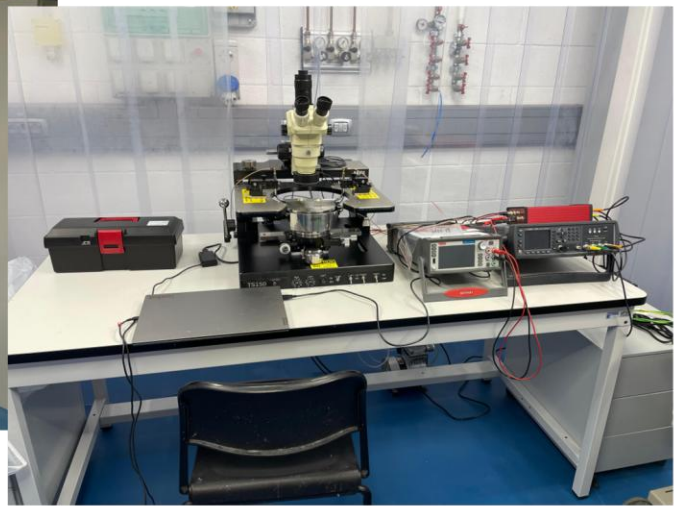
RSD for Silicon Wrapper (GE)





Set-up per caratterizzazione di sensori al silicio (in particolare RSD)

- Sistema con nuova probe station installato in camera “soft-wall” dedicata
- Sistema laser TCT pronto



Studi di simulazione su granularità silicon wrapper e introduzione misura di tempo

- Impatto in funzione di η

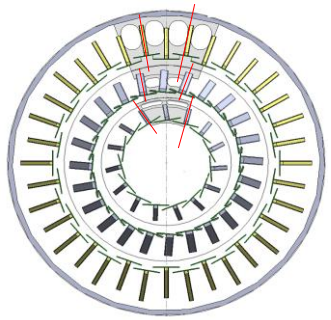
Possibili studi su nuovi canali di benchmark per l’utilizzo del TOF nella separazione K/π

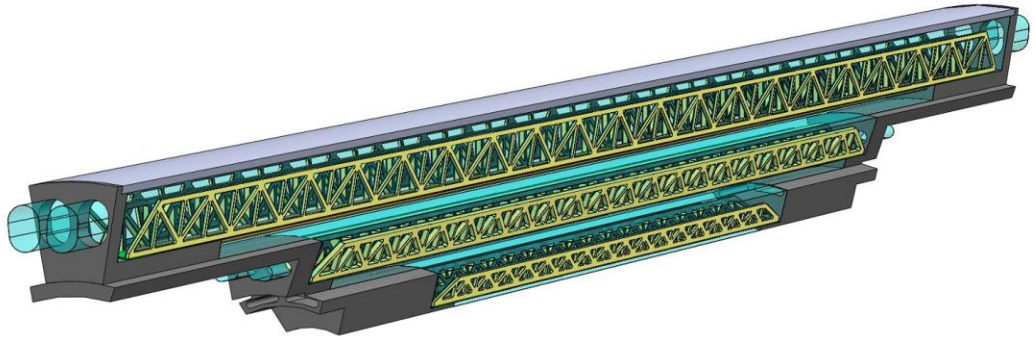
Sviluppo sensori: Richieste

Sezione	Capitolo	Richieste	DRD	Motivazione
GE	missioni	4 sj		Test su fascio di sensori RSD
MI	missioni	4 sj		Test beam rivelatori monolitici
PD	inventario	10	3.1, 7.6	Contributo per acquisto cofinanziato DOE/CSN1/CSN3/Sez.PD - ANTICIPABILE (se anticipato anche da CSN1) macchina bondatrice per attivita' di R&D comuni a FCC, MuC ed esperimenti di CSN3. (Riduzione richiesta 2025 macchina ora definita – vedi backup)
TO	consumo	10 sj		Progettazione e produzione wafer probe-card per ARCADIA-MD3, SJ a progetto PC e preventivo
TO	consumo	3.5		Produzione nuovo batch di 4 schede di front-end per sensore CMOS MD3
TO	consumo	1.5 sj		cavi e connettori per wafer testing di MD3, SJ a produzione probe-card per MD3
TO	missioni	1	7.6	Coordinamento DRD7.6a "Common access to selected imaging technologiesâ•per la tecnologia ARCADIA LF11is, 1x viaggio CERN per riunione Technical Board
TO	missioni	2	7.6	Partecipazione DRD7.6a "Common access to selected imaging technologiesâ•per la tecnologia ARCADIA LF11is, 1x viaggio x2 partecipanti CERN per Workshops DRD7
TO	missioni	2		Riunioni WP Silicon Trackers e IDEA in Italia e CERN (CMOS FD-MAPS ARCADIA, CMOS LGADs e CMOS AC-LGADs)
TO	missioni	2	3.2	Riunioni CERN per DRD3 (WP2 e WP3) compensated LGAD per tracking at extreme fluences
TO	missioni	1.5	3.4	Riunioni CERN per DRD3 (WP4), 2x viaggi al CERN
TO	missioni	2 sj		Partecipazione a Test-Beam (DESY) per FD-MAPS

Thermal Analysis (PG)

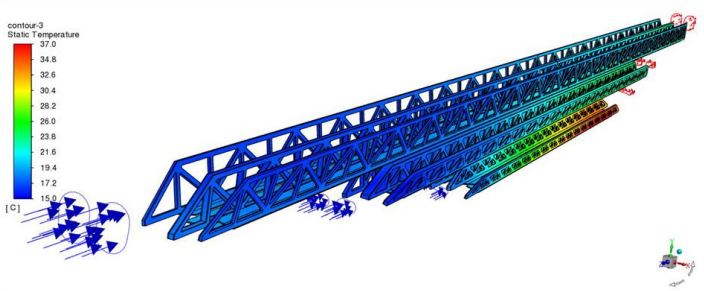
Simulated a full sector of the IDEA Vertex which includes all the three layers.



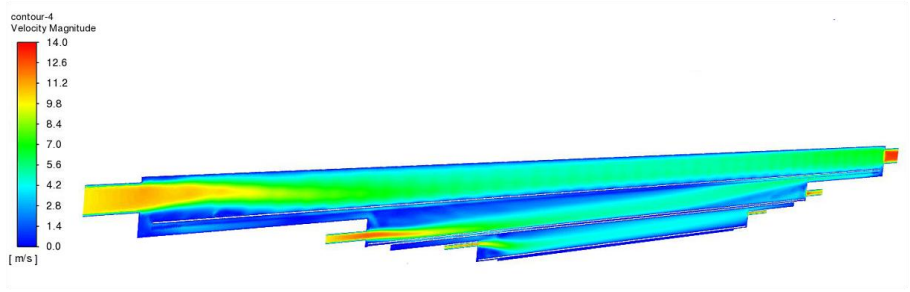


- Maximum temperature of about 35°C in layer 1, when having inlet air at 15°C with a constant velocity of 10 m/s and 10% turbulence intensity.
- Some cross-talk between air flow of different layers (this opens for further optimizations for layer 1 and 2).

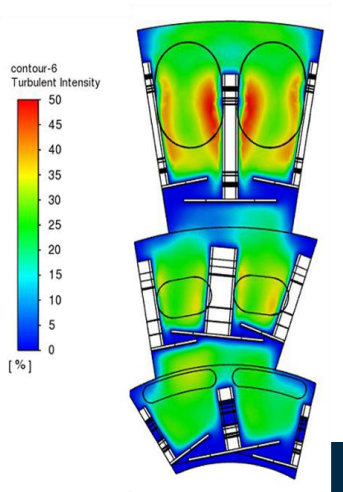
Temperature along the staves



Velocity field



Turbulent intensity



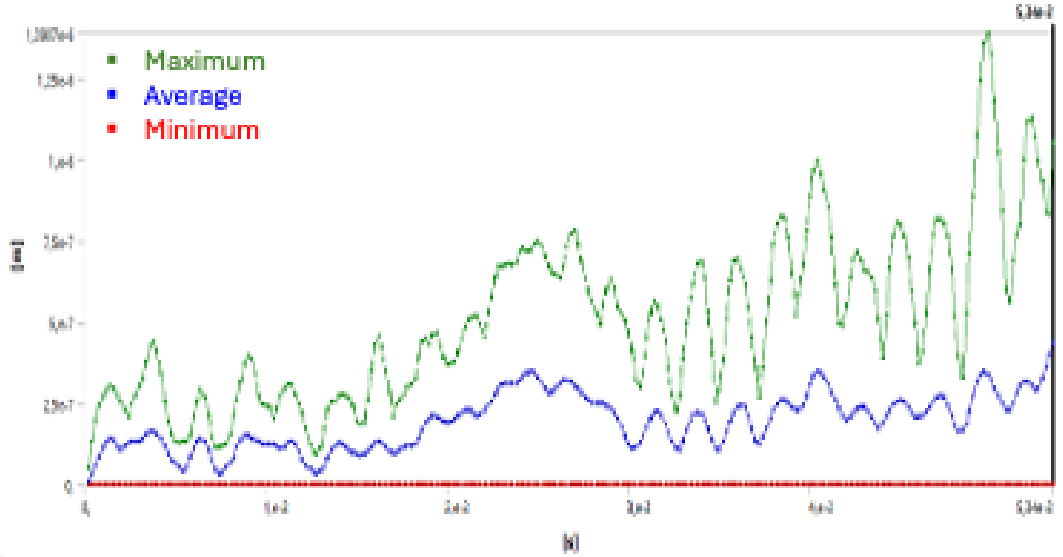
Areolastic Analysis (PG)

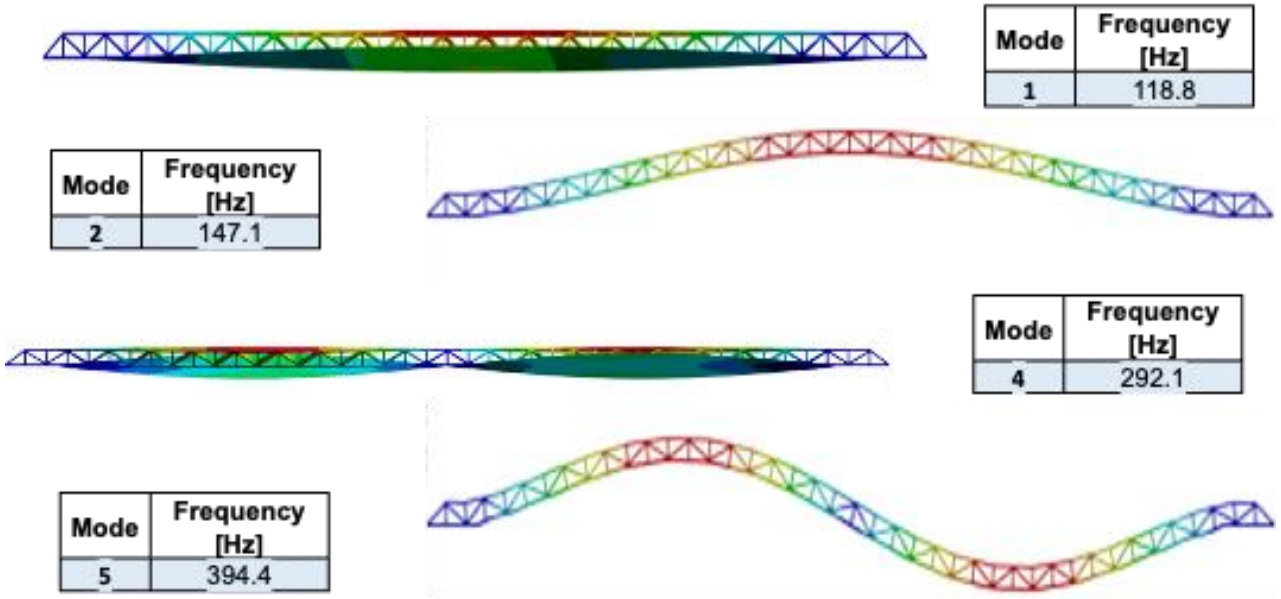
Performed on a single stave of layer 3 (the longer one, so it is plausibly a worst case for vibrations)

Natural frequencies of the structure have been estimated

- 1st mode @ about 120 Hz.
- Vibrations found in the micron scale.

Global deformation:





Mode	Frequency [Hz]
1	118.8
2	147.1
4	292.1
5	394.4

Natural frequencies and vibrations modes

Huge dependency of the results on mechanical constraints and material properties → Experimental measurements are crucial

Richieste 2026 (PG)

Motivazioni:

Attualmente, queste proprietà sono stimate basandosi su librerie ed esperienza.
Per esempio, la fibra di carbonio (CF) si comporta in modo molto diverso a seconda dei materiali di base degli strati, dell'orientamento, del numero di strati, della pressione durante la polimerizzazione…

Sinergia con il Progetto **DRD8 WP 2.2** "Caratterizzazione delle proprietà dei materiali e sviluppo di database", dove Perugia è coinvolta.

→

Realizzazione di un'apparecchiatura personalizzata per la misurazione della **conducibilità termica**.

Il design è già disponibile.

Richiesta di 4.000€ per l'acquisto dei componenti.

2) Risorse per simulazione

Le simulazioni finora sono state eseguite su due workstation desktop di medie prestazioni.

Le simulazioni dinamiche richiedono maggiori risorse di calcolo; quelle attuali sono attualmente sature. **DRD8 WP 1.1**

→

Nuove risorse in un modello computazionale diverso, sfruttando i cluster locali.

Richiesta di 4.000€ per co-finanziare con UNIPG un nuovo server+storage das integrare nel cluster locale

N.B: Attività e richieste di Pisa discusse nella parte MDI dell'acceleratore

Richieste 2026 (PG)

Richiesta di acquisto per un sistema ottico-digitale di ispezione e analisi metrologica

- Il miglior modello individuato per le nostre esigenze: **Keyence serie VHX ->** Costo: **~ 100 K€**
- Alcune caratteristiche:
  - Ispezione ottica fino a 6000X, scansione 3D tramite focus stacking.
  - Metrologia ottica automatizzabile, image stitching tramite tavolo motorizzato.
  - Misure di proprietà superficiali dei materiali (Es. rugosità)

Campi di applicazione: potenzialmente tutte le attività di costruzione meccanica e assemblaggi

interplay con DRD8 -

WP 1.1 (attività: Thermal simulations of the vertex region)
WP 3.2 (attività: Thermal simulations of Microchannels)
→ Input geometrici fondamentali a scale così piccole

WP 2.2 (Attività: Material characterization) → Fondamentale per l'analisi di rugosità e porosità per la caratterizzazione dei materiali e la qualifica dei provini

Totale **100 K€**

Richiesta di cofinanziamento: **30% FCC**

70% tra sezione, dotazioni e università (già discusso in sezione, volontà di contribuire da sezione, dotazione 1 e dotazione 2)

DRD3 CCF Proposal

MI + (TN, TO, FBK)

- This proposal aims to develop a **large area HV-CMOS pixel detector demonstrator** for large-scale production in **future Higgs factory** experiments, based on **multi-chip modules** with **data aggregation** and **serial powering**.
- These multi-chip modules, including **low-mass multilayer flexible PCBs**, will then be integrated in staves, where modules will be powered in serial mode utilising the on-chip Shunt Low Drop Out (SDLO) regulators. Together with data aggregation, this will substantially **reduce the number of stave data and power connections**.
- **Low-mass aluminium flex productions**, innovative connection methods (e.g. single-point Tape Automated Bonding), **low-mass mechanical support**, and **efficient cooling technologies** will be explored for overall system optimization in power and material budget.
- *The expertise gained by the participating institutes will be beneficial for the integration of future full-size devices that will be developed by the strategic DRD3 projects in the next few years*

Available for comment in DRD3 CDS Repository: CERN-DRD3-PROJECT-2025-014

Progetto DRD3

Procurements		Cost (CHF)
Al Serial Power Bus for ATLASPIX 3.1 (CERN)	2025: 14k MI da CSN1	15,000
Cu Multi Chip Module Flex LF sensors (design verification)	Coperto da IHEP	5,000
Al Multi Chip Module Flex LF sensors (FBK)	Fondi DRD3	15,000
Al Serial Power Bus for LF sensors (CERN)	Fondi DRD3	15,000
DAQ Upgrades (FPGA, chip carriers and readout boards)	2026: 4k MI + Istituti partecipanti	15,000
Chip-to-Module assembly jigs	Richieste PI+MI da finalizzare nel 2027	2,000
Stave loading and test equipment		10,000
CMOS Wafers production and processing (thinning and dicing)	Fondi DRD3 + *contributi KIT/UK*	20,000
Total project cost:		**107,000**

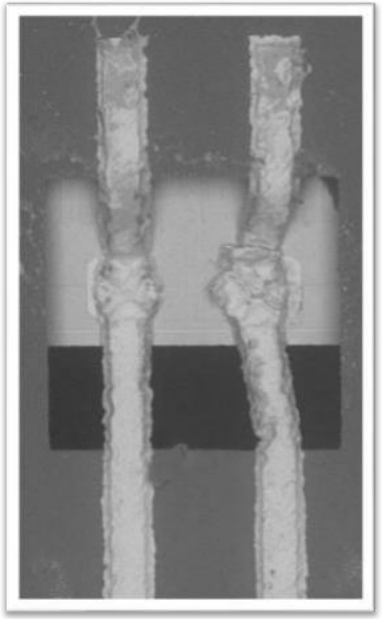
New process

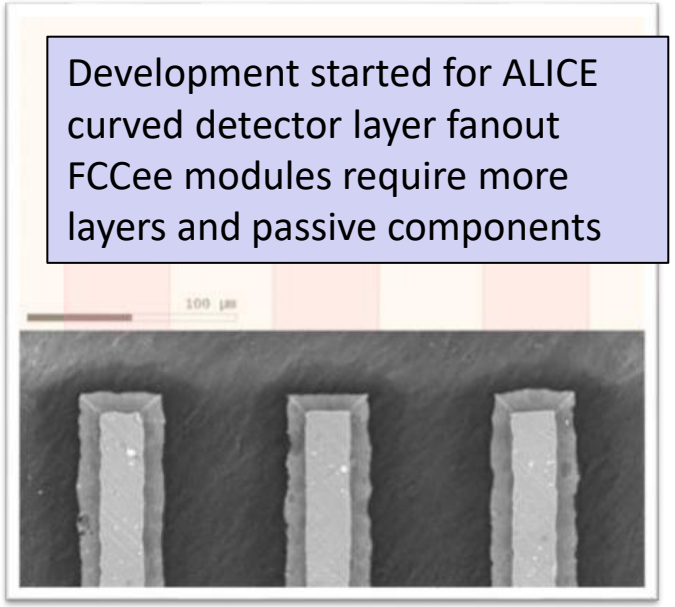
New sensors

- **Total project cost:** **107,000 CHF**
  - DRD3 CCF contribution (13 institutes × 2650 CHF) 34,450 CHF
  - RD50 CCF contribution (6 institutes × 2650 CHF) 15,900 CHF
  - Funding from participating institutions 56,650 CHF

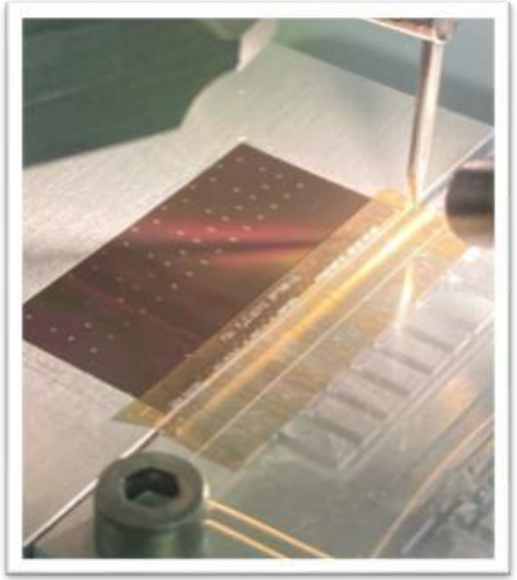
FBK thin PCB process

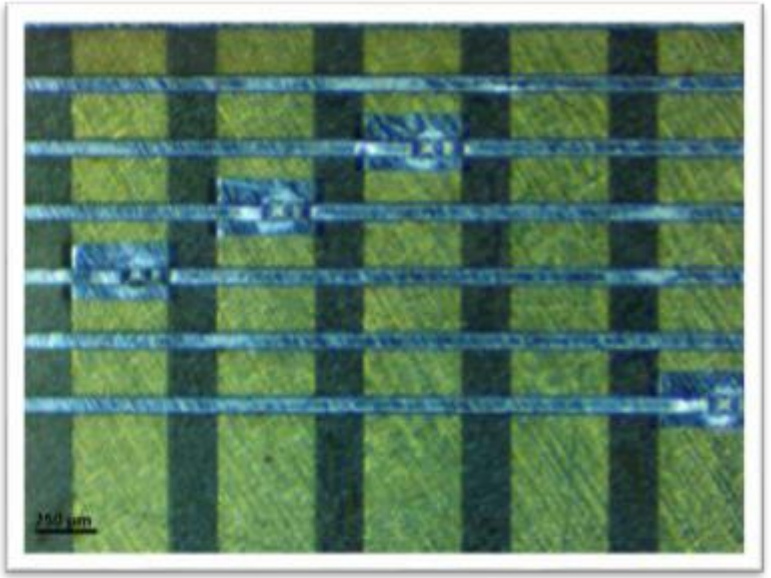
- Fabrication process inspired from the state-of-art LTU-Kharkiv [DOI: 10.15407/fm24.01.143]
- Processing inside FBK cleanrooms
- Kapton-Al PCBs
  - 20 μm Al thickness
  - 25 μm Kapton thickness
  - **Wafer level manufacturing (6" wafers)**
- Feature size
  - minimal size is 2 × Al thickness = 40 μm
  - very high line density (90 μm pitch)
- Interconnection
  - spTAB 75 × 75 μm tool tip
  - flex-to-chip TAB
  - flex-to-flex TAB:
    - use TAB as vias to reduce overall material
    - connection to additional flexible PCB





Development started for ALICE curved detector layer fanout FCCee modules require more layers and passive components





Integrazione: Richieste

Sezione	Capitolo	Richieste	DRD	Motivazione
MI	consumo	4	3.1	Ammodernamento sistema di DAQ per HV-CMOS (Common Fund Project)
MI	consumo	26	3.7	Sviluppo di circuiti flessibili sottili con FBK Stima da parte di FBK per processo a 4 layer necessario per FCC: 11 maschere equivalenti (5k a maschera, ma attivabile convenzione INFN: CSN1 50%) Potrebbe rientrare in un progetto strategico del DRD3-WP7 *In-house plating, hybridisation and module-integration technologies for pixel detectors* CERN-DRD3-PROJECT-2025-002
PG	consumo	4	8.2	WP3 - TK - apparato per la misura della conducibilita' termica
PG	inventario	4		WP3 - CALCOLO - cofinanziamento 50% (altro 50% UNIPG) server alte prestazioni per le simulazioni termiche e meccaniche
PG	inventario	30	8.2	WP3 - TK - cofinanziamento 50% strumento ottico per metrologia (sinergia DRD 8 - WP2 - 1.1, 2.2 e 3.2). Il restante 50% tra sezione e UNIPG. La discussione per la definizione del cofinanziamento e' in corso.

BACKUP

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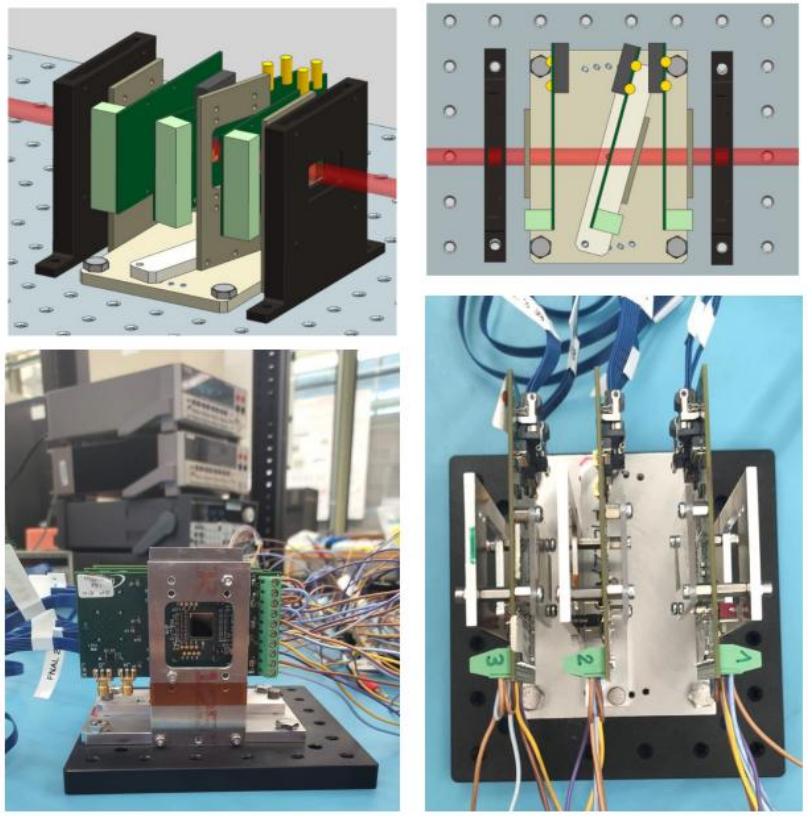
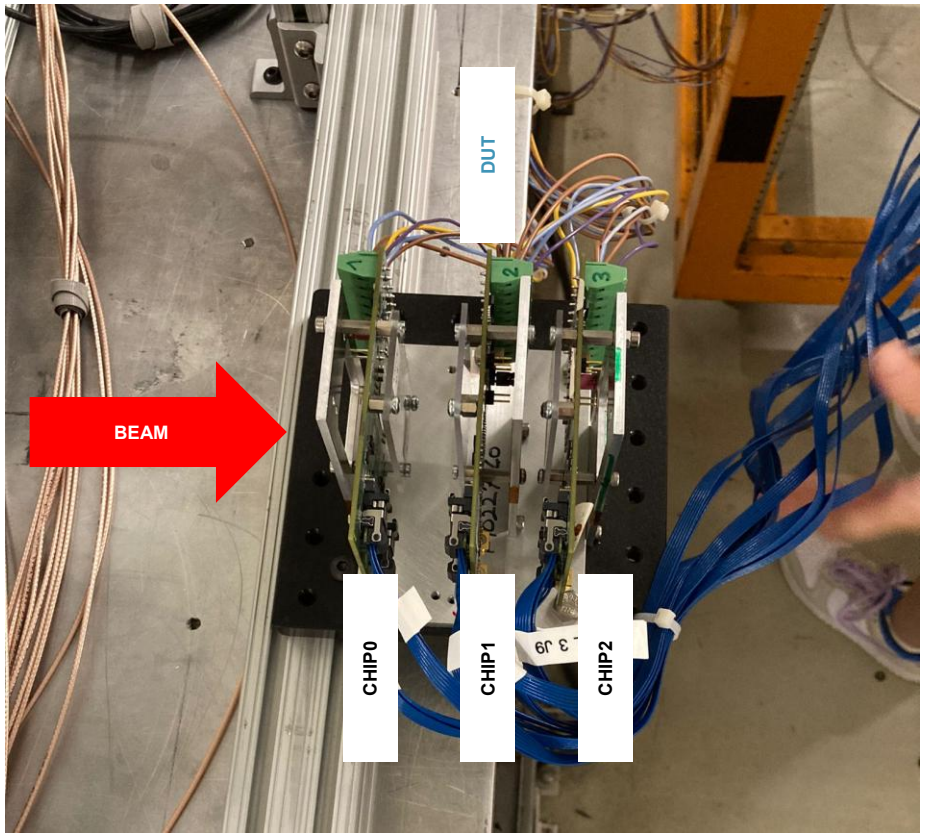
UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

ARCADIA MD3: Test beam @ FNAL

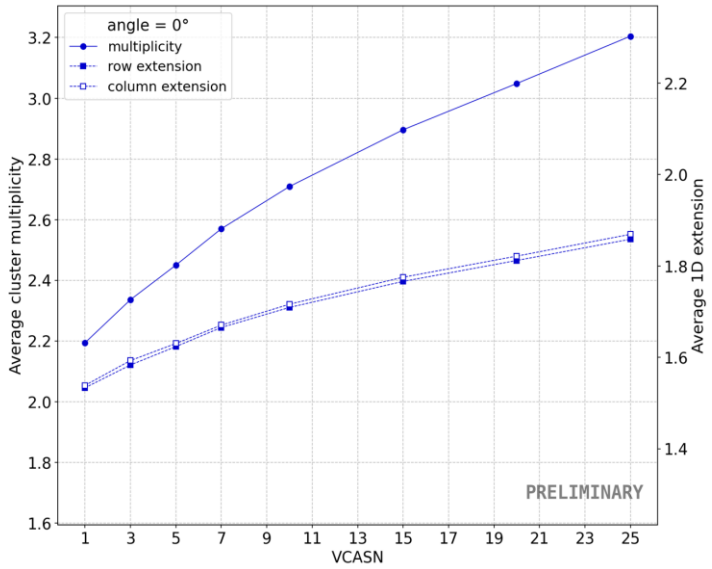
- 120 GeV proton beam
- Telescope with 3 ARCADIA-MD3 chips (one DUT, two tracking planes)
- Threshold, sensor HV, Front End circuit parameter and incidence angle parametrization: study of cluster size, tracking efficiency, spatial resolution



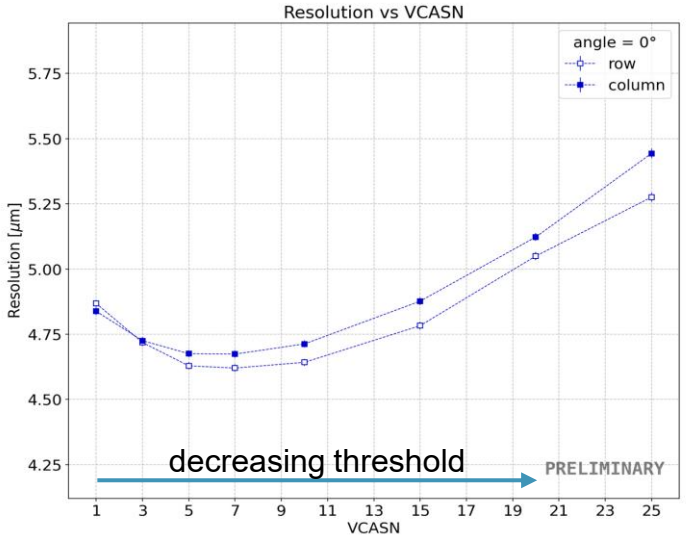


ARCADIA MD3: Test beam @ FNAL

Cluster size



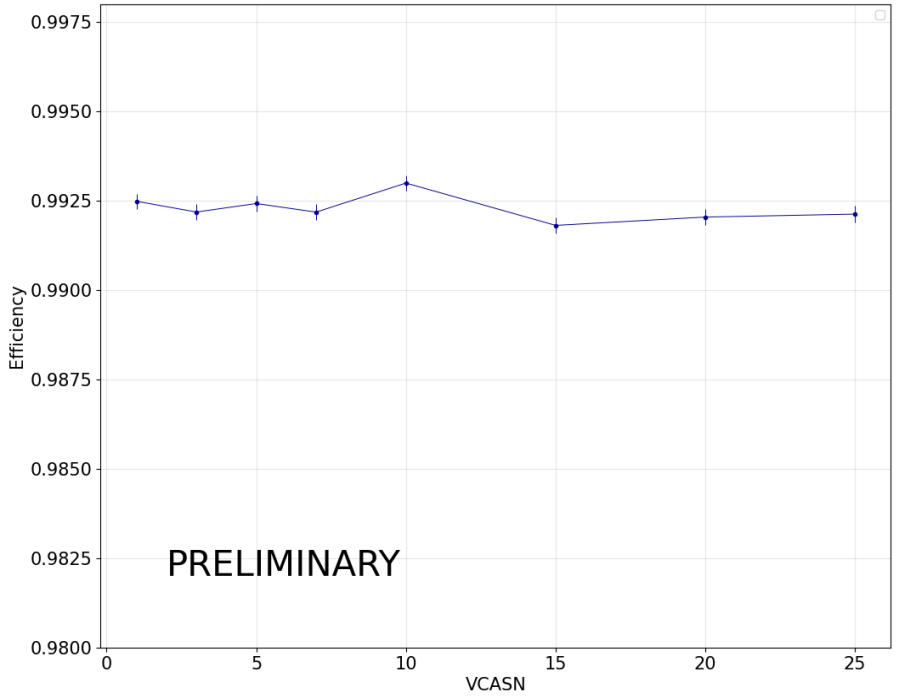
Resolution



Results with DUT orthogonal to the beam

Detection efficiency

Average efficiency over threshold scan range: 99.23 %



VCASN is the DAC parameter controlling pixel **threshold**
The two parameters are **inversely proportional**

TPT HB16 Wire Bonder

HB16 Wire Bonder

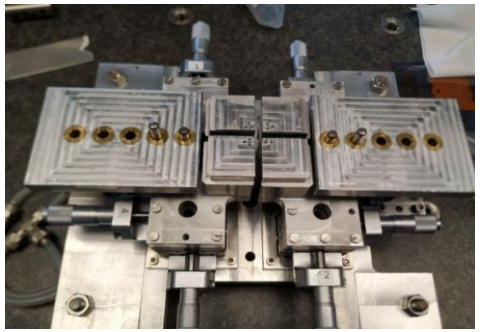
with motorized Z- & Y - Axes

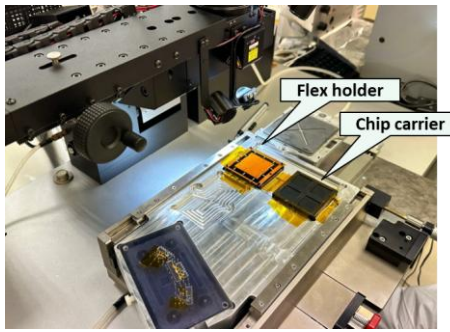
Our goal is to support developers in realizing new ideas and applications for microelectronics. Our customers are startups, universities and large corporations, in more than 40 countries around the globe.

Disponibile offerta per 66517 Eur IVA Esclusa
10 kEur contributo RD_FCC - PD
Rimanente da MuCol, esperimenti di CSN3, dotazioni e fondi di sezione

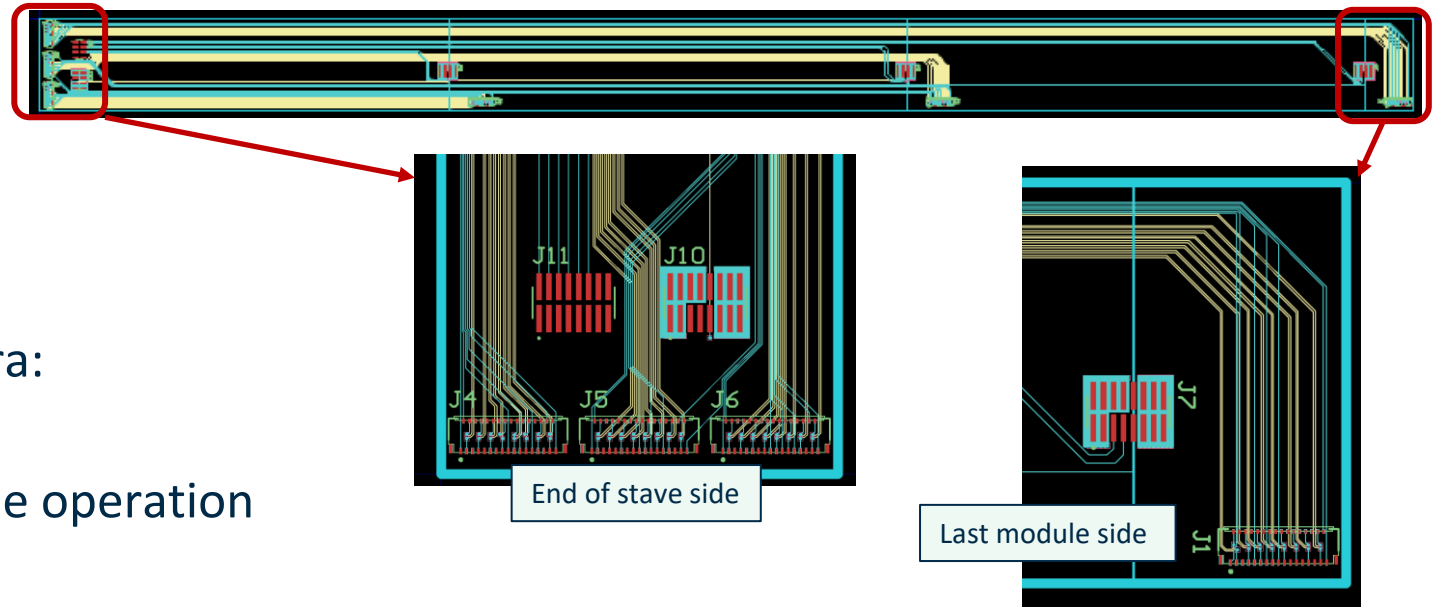
Stage 1 Completion

- Assembly modules with remaining ATLASPIX3.1 chips
  - ~6 modules with 150 μm sensors probed by Milano/Edinburgh
  - 50 μm sensors available from Heidelberg
  - Either pick-and-place or dedicated jig





- Designed a power bus to test a multi-module serial power chain
  - Aluminium conductor to reduce thickness in radiation lengths
  - Connecting to modules by pigtails
  - 4 cm × 60 cm size to match CERN Microfabrication Lab capability
  - Received quotation from Rui De Oliveira: 14,200 CHF for a panel (5-8 pieces)
  - Ready to start production, since module operation issues are solved



- Loading of cold plate (half stave with 3 modules + heaters)
  - **All material already available in Pisa from previous year RD_FCC funds**

Institutes and Contact Persons

Institute	DRD3	RD50	Project contact
University of Birmingham	x	x	James Glover
University of Bristol	x		Jaap Velthuis
University of Edinburgh	x		Yanyan Gao
University of Heidelberg	x		Heiko Augustin
Hochschule RheinMain	x		Daniel Muenstermann
IHEP	x	x	Yiming Li
INFN and University of Milano	x		Attilio Andreazza
KIT	x		Ivan Peric
University of Lancaster	x	x	Harald Fox
INFN Pisa	x	x	Fabrizio Palla
FBK Trento	x	x	David Novel
TIFPA and University of Trento	x		Roberto Iuppa
INFN Torino	x	x	Stefania Beolé
Participating institutes	**13**	**6**	

Deliverables and timelines

Deliverable	Timeline
Multi-chip module construction and readout (ATLASPix3.1)	06/2025
Al-flex production for ATLASPix3.1 power bus	09/2025
ATLASPix-based SP chain prototype construction and characterisation	03/2026
Submission and production of new CMOS sensors (LF)	07/2025-03/2026
Multi-chip readout flex submission for the LF CMOS sensors	12/2026
Multi-chip LF module construction and readout	03/2027
Al-flex production for the LF CMOS sensors	09/2027
LF sensors based SP chain prototype construction	01/2028
LF sensors based SP chain prototype evaluation	03/2028

Stage 2 planning

1. **Submission and production of LF generic R&D chips**
2. **Thinning of sensors to samples of 150 and 50 μm thickness**
3. **Design and production of multi-chip module PCB for LF sensors:**

   Requires sequential steps in understanding and verification of chip behaviour:

   1. Test of chips on single-chip-carriers, to define the operating point, minimal amount of signal, wire bonding and register configuration
   2. Copper based version, standard wire bonding, to verify the schematics and operation of the multi-chip modules
   3. Low-mass Aluminum based using FBK technology, implementing tab bonding
4. **Assembly and operation of SP chain with multi-chip modules**
   - Daisy chaining of modules through adapter cards
   - Interface to DAQ system
5. **Realization of an integrated power bus and multi-chip module PCB**
   - Major step with respect to the separate structure with power bus and module PCB as separate pieces, connected by pigtails
   - **May test some of the chip-to-flex attach technologies being developed in WG7**

DRD3 CCF: Risk Assesment

- **LF submission will not provide suitable chips**
  - hold some ATLASPIX3.1 chips till result of submission is known
  - perform stage 2 with P2Pix sensors
  - "digital modules" using RD53 pixel chips for HL-LHC (no physical signal, electrical only test – too high power consumption)

- **Do not get INFN funding for FBK flexible PCB production**
  - build module flex with standard wire bonding technique
  - explore another vendor