Design of a multi-function ASIC for reading out large SiPM-based systems

Università di Siena & INFN Sezione di Pisa
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Sezione di Pisa

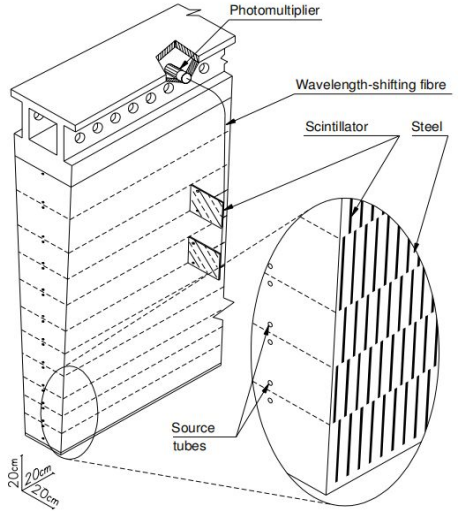
UNIVERSITÀ DI SIENA 1240

Introduction

- The idea of developing a **new versatile device** for handling analog inputs from a multichannel photo-sensor originates from the proposal to increase the TileCal readout granularity for the HL-LHC phase by replacing single-anode PMTs with MA-PMTs, while minimizing the increase in digital readout channels.

- The system must be able to independently amplify each readout channel (equalization) and sum a configurable number of channels into a single output signal.

- **This readout concept is valuable not only for TileCal but also, more broadly, for various future calorimeters—especially since all upcoming designs plan to use SiPMs and will benefit from fully configurable readout systems.**



Just a few examples

1) All calorimeters

Configurable sums of energy deposit would allow to use the same device for defining trigger towers in different regions (barrel/forward/end-cap) and for different calorimeter sections (e.m./hadronic).

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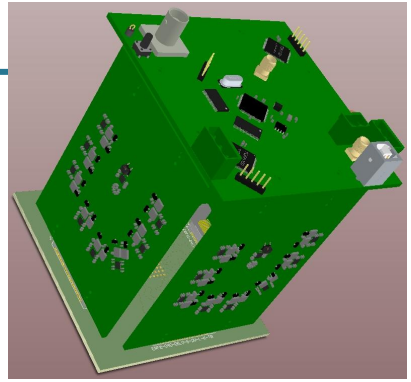
3) Hadronic sampling calorimeters à TileCal (ALLEGRO HCAL barrel) and dual readout Dream-like calorimeters (HiDRa), with SiPM readout

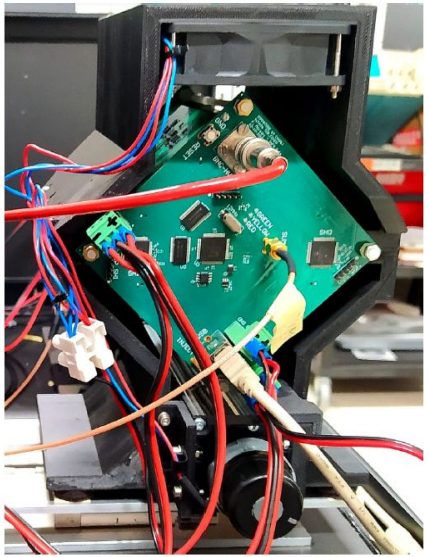
Dynamics definition of Regions of Interest (ROIs) for energy deposits would improve both the separation of small radius jets and the definition of the contour of merged jets in hadronic decays of boosted particles.

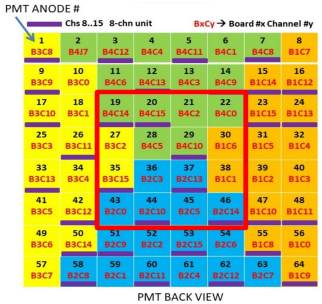
Discrete-component prototype



- Designed and developed by Dr. Fabio Morsani (INFN-Pisa)
- The system is composed by **6 Printed Circuit Boards** (PCBs), built with high-bandwidth Integrated Circuits (ICs).
- As a first proof of feasibility no constraint on system dimensions, nor on power consumption (25 W) was applied.
- The prototype was tested using a signal injection system, and a laser system for the readout of a MA-PMT;

Excellent results were obtained in terms of time jitter (~ 50 ps), as well as linearity and pulse shape stability in the analog sum of an arbitrary number of channels.





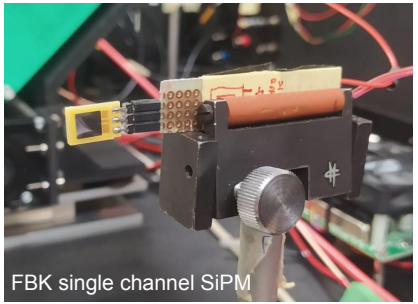
Tests in Pisa: from MA-PMT to SiPMs

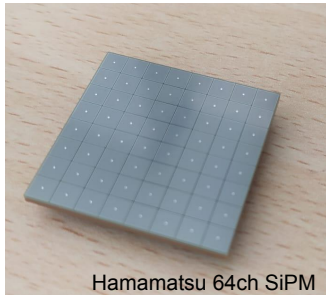
- Tests of the discrete-component prototype using a single channel SiPM (FBK) have started in the ATLAS-Pisa lab;

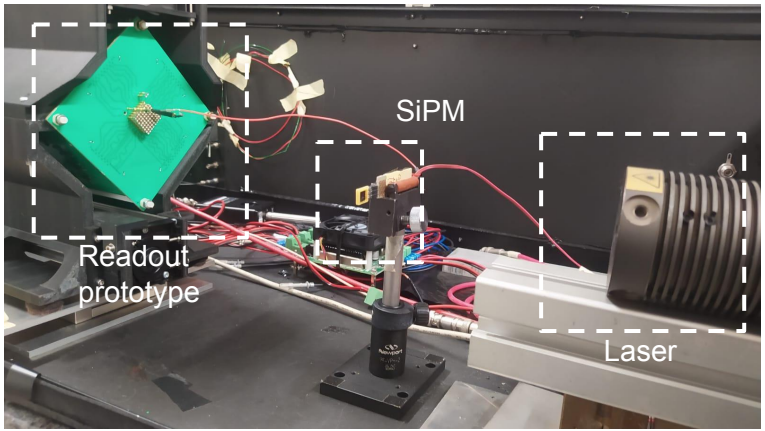
  The goal is to gain experience and transition from working with PMTs and multi-anode PMTs to SiPMs, aligning with future calorimeter developments and understanding how to properly read these devices.

- We developed a system to adapt the single-channel SiPM to the discrete-component prototype and built an optical line with a laser setup for testing.

- We are also planning a hybrid solution (CAEN A5251 adapter + custom PCB) for upcoming tests with a 64-channel SiPM (Hamamatsu S13361-3050AE-08, currently borrowed from medical physics), scheduled for September 2025.

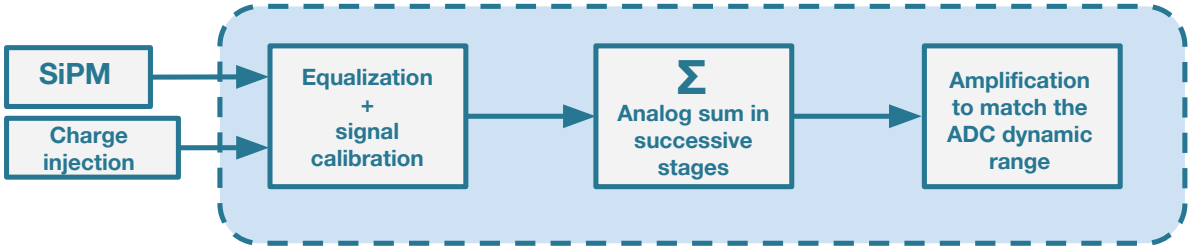

FBK single channel SiPM


Hamamatsu 64ch SiPM



A new versatile analog ASIC

- **The aim is to design a new ASIC device to readout multi-channel photodetectors, with the same features as the prototype, namely based on the equalization and on the analog sum of a programmable number of channels.**
- The idea is to design a first basic prototype for an ASIC 64-channels version of the device.



- The ASIC will be **versatile** and will allow the addition of features to meet the needs of future users.

Potentially interested institutes

- **The project is officially part of the CERN DRD6 WP3 project for the development of new sampling calorimeters with scintillating tiles (TileCal, sub-task 3.3.2).**
- Also the project for the development of Dual readout Dream-like calorimeters expressed interest in this device → **synergy with HiDRa (sub-task 3.3.1)**
- Regular meetings are held with representatives from Italian institutes to define the specifications of the future ASIC.

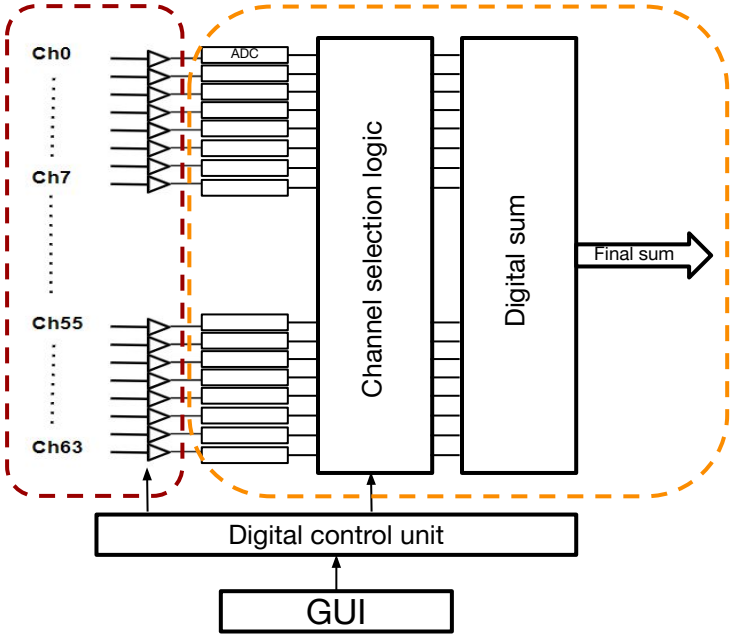
International institutes	Expertise
CERN	ALLEGRO project
Prague, Uni Bergen/ Gottingen, FOTON	SiPM readout
University of Valencia	RF amplifiers for SiPM readout

Italian institutes	Field of interest
INFN Pisa	Architecture development
Università di Siena	Architecture development
INFN Torino	ASIC design
INFN Pavia	Interface to HiDRa application
INFN Milano e Università dell'Insubria	Interface to HiDRa application

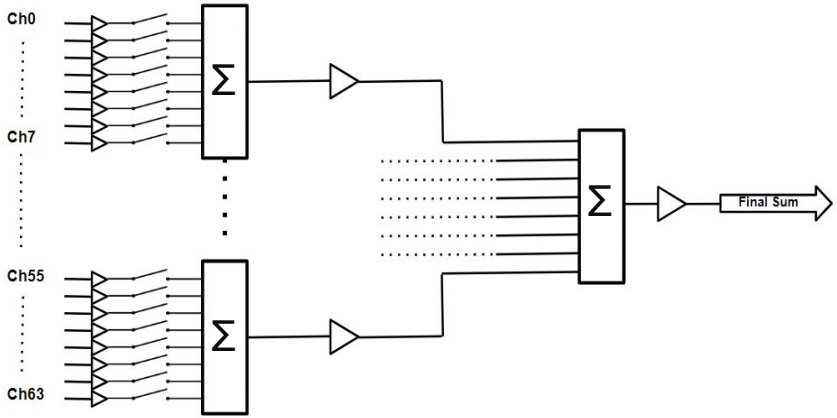
The table represents a possible division of tasks if the project moves forward.

Two possible designs

Hybrid: analog + digital design



Analog design



- **Same architecture as the discrete-component prototype already tested with a MA-PMT.**

Comparison between the two designs

Hybrid: analog + digital design

Pros:

- Possibility to integrate pre-existing blocks and reduce the design time.

Cons:

- The integration of complex custom ADCs, required by high conversion rates, could be challenging and time-consuming.

Analog design

Pros:

- Possibility to integrate commercially available ADCs.

Cons:

- Developing a completely new design may extend the overall timeline.

Iniziativa RD_FCC
con tag DRD6-TileCal
(WP3, sub-task 3.3.2 TileCal)

Richieste 2026

Sezione INFN Pisa

Anagrafica a Pisa

Nome	Ruolo	FCC FTE (%)
Chiarelli, Giorgio	DR	15
Cucinotta, Martina	Dottoranda	10
Leone, Sandra	PR	15
Pedreschi, Elena	Tecnologo	5
Scuri, Fabrizio	PR/Senior	30
Spinella, Franco	PR	5
TOTALE=		80

Richieste economiche per 2026

Missioni:

5 kEur per:

1-2 meetings/anno
1 settimana a Torino per 3 persone per training e collaborazione

Inventariabile:

3kEur per:

Una basetta CAEN A5251 - MPPC header adapter for A5202/DT5202
Un picoamperometro da banco
Un SiPM (Hamamatsu S13361-3050AE-08)

Consumi:

2kEur per:

Materiale di laboratorio comprendente un "case" per l'apparato di test, cablaggi, componentistica varia.

Conclusions and next steps

- INFN Pisa designed and tested a prototype of a new analog device for SiPM readout. The device enables configurable readout granularity for calorimeters while minimizing the number of output channels. Tests demonstrated excellent stability in pulse shape, linearity, and timing when summing multiple channels.
- **Encouraged by these results, we plan to develop an ASIC with the same features for reading 64-channel SiPMs.**
- To gain experience, initial tests on SiPM readout began in the past weeks in the ATLAS Pisa lab.
- The project is included in WP3 of DRD6 (3.3.2 TileCal) and is part of the FCC Pisa group activities.

Next steps:

- Conduct tests of the prototype using a single-channel SiPM (FBK);
- Design a PCB to adapt a 64-channels SiPM (Hamamatsu S13361-3050AE) to the prototype input;
- Test the prototype using the 64-channel SiPM, also in preparation for a possible test beam in 2028, should the ASIC not be ready by then.
- Select the ASIC design
- **Organize an in-person meeting between the Pisa group and representatives of the involved Italian institutions by October 2025.**

Backup

Milestones & deliverables

D Number	M Number	Title	Description	Start date	End date	Estimated cost [kCHF]	Received Funding [%]	Execution Status
	M3.17	Detector Design	- Performance studies and geometry optimisation with simulation - Mechanical design of a prototype module for beam tests	2024	2026			ongoing
	M3.18	Optical Instrumentation	- R&D of new scintillating materials - Tile+fibre+SiPM coupling - Fibre preparation for the prototype	2024	>2026			ongoing
	M3.19	Detector Readout	- Readout electronics for SiPMs - Data Acquisition and Analysis Software	2025	>2026			planning
D3.13		**Prototype Sub-Module 1**	**Prototype sub-module for beam tests (longitudinal containment)**	**2024**	**2028**	**421**	**61**	**planning**
	M3.20	Test Beam Results	Results from the beam tests and publication	2029	2030			planning
D3.14		**Prototype Sub-Module 2 and 3**	**Set of prototype sub-modules for beam tests (lateral containment)**	**2029**	**2030**	**740**	**7**	**planning**

General architecture for the new device

- The solutions currently available on the market involve the digitization of all channels *

  ….but the cost of such a device could be unaffordable due to the very large number of channels to be digitized

Advantages:

- Apply digital filters to dump the noise
- Avoid problems of signal synchronization
- Apply digital weights in the digital sum of different channels

- We want to invert the concept flow chart:

  ➡ **first make an analog sum of selected subsamples of readout channels, than convert only the desired sum(s)**

- The challenge is to avoid distortions of the time profile in the resulting analog sum and to keep at the same time all configuration flexibility that the other concept allows.

*MUSIC ASIC architecture

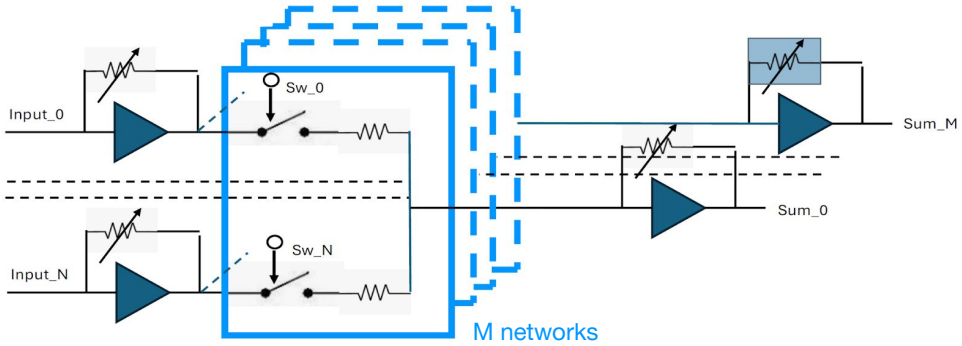
Features and general architecture for the new device

- **The key feature of this device, which differentiates it from existing commercial devices, is its ability to perform the analog summation of any configurable subset of input channels**
- Let's introduce the building block diagram for a new concept device with full scalability:

  1) A first stage with variable gain fast (2 GHz BW) amplifiers to allow for input weighting,

  2) A second stage with M equal resistive networks with N fast analog switches remote controlled (N is the number of analog inputs, M is the number of analog sums),

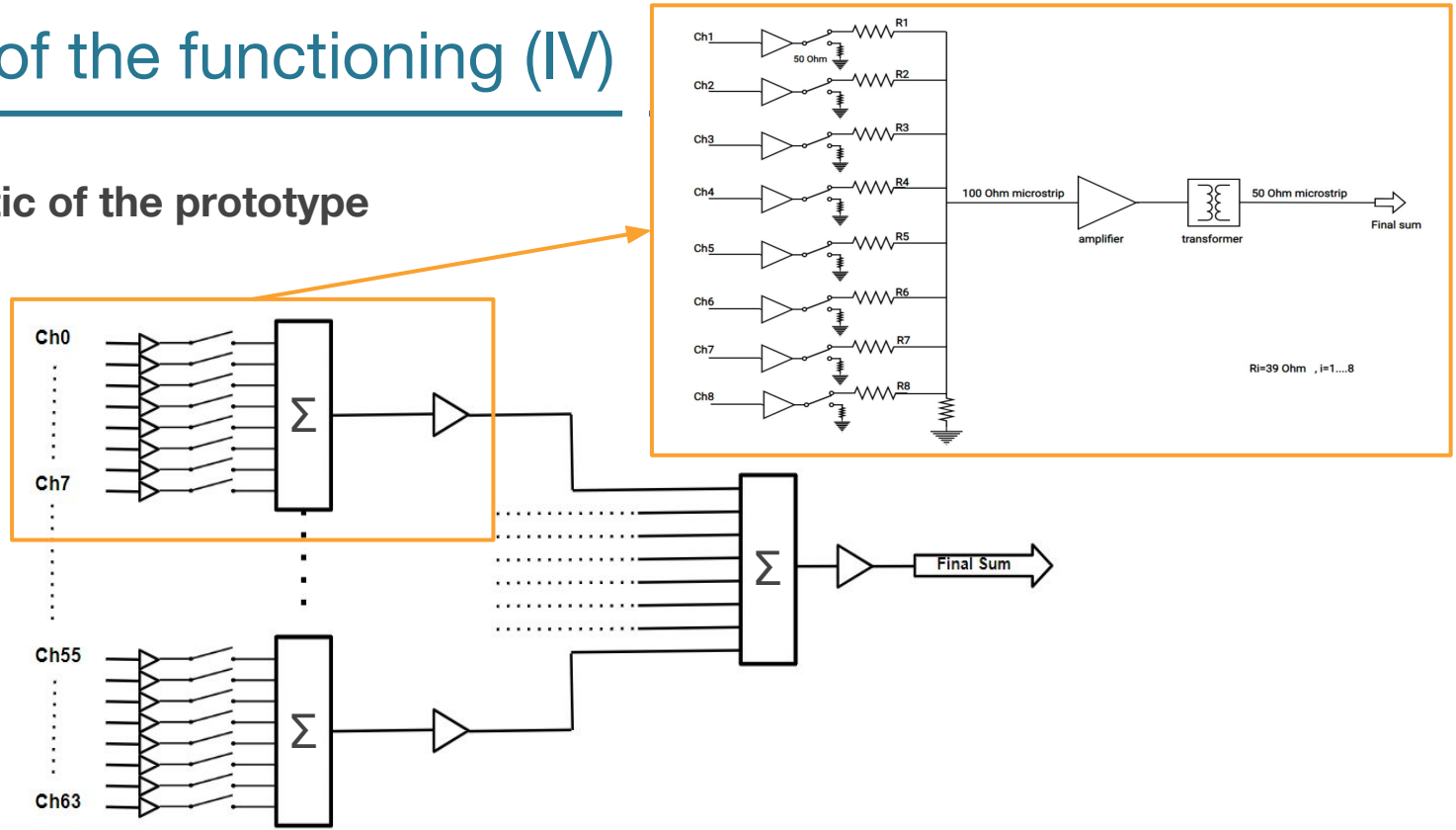
  3) A final stage performing the M analog sums with variable gain fast amplifiers to cope with the dynamical range of the user selected ADC.



What was done?
A prototype for this type of readout with high-bandwidth integrated circuits was designed, built and tested at INFN Pisa.

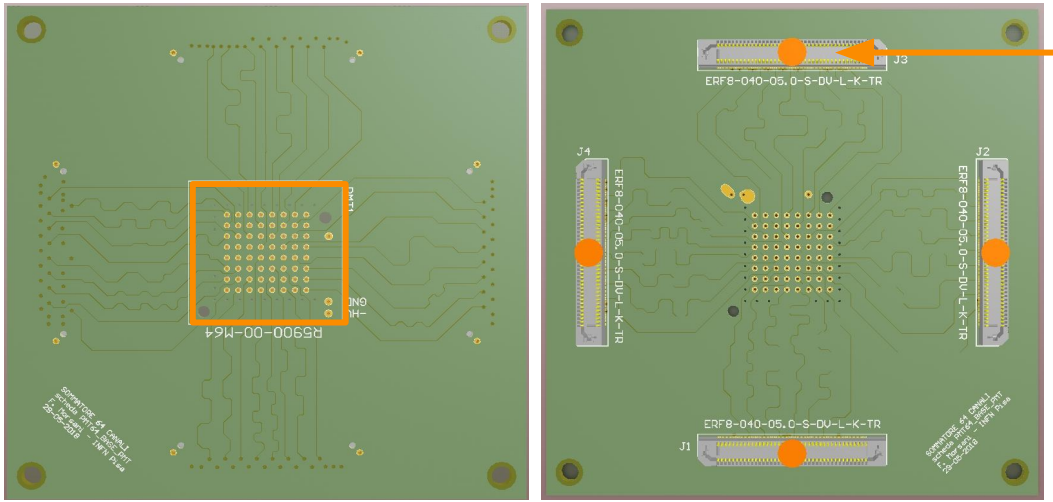
Description of the functioning (IV)

Circuit schematic of the prototype



➡ The 64 amplified readout channels are fed to eight 8-channel resistive summing networks.

Prototype description (1)

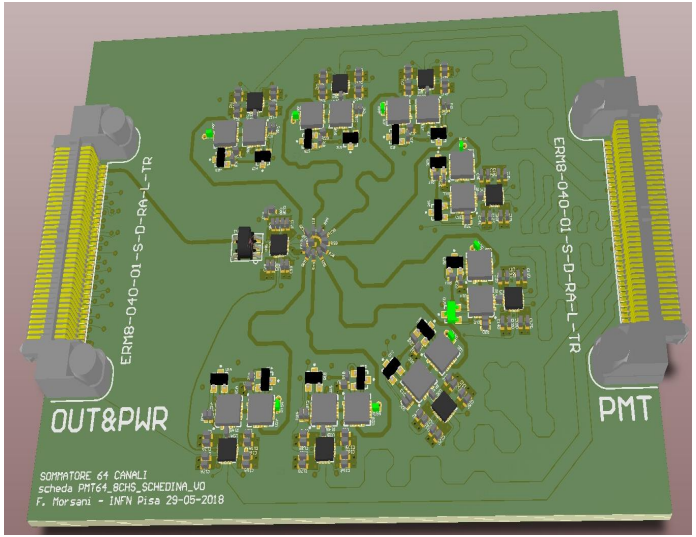


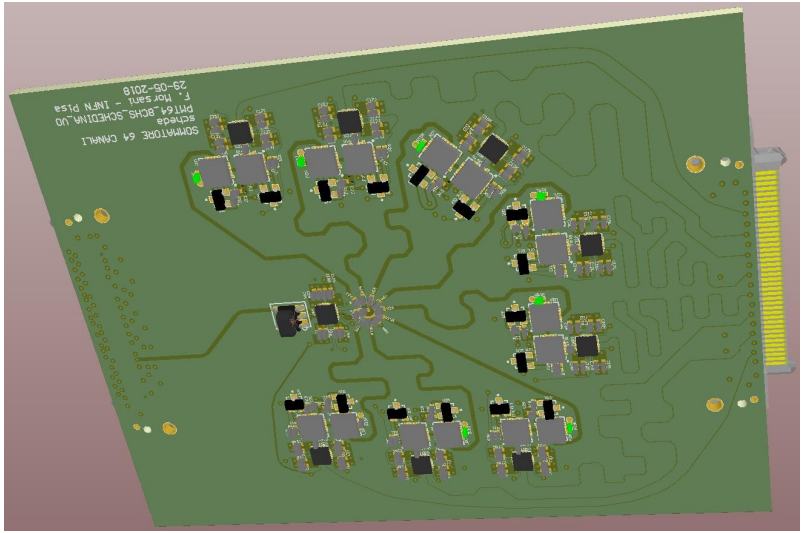
Board-to-board connector

First base board (front and back)

- The prototype is designed to host a 64-channel MAPMT with a sensitive area of 18 × 18 mm^2 and an anode pitch of 2.54 mm.

Prototype description (2)

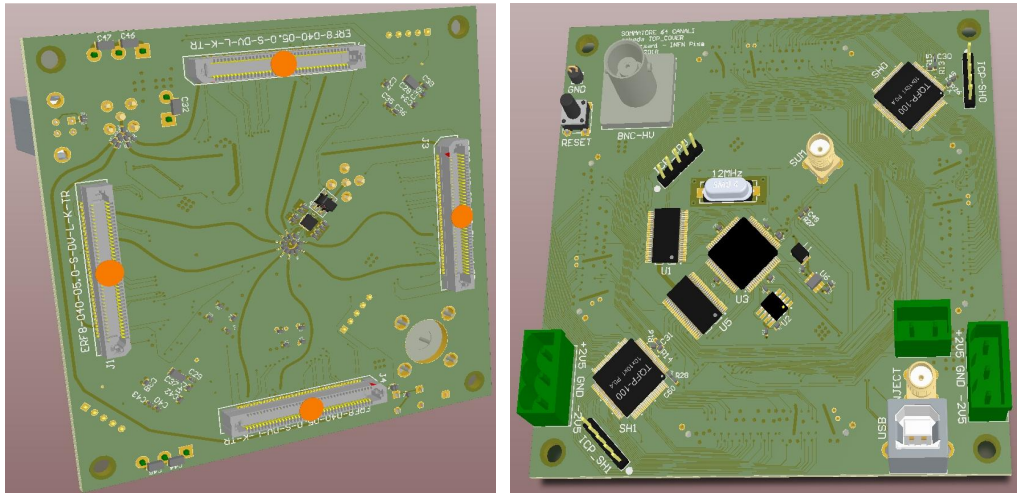




Lateral board

- 8 single-channel amplification systems
- 1 resistive network to perform analog sum of 8 channels

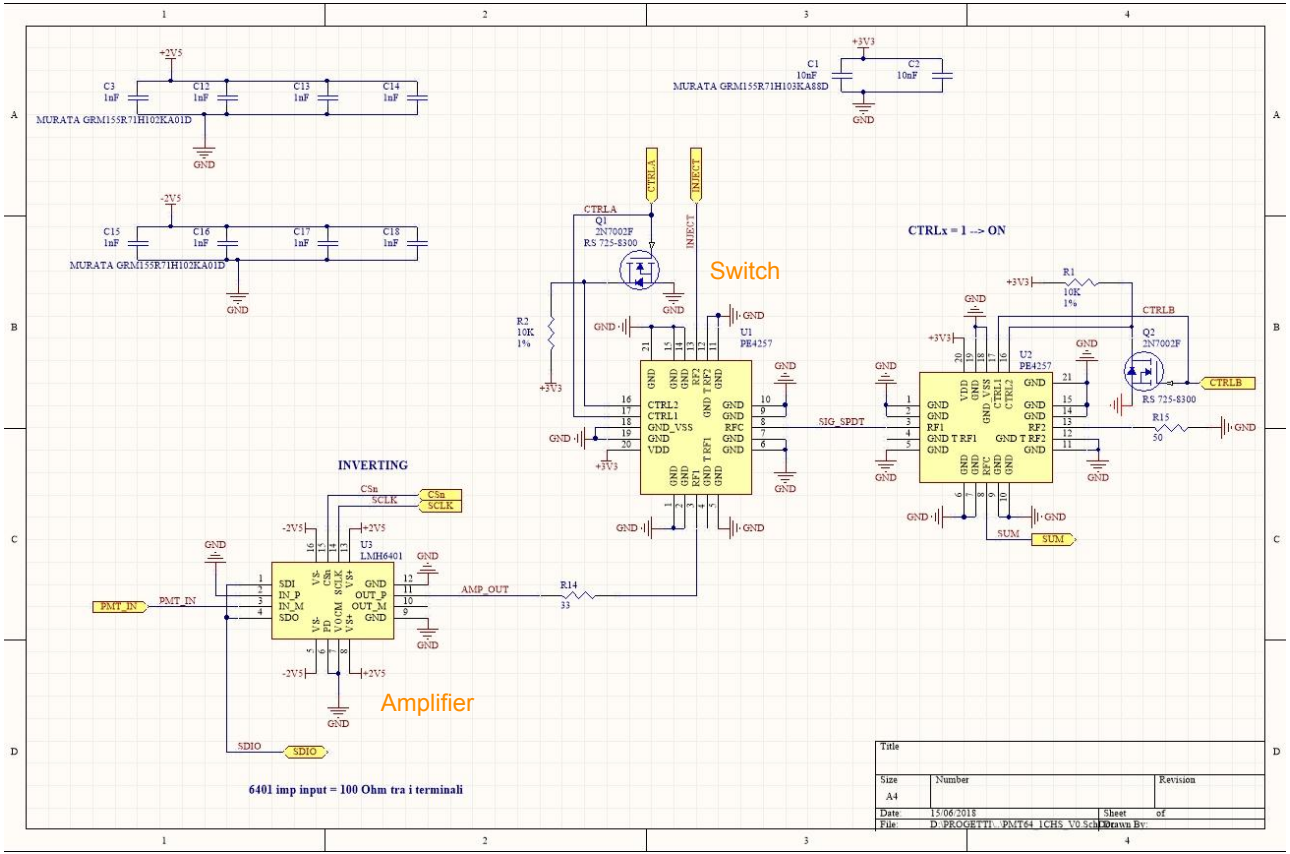
Prototype description (3)



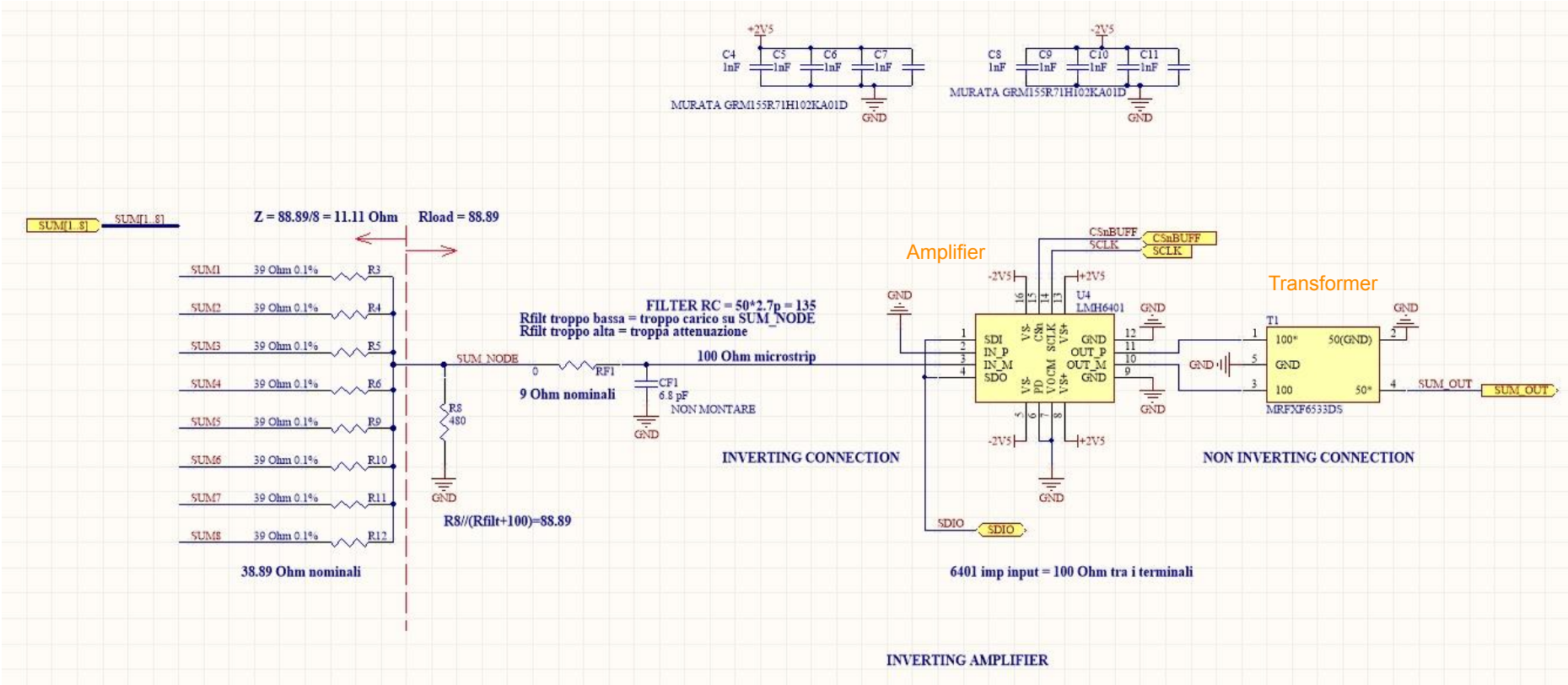
Second base board (front and back)

- Final sum stage (final resistive network + amplifier)
- Microcontroller and logic level shifters
- USB interface
- BNC-HV

Single channel amplification circuit

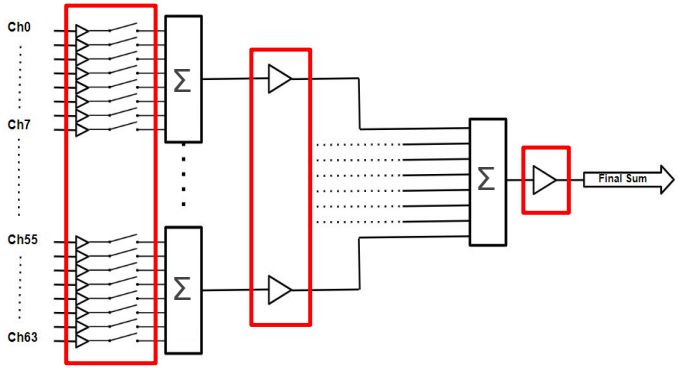


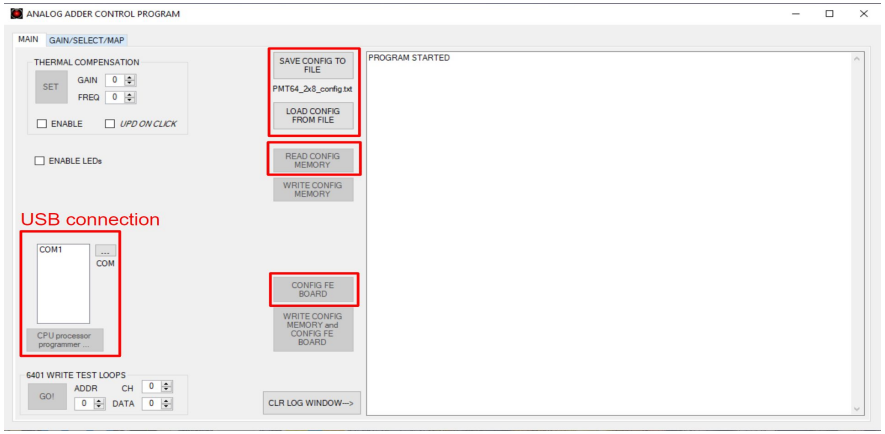
8-channels summing network

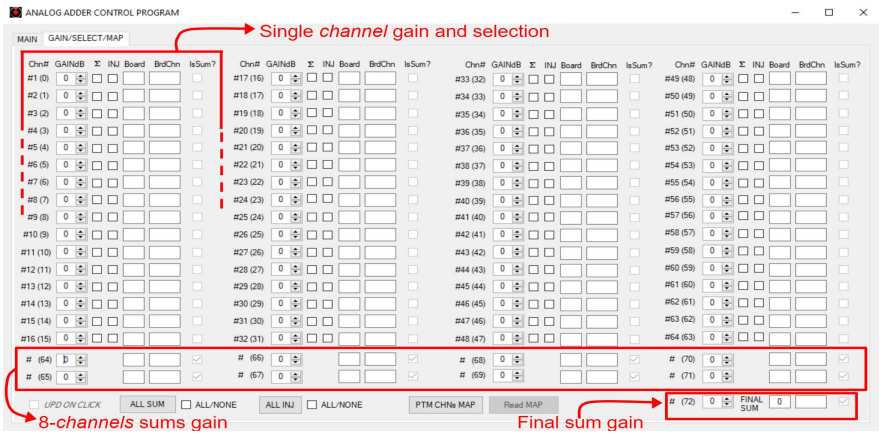


GUIs

- The selected channels and all amplifications can be set through a GUI, allowing to establish USB connection with the prototype and to upload the selected configuration for the final sum.







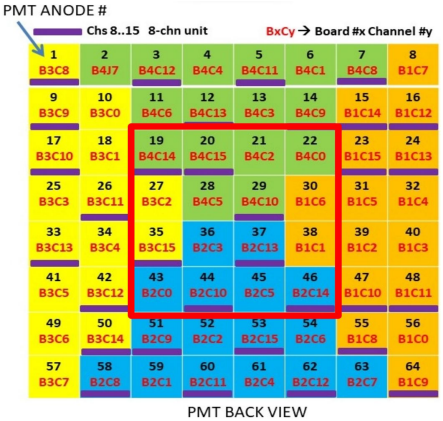
Prototype tests: introduction

- The prototype has been tested in Pisa in terms of pulse shape stability and linearity of the analog sum of an arbitrary number of channels.

- Various tests were done with two different experimental setups:

  ➡ test of the 16 central readout channels injecting an input signal

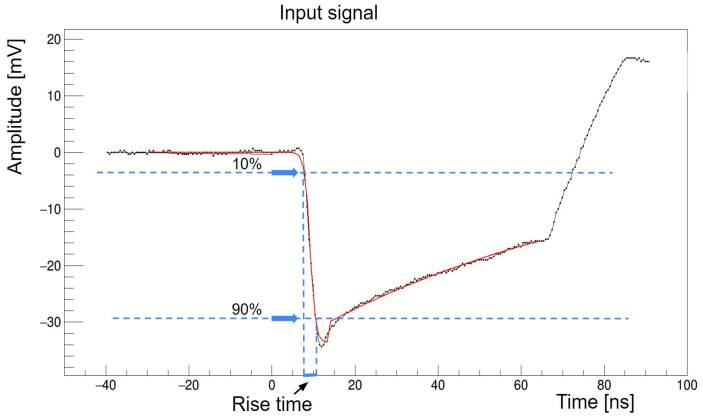
  ➡ test of the readout system using a MAPMT and a laser system



Readout prototype tests with signal injection

Input signal

- Input signal used to test the 3 readout prototype amplification stages.
- Generated by differentiating a square pulse with a 60 pF capacitor to simulate the signal produced by a PMT.



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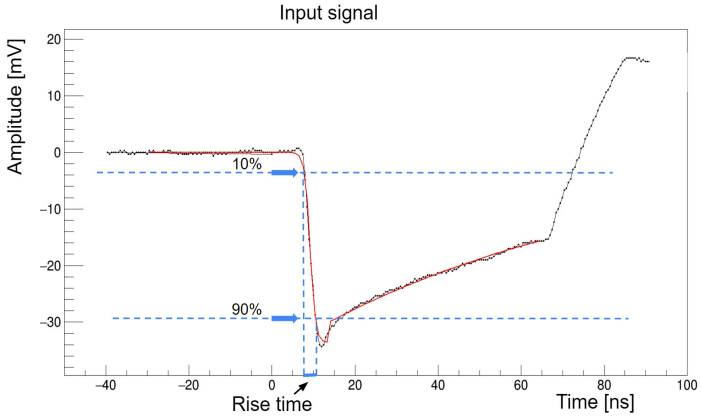
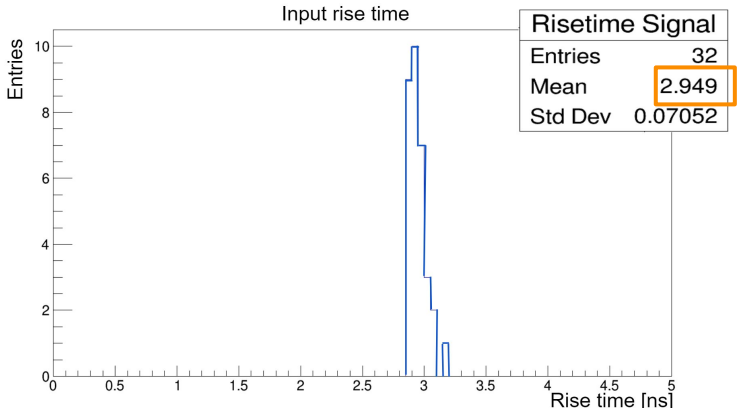
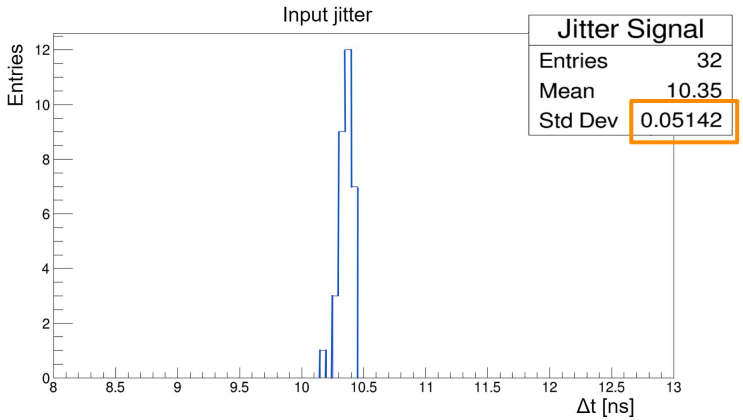
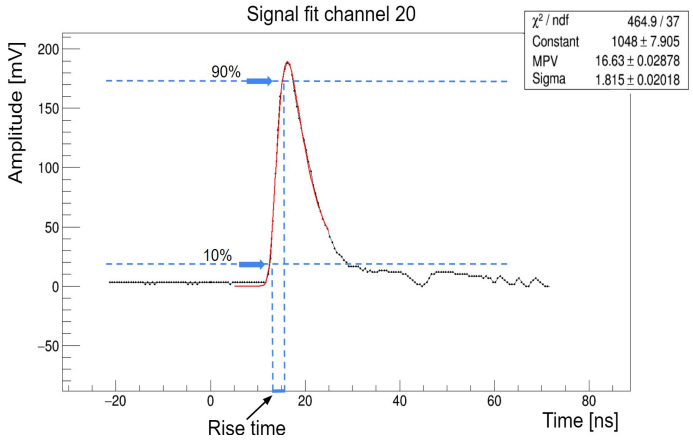




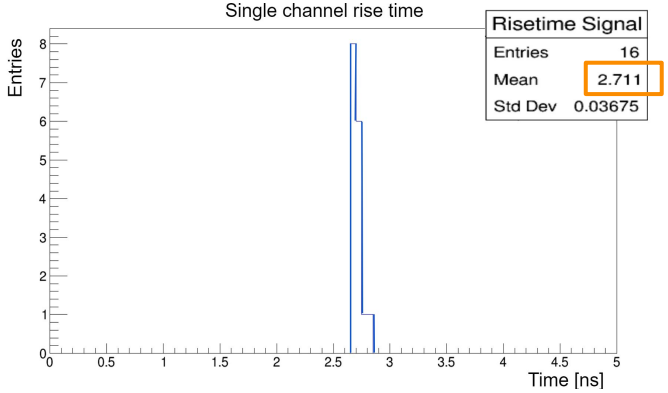


Single channel output signals: rise time

- Landau fit function to calculate the amplitude and the baseline of the signal for the rise time evaluation.

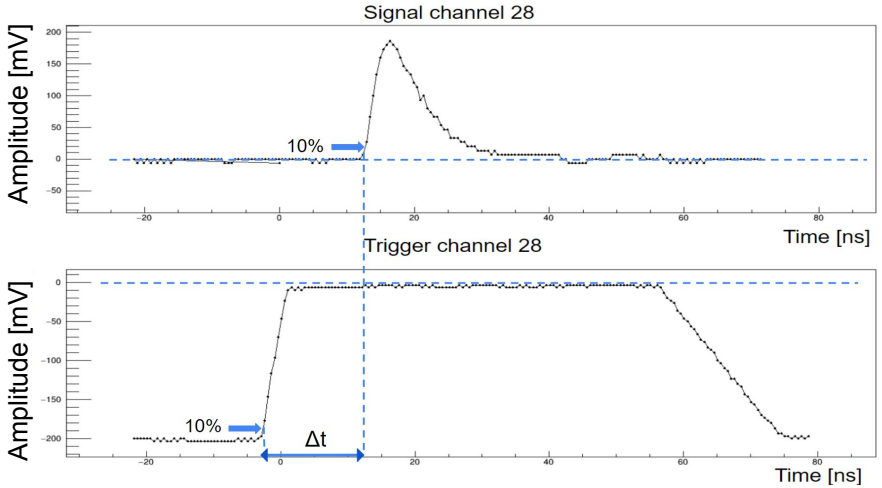


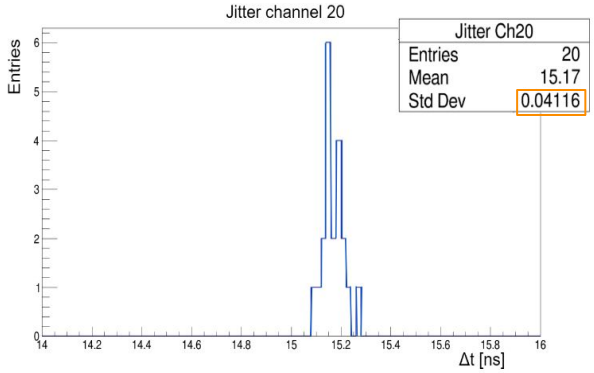
- Output signal rise times are ~ 2.7 ns.

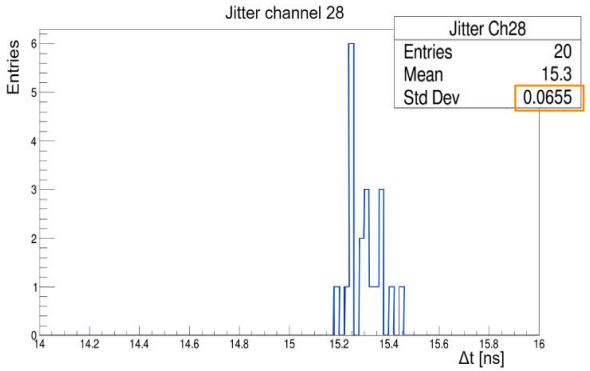


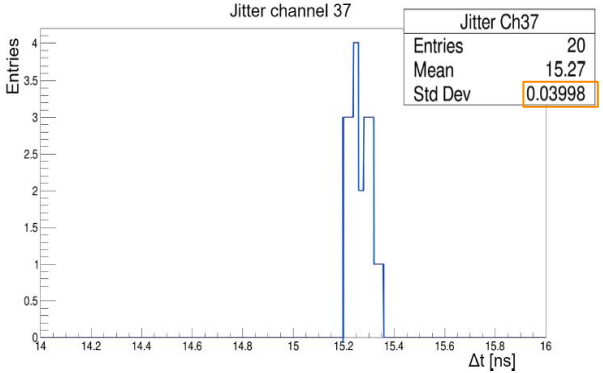
Single channel output signals: jitter time

- Jitter values ~ 50 ps.
  - ➡ Good temporal stability for this type of readout system;
  - ➡ Output jitter compatible with the input jitter ⟶ good data transmission through the readout prototype.

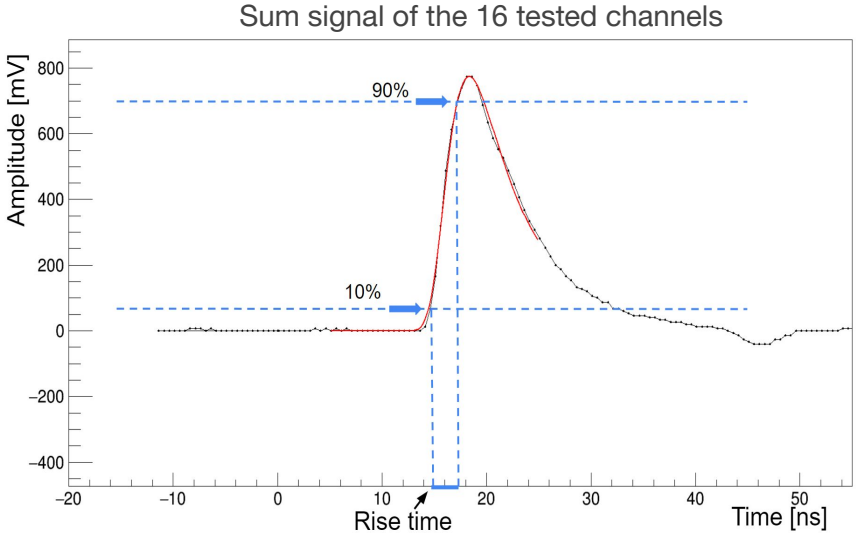


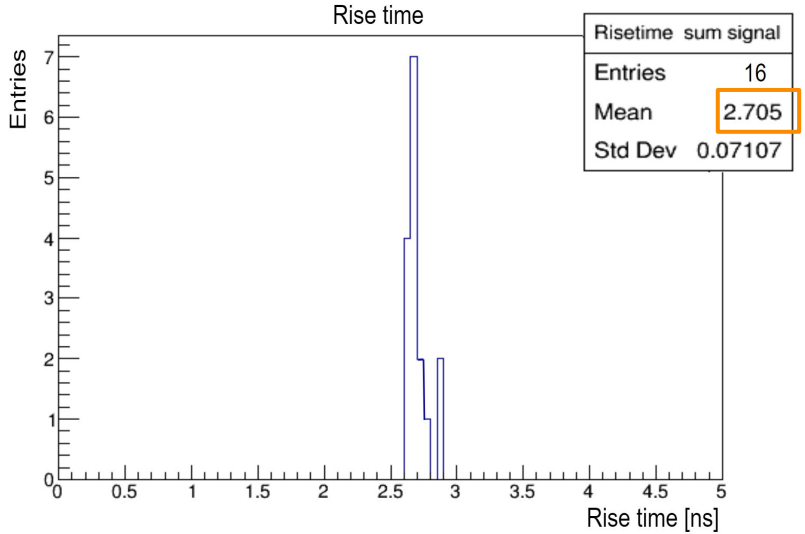






Signal stability as a function of the number of channels

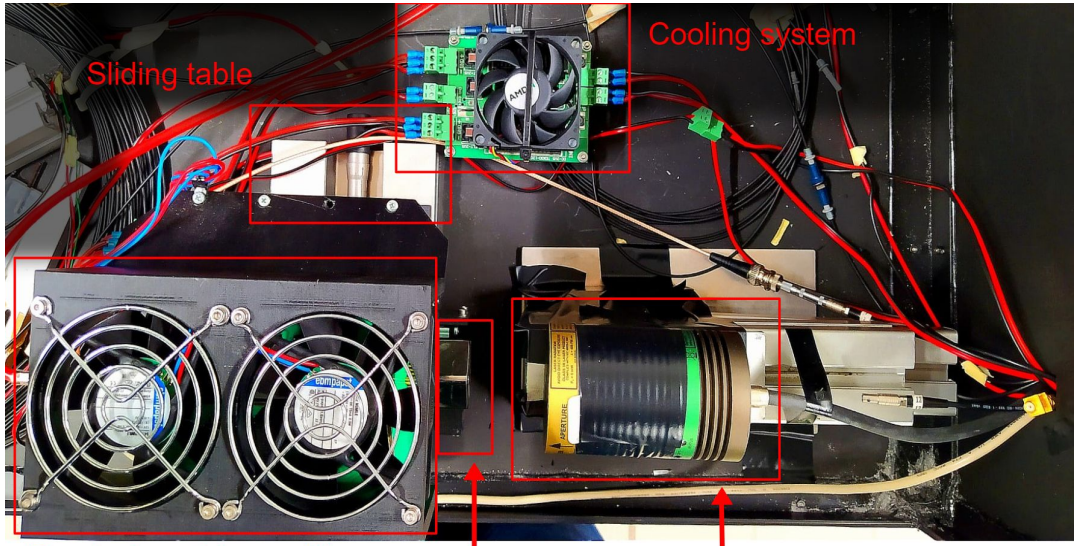


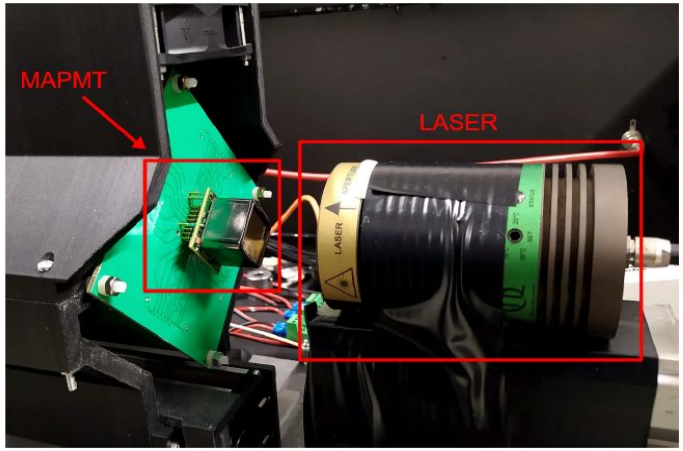


- Rise time value compatible within one standard deviation with the rise time of the individual channels.
- The operation carried out by the resistive networks to sum the analog signals does not alter the shape of the outputs.

Readout prototype tests with a MAPMT and a laser system

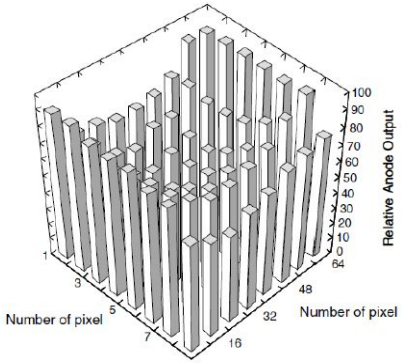
Test with MAPMT and laser: experimental setup

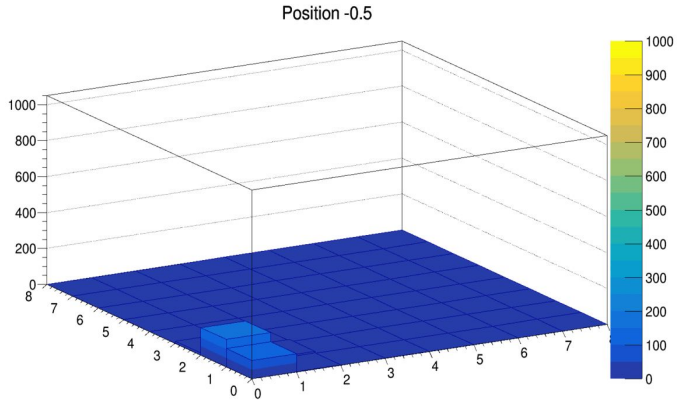


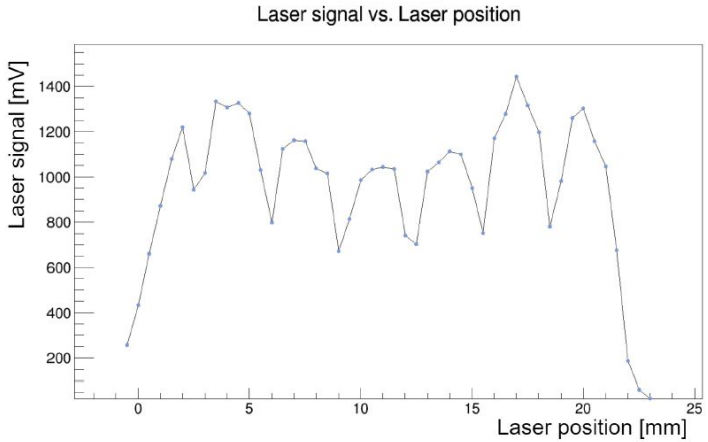


Scan of the MAPMT photocatode with a laser system

- The beam spot moves along the photocathode diagonal.
- Acquired the signal amplitudes for all 64 channels across 48 positions of the laser spot along the diagonal.
- Spot dimensions and optical crosstalk → the laser signal spreads in more than 1 channel.







Prototype tests conclusions

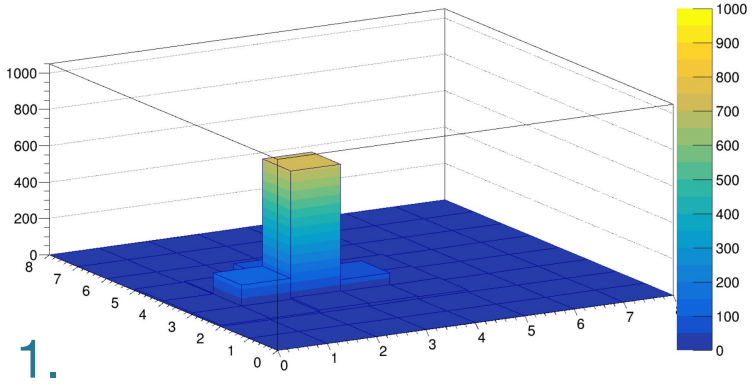
- The readout prototype guarantees shape stability, in the analog sum of the signals (rise times ~ 2.7 ns);
- The resistive summing networks do not alter the shape of the outputs;
- Jitter time ~ 51 ps, good data transmission;
- Observed coupling effects between channel → minimal effect that does not alter the correct functioning.

More information: https://etd.adm.unipi.it/t/etd-02052024-191133/

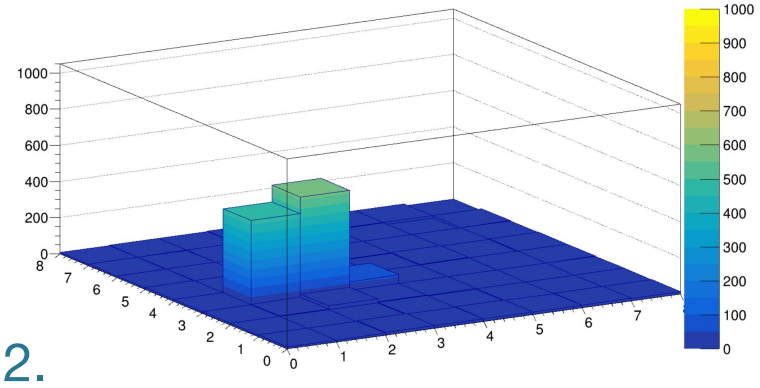
Two specific cases

1. The laser spot is centered on a given anode pixel of the MAPMT.

2. The laser spot is almost equally shared on two adjacent channels.



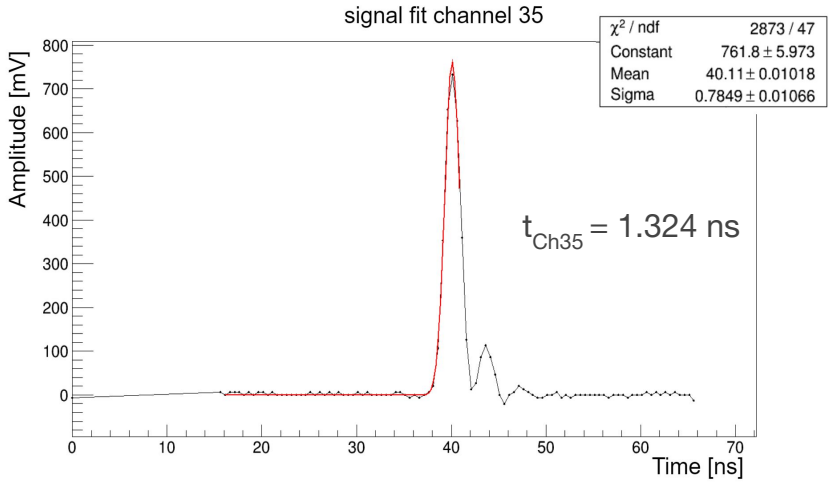
1.



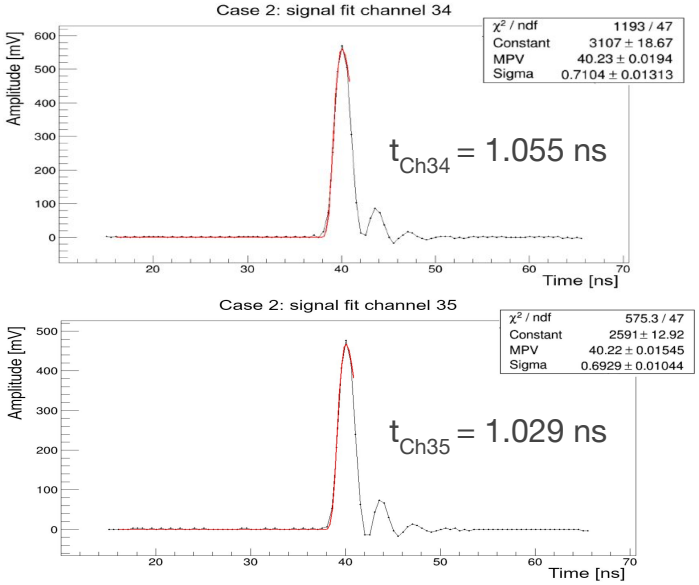
2.

Single channel signals

1.



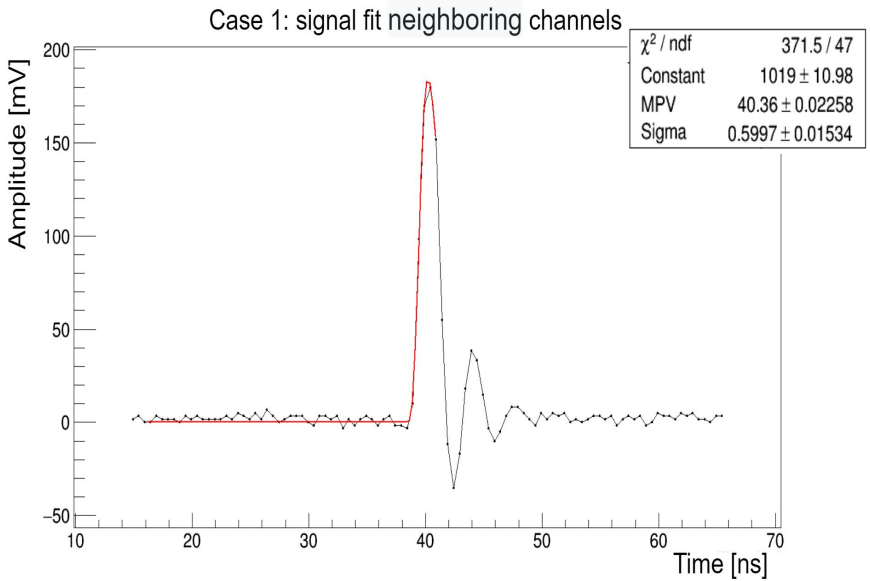
2.



The rise time of *Ch35* is larger when it alone receives the most signal relative to the case when the signal is almost equally shared between *Ch34* and *Ch35*.

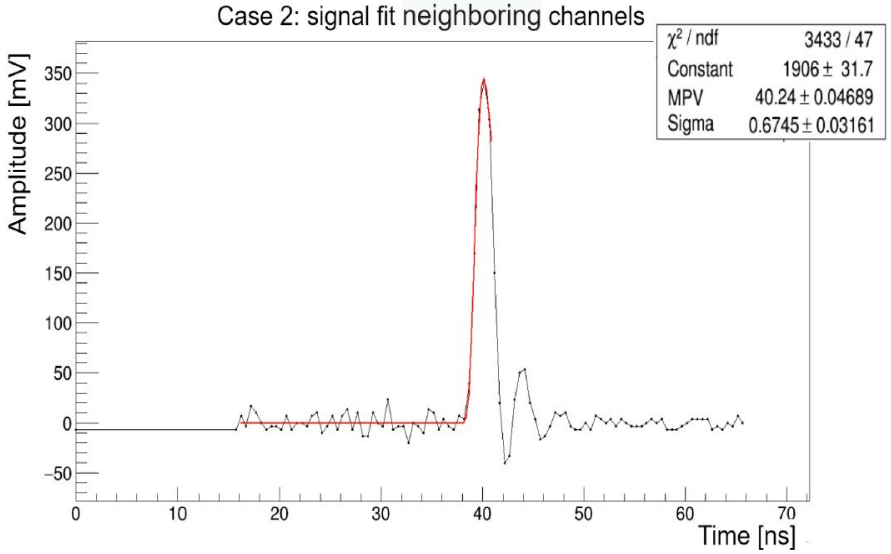
Analog sum of neighbouring channels

1.



$t_{sum}(8) = 1.002$ ns

2.

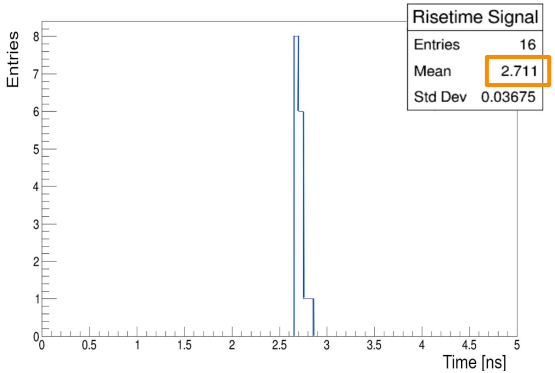


$t_{sum}(10) = 0.890$ ns

In both cases the signal rise time is larger for individual channels detecting the main part of the signal relative to the sum of the neighbouring channels.

Prototype tests results

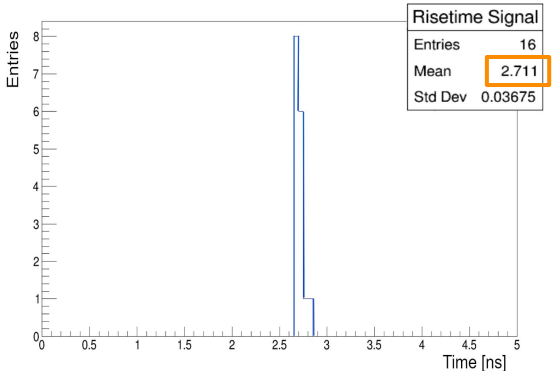
- The readout prototype guarantees pulse shape stability and linearity in the analog sum of the signals (rise times ~ 2.7 ns);



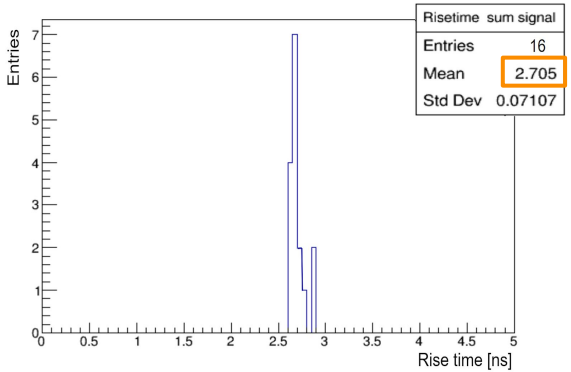
Single channel rise time distribution

Prototype tests results

- The readout prototype guarantees pulse shape stability and linearity in the analog sum of the signals (rise times ~ 2.7 ns);
- The resistive summing networks do not alter the shape of the outputs;



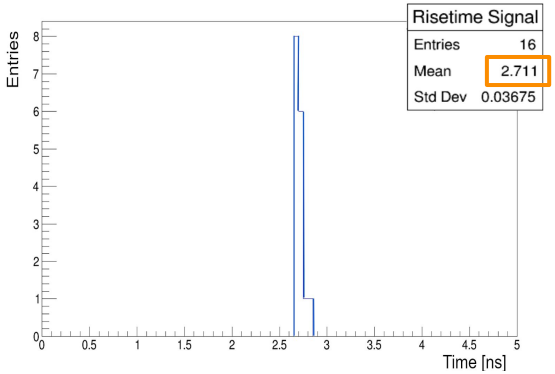
Single channel rise time distribution



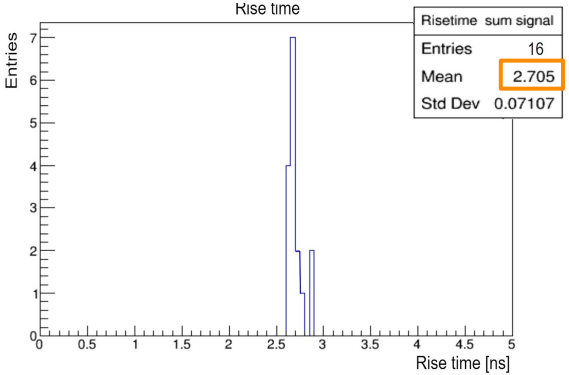
Distribution of the rise time of the analog sum for an increasing number of channels

Prototype tests results

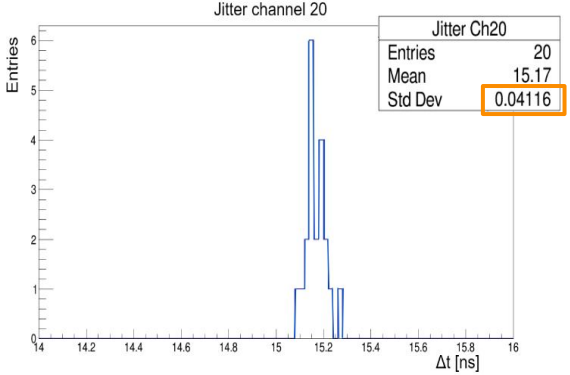
- The readout prototype guarantees pulse shape stability and linearity in the analog sum of the signals (rise times ~ 2.7 ns);
- The resistive summing networks do not alter the shape of the outputs;
- Jitter time ~ 40 ps, good data transmission;



Single channel rise time distribution



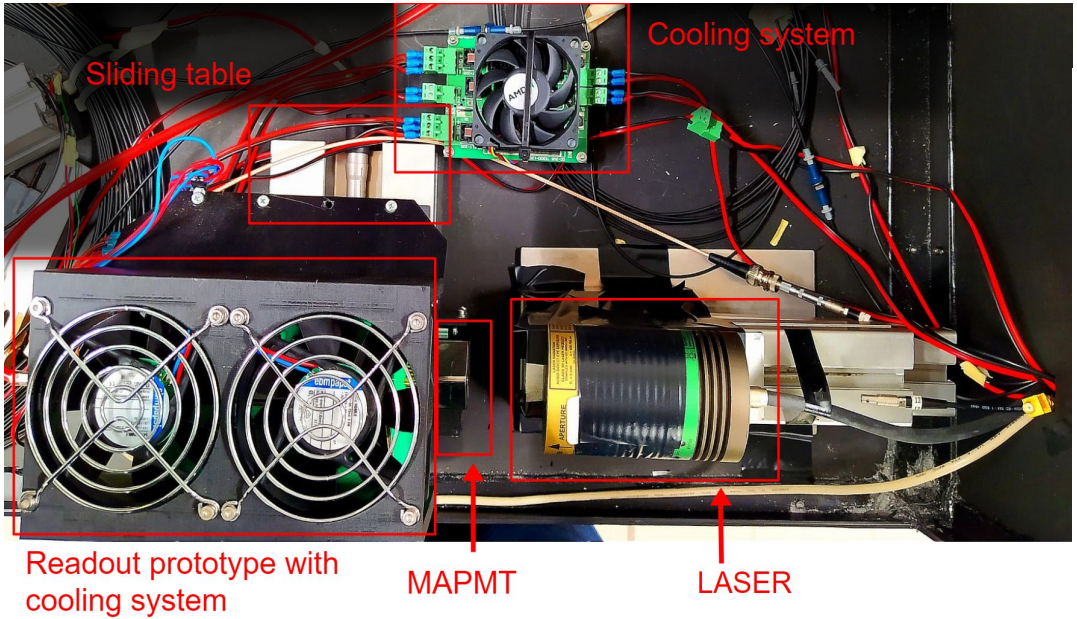
Distribution of the rise time of the analog sum for an increasing number of channels

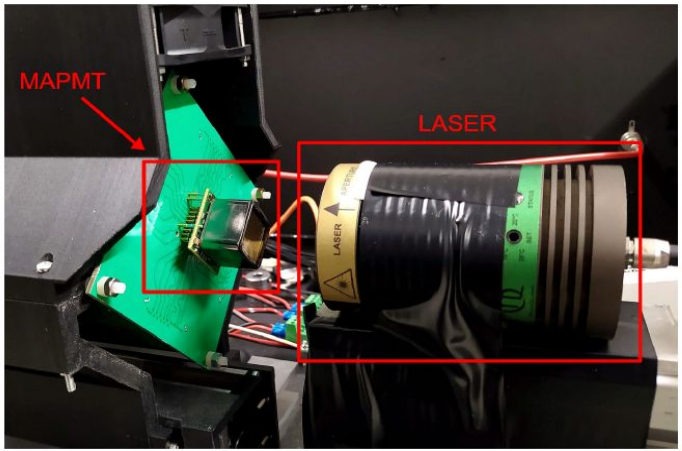


Channel 20 Δt distribution for jitter estimation

Tests with a MAPMT and a laser

- Observed coupling effects between channel testing the prototype with a MAPMT, whose channels are excited with a laser.

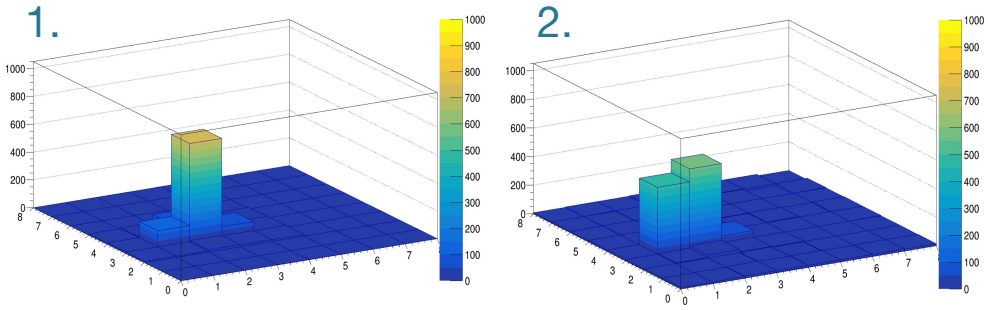


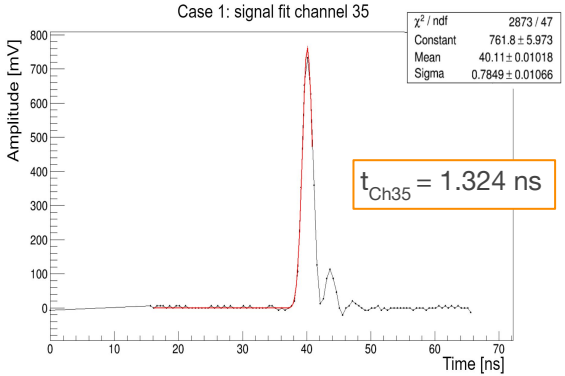


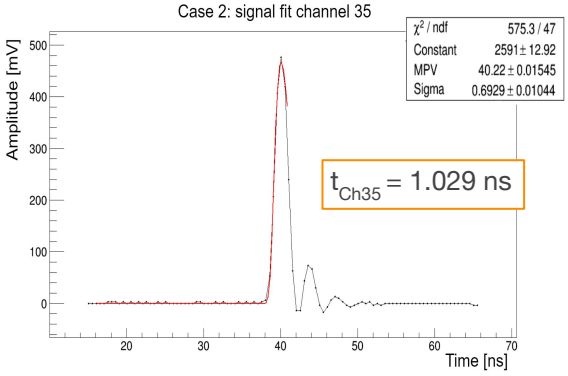
Two specific cases

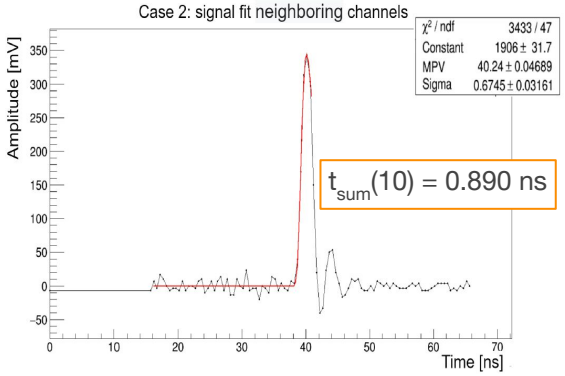
1. The laser spot is centered on a given anode pixel of the MAPMT.

2. The laser spot is almost equally shared on two adjacent channels.









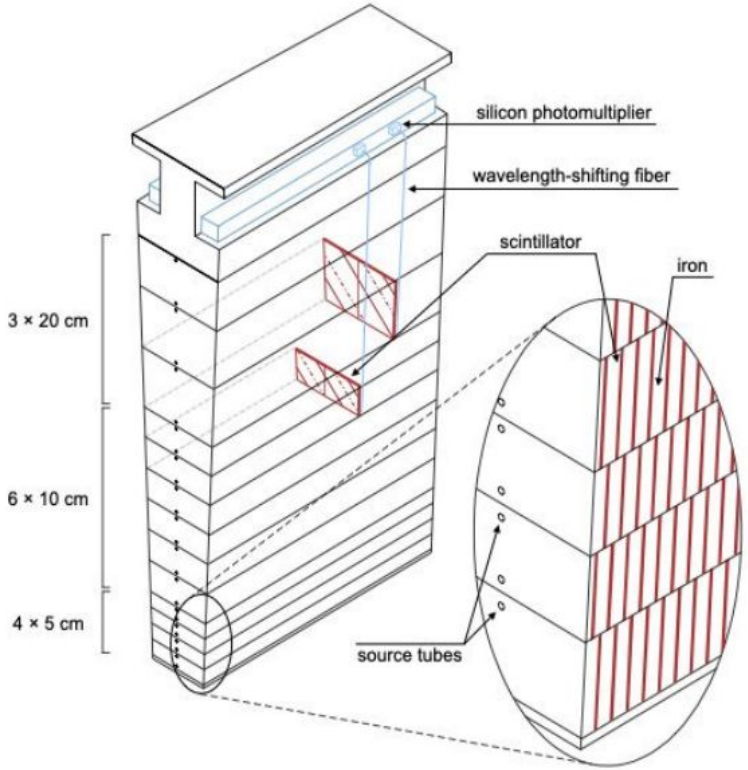
- **Observed coupling effects between channel → minimal effect that does not alter the correct functioning.**

ALLEGRO HCAL

- A possible application of this device is the ALLEGRO HCAL barrel, which involves a readout system based on **tile + fiber + SiPM**.
- Design based on alternating steel and scintillator layers (5 mm absorbers, 3 mm scintillators)

  Barrel:13 radial layers
  Endcap: 6 / 9 / 22 radial layers

- 128 modules in ϕ, 2 tiles per module
  $\Delta\phi$ = 0.025
  $\Delta\eta$= 0.022 (grouping 3-4 tiles)
- **Performance studies ongoing**
- Potential application in any calorimeter with SiPMs, which are expected to be widely used in future calorimeters.



A versatile analog ASIC

- The basic version can be enriched with additional features to meet the needs of future users.
- For example: signal timing optimization, two amplification level and charge integration for **ALLEGRO HCAL**