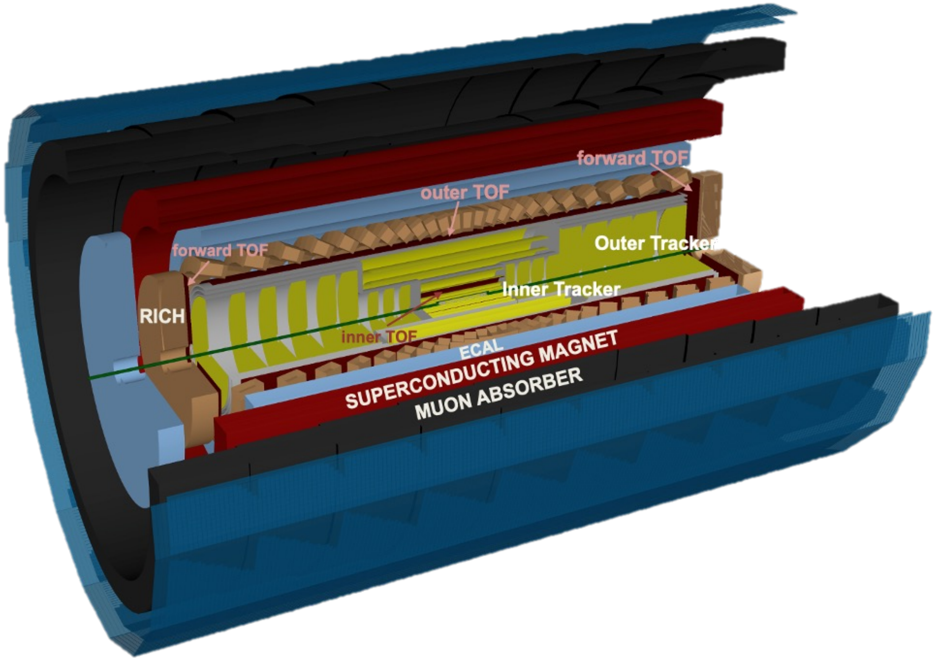
ALICE

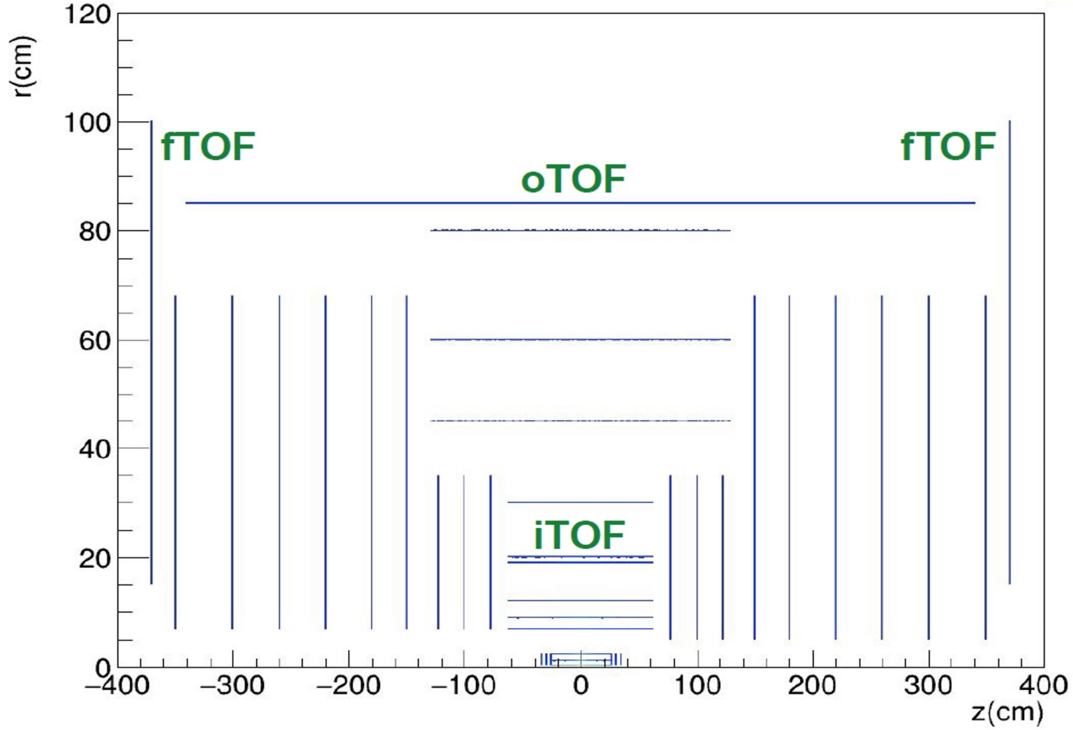


ALICE 3 TOF: ATTIVITÀ IN CORSO E PROSPETTIVE FUTURE

S.Bufalino, M.Colocci, A.Rivetti
(grazie al contributo di molt* collegh*)

Riunione referee ALICE – Roma, 9-10 luglio 2025

ALICE 3 TOF: layout



International Collaboration with INFN Leadership:
Brasil, South Africa, Japan*, China*, Netherlands*
Interest from India and Rumenia
*(new institutes)

INFN Units and Universities involved: Bologna, Torino, (Unito, UPO and Polito) and Trento

Table 10: TOF specifications. The Outer TOF barrel length, the Forward TOF radius and the hit rates have been updated with respect to the LoI values.

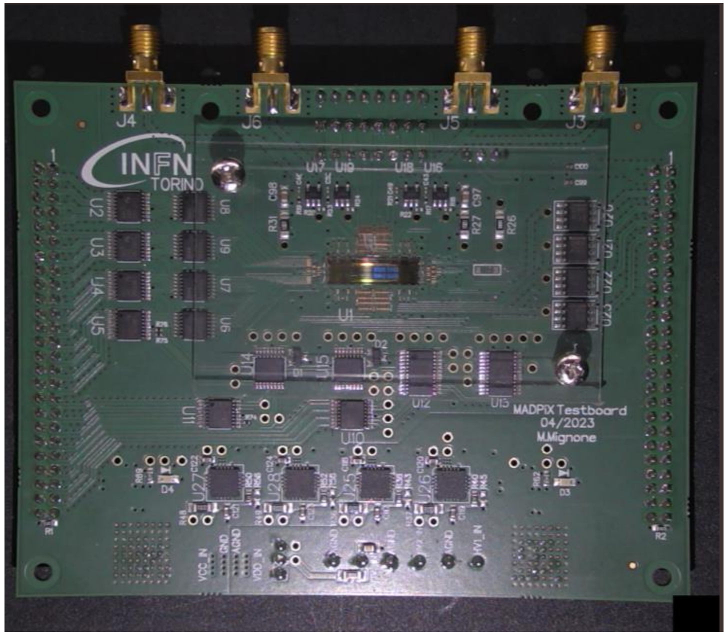
	Inner TOF	Outer TOF	Forward TOF disks
Radius (m)	0.19	0.85	0.15 to 1.0
z range (m)	−0.62 to 0.62	−3.50 to 3.50	±3.70
Area (m^2)	1.5	37	6
Acceptance	$\|\eta\| < 1.9$	$\|\eta\| < 2$	$2 < \|\eta\| < 4$
Granularity (mm^2)	1×1	5×5	1×1 to 5×5
Hit rate (kHz/cm^2)	200	15	280
Material thickness ($\%X_0$)	1 to 3	1 to 3	1 to 3

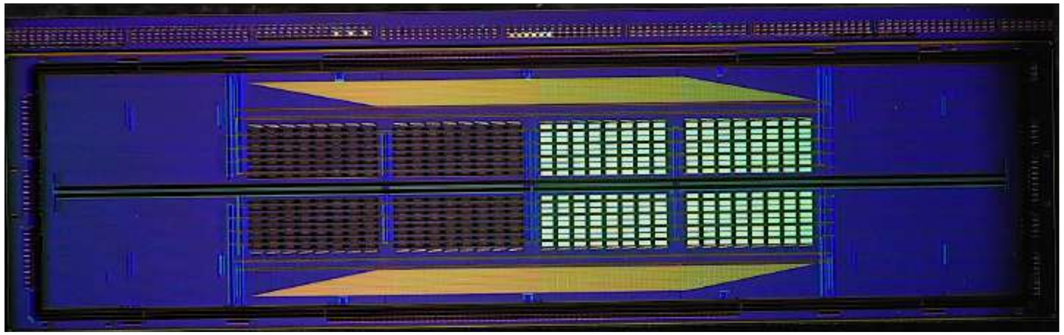
- Silicon detector with tracker-like mechanics
- Key challenge: 20 ps timing resolution
- Moderate constraints on rates, space resolution, material budget

R&D strategy in 2024-2025

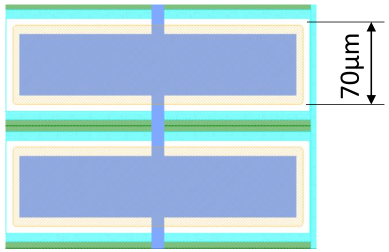
- Focus on **monolithic sensors**
  - need to push the timing resolution well beyond the state of the art
- Chosen approach: add a gain layer to a standard CMOS process
  - synergy with the INFN ARCADIA project (LF 110 nm): re-use of existing masks with custom substrates and addition of a gain layer
  - 3 short loop runs so far (1 in 2023, 2 in 2024)
  - CMOS-LGAD chip with sensor and front-end electronics (Madpix)
- Synergy advantages :
  - Implementation with a novel sensor concept at a very reduced cost
  - Provides enough information to understand key issues
  - Fine-tuning of sensor simulations in TCAD with inputs from measurements
- Synergy drawbacks:
  - Constraints on collection electrode geometry
  - Not possible to reach the ultimate time resolution without a full set of dedicated masks
    → full Engineering Run needed in the near future

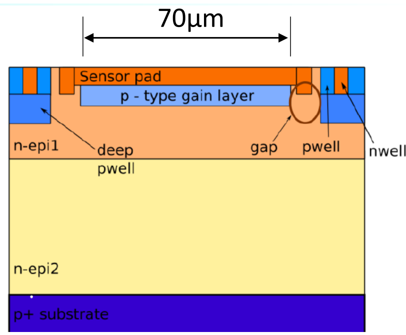
The MadPix test structure





- 8 matrix with 64 pixels each
- Chip size: 16.4 mm x 4.4 mm
- Embedded front-end and output buffers
- Oscilloscope readout

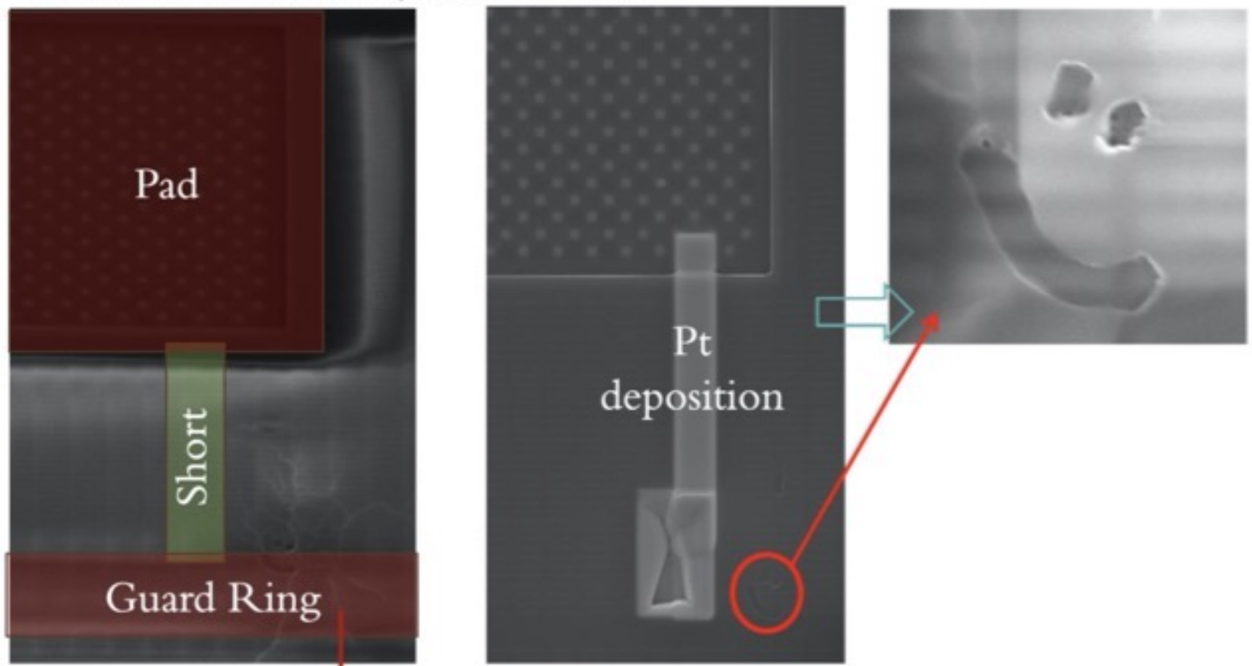




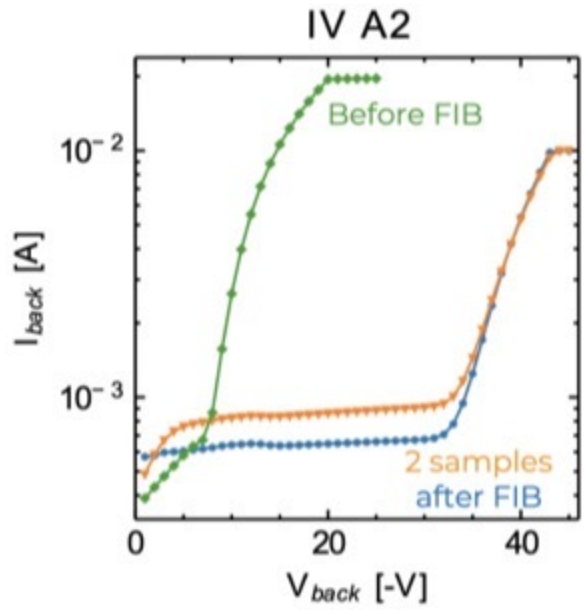
- Characterization
  - In the lab (electrical, source, lasers)
  - Beam tests

Reducing back-side currents

Focused Ion Beam Facility at INRIM Torino

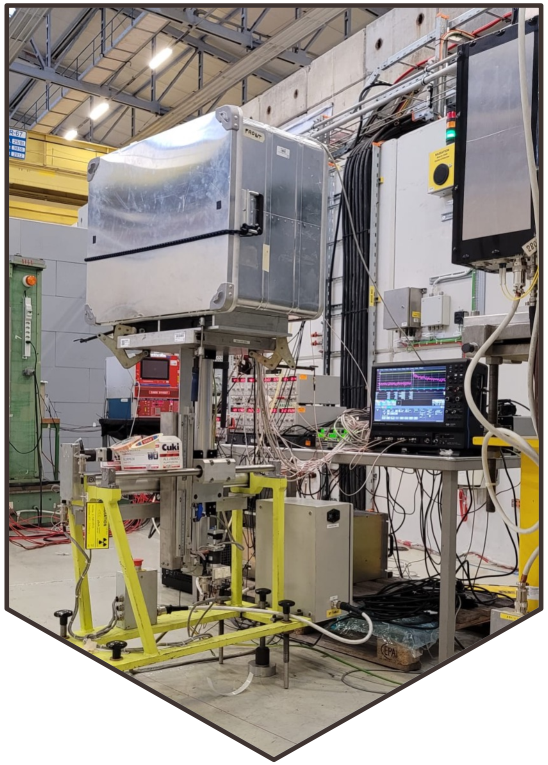


Floating guard ring to be shorted

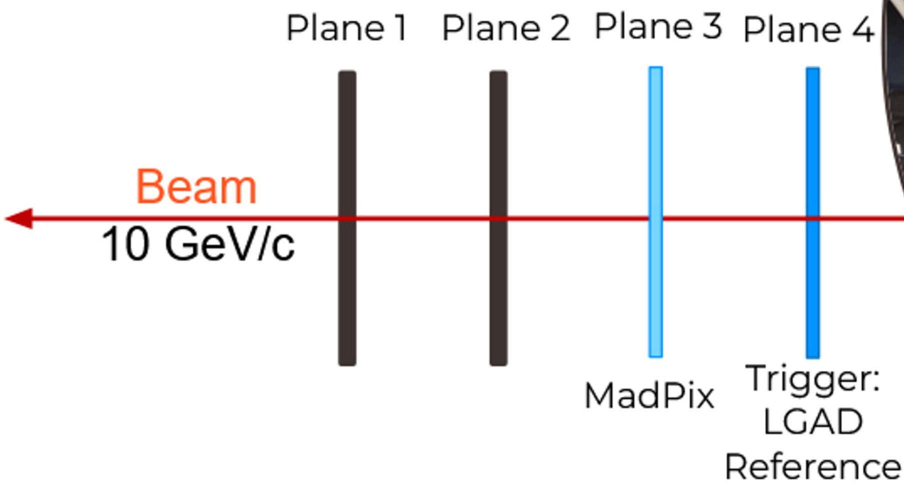


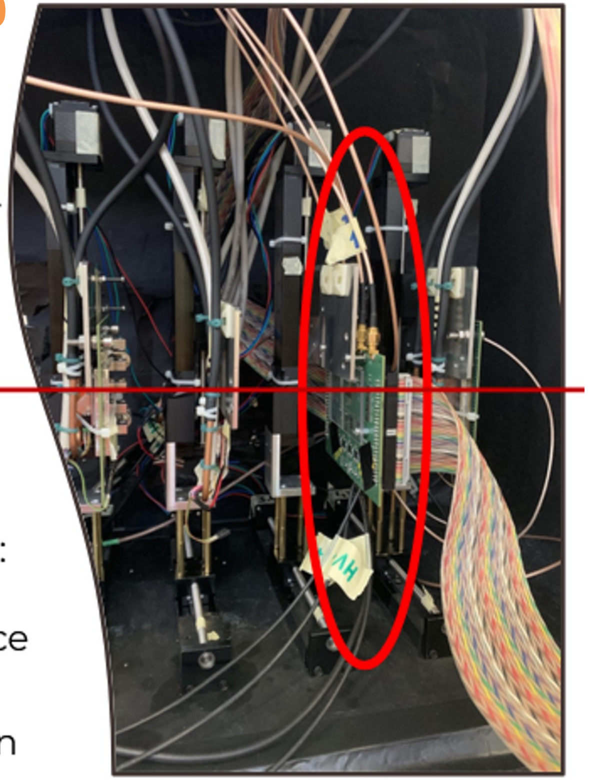
Backside current lowered of
2 order of magnitude

Beam tests at CERN PS



Beam-test setup (INFN-BO-TO) @ CERN-T10





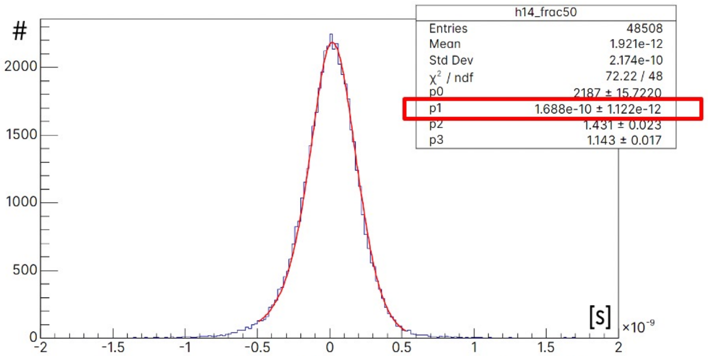
- 4 planes telescope
- MadPix linked to a Xilinx FPGA controlled in control room
- Readout → Oscilloscope for signal acquisition

Results: one year ago

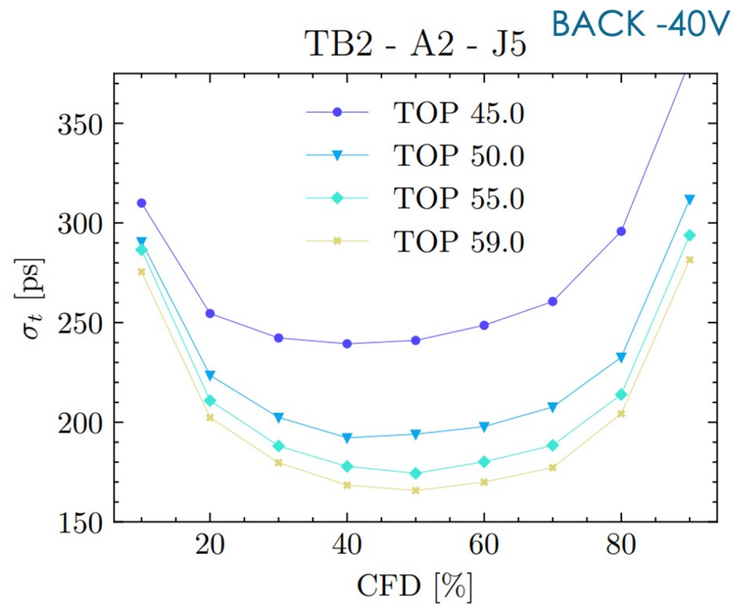
MAPS with gain: timing resolution

test beam @ CERN - July 2024

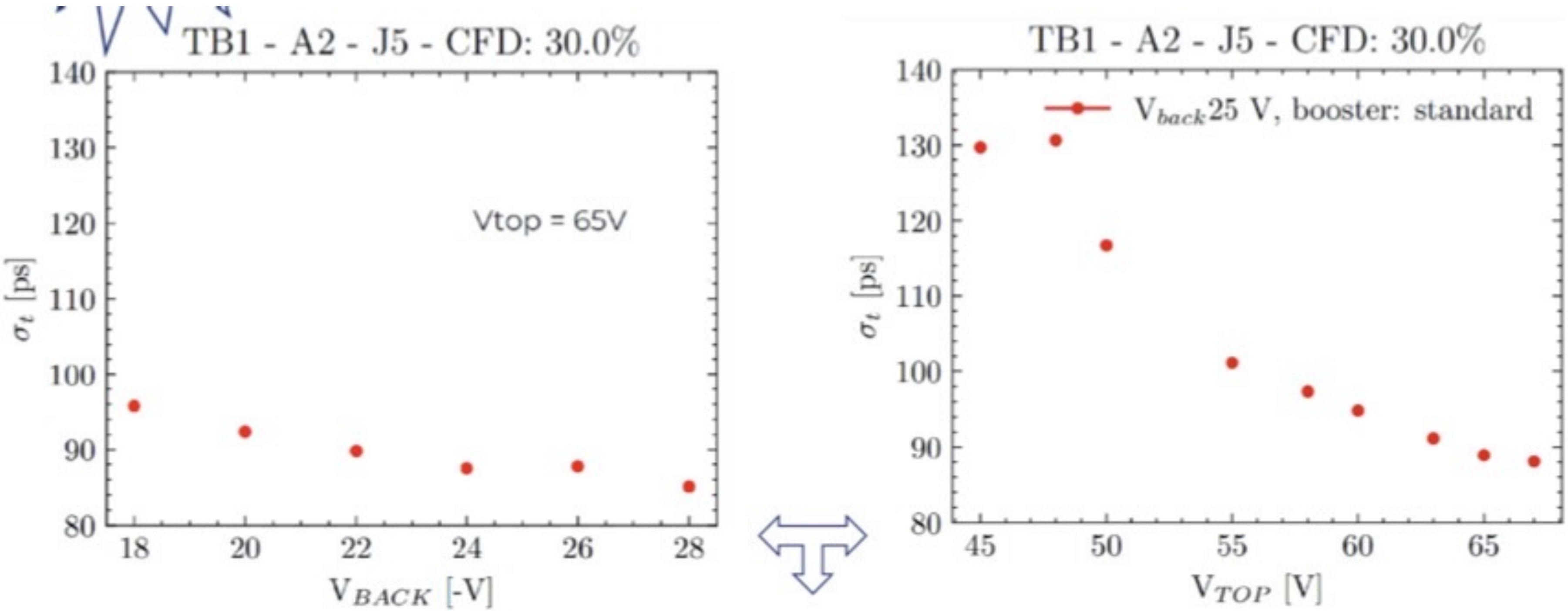
- Time resolution = standard deviation of the time difference between the reference time of the LGAD and CMOS trigger time
- Reference time: LGAD time @ 50% of the amplitude of the signal ($\sigma_t \approx 30$ ps)
- CMOS trigger time: crossing time of a fixed fraction of the CMOS amplitude
- Scan of the collection electrode voltage



Gaussian fit with asymmetric tails



Results: today



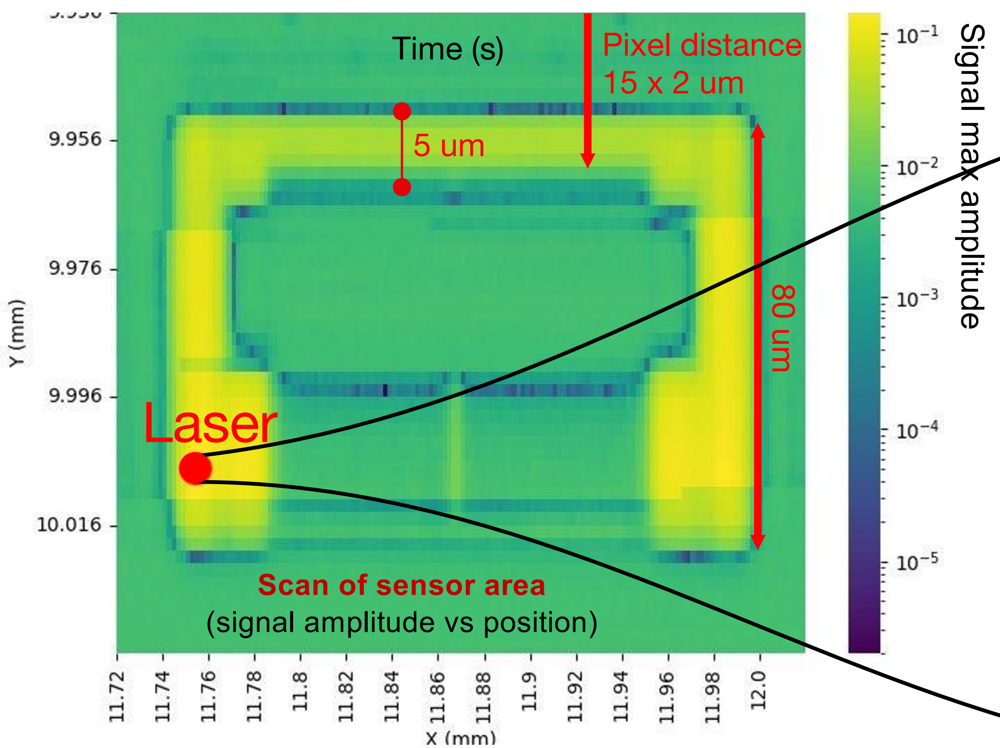
Time resolution sensor + front end (@0.18mW/ch): 88 ps

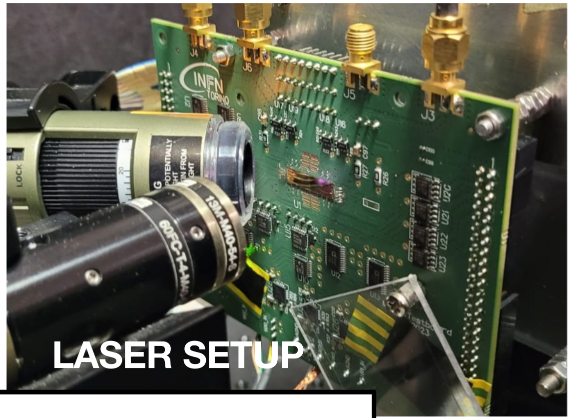
Time resolution sensor: ≈ 75 ps (with increased power)

17

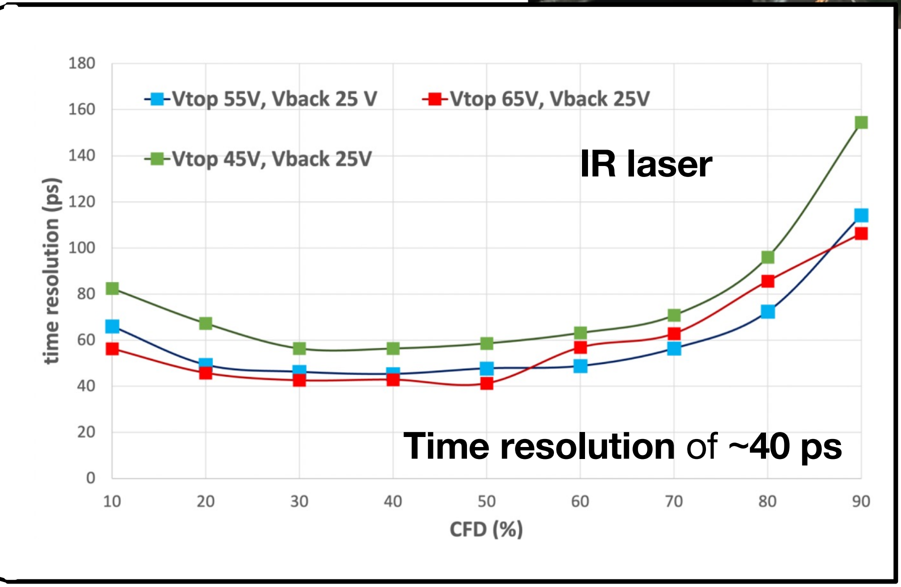
Characterisation with a laser setup

- Characterisation of active structures performed with IR laser **ongoing**:
  - allows for the estimation of the gain with a focused beam spot (~7 μm)
  - needed for measuring the jitter contribution to the total time resolution
  - Next: different FEE amplification params, thinner sensors with higher gain





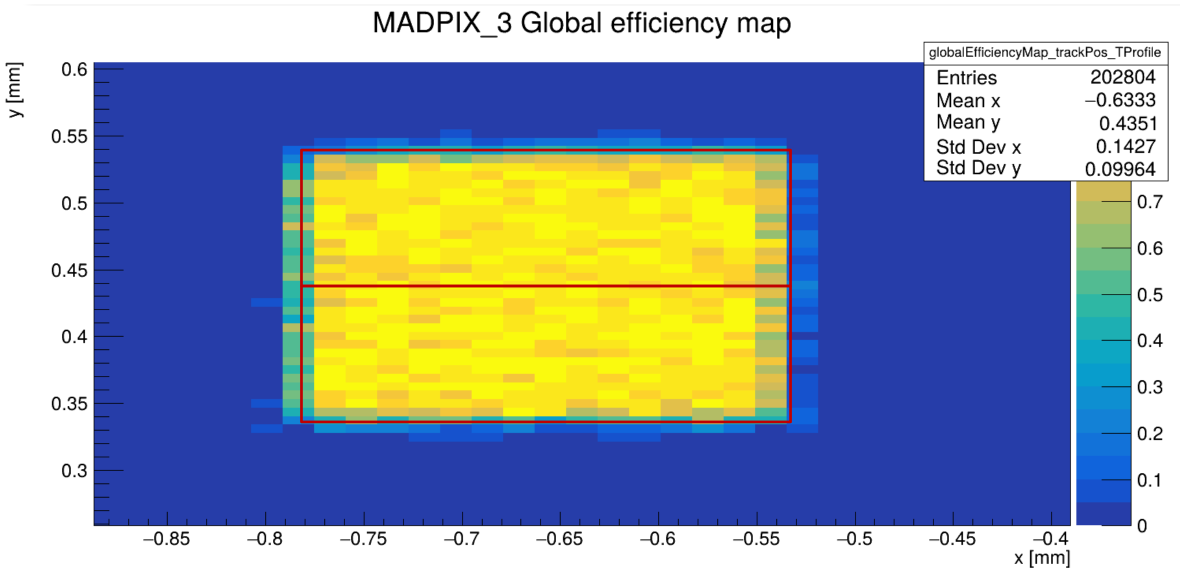
λ=1064nm

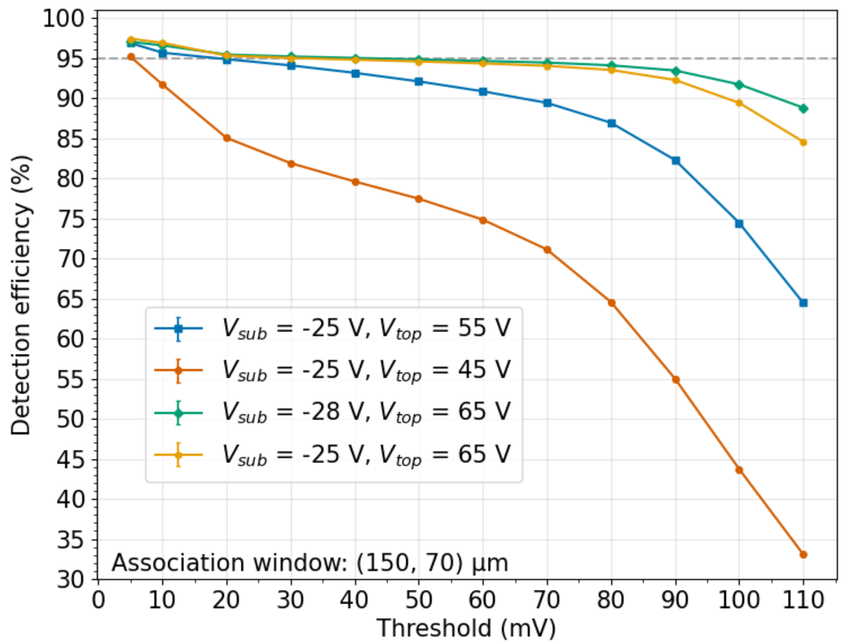


DESY beam tests

- 6 MIMOSA planes
- Active area: 2 cm x 1 cm
- 115.2 us per cycle, 2 cycle readout
- DAQ System: AIDA TLU
- Without DUT: 2kHz event rate
- Trigger w. DUT: 10-100 particles s^{-1} mm^{-2}
- Track resolution: 1.8 um

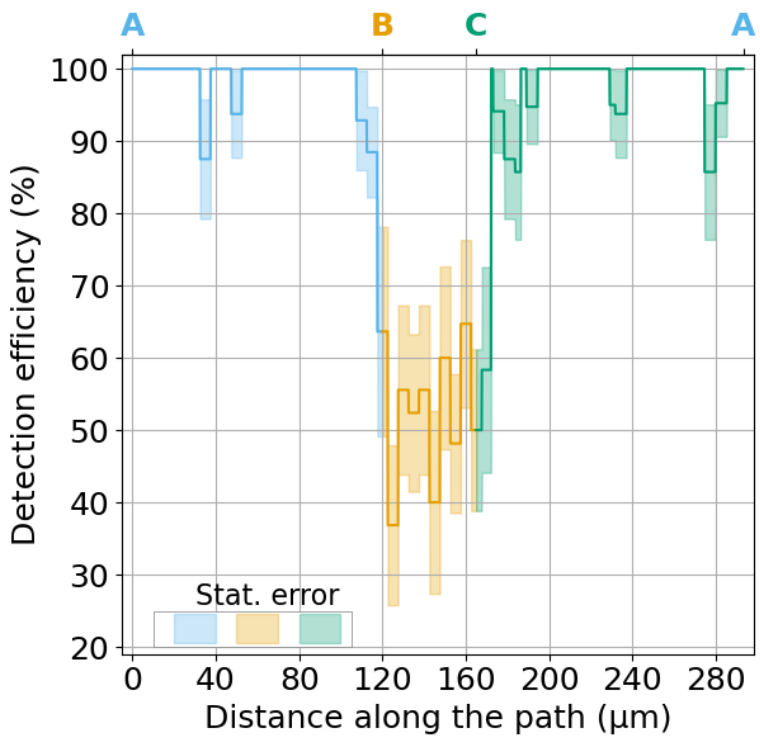
DESY beam tests: preliminary

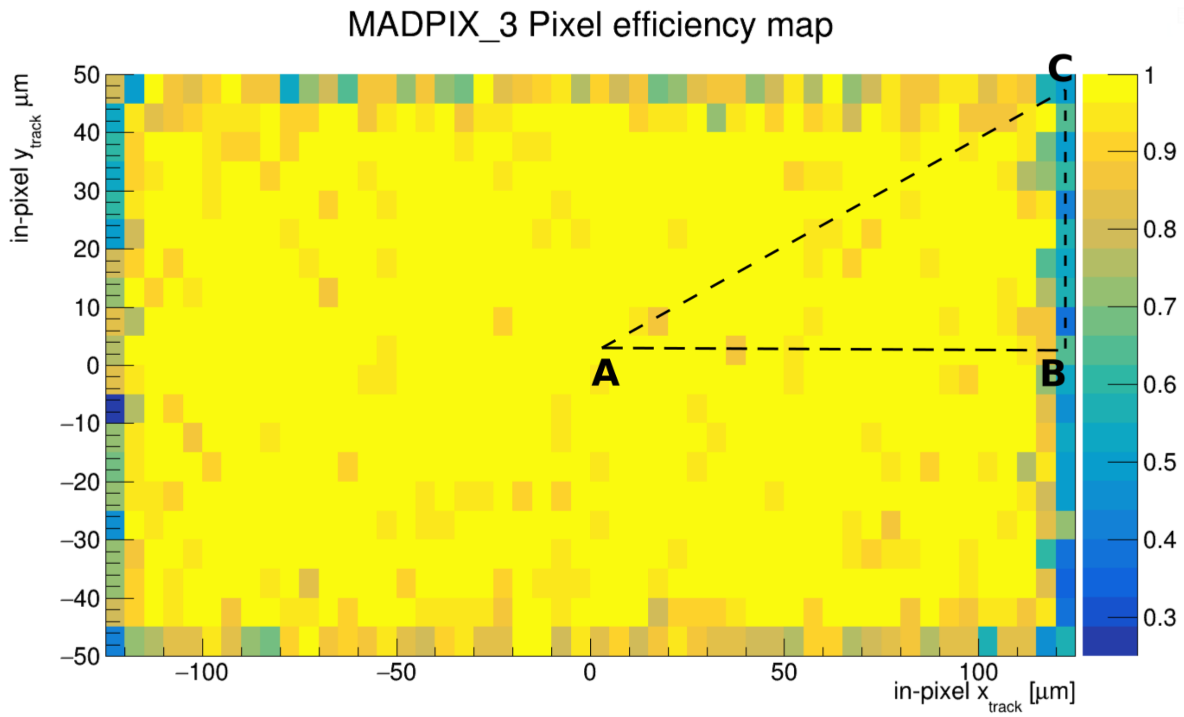




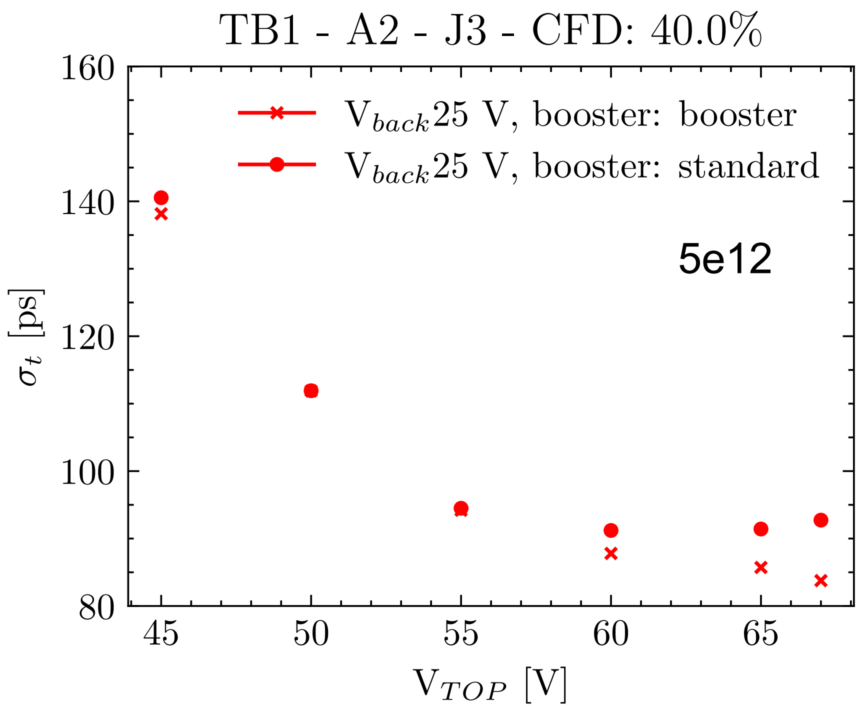
- First integration of MadPix with a tracker
- Efficiency studies and time resolution mapping
- Very stable system running
- Time resolution fully compatible with CERN test beam results

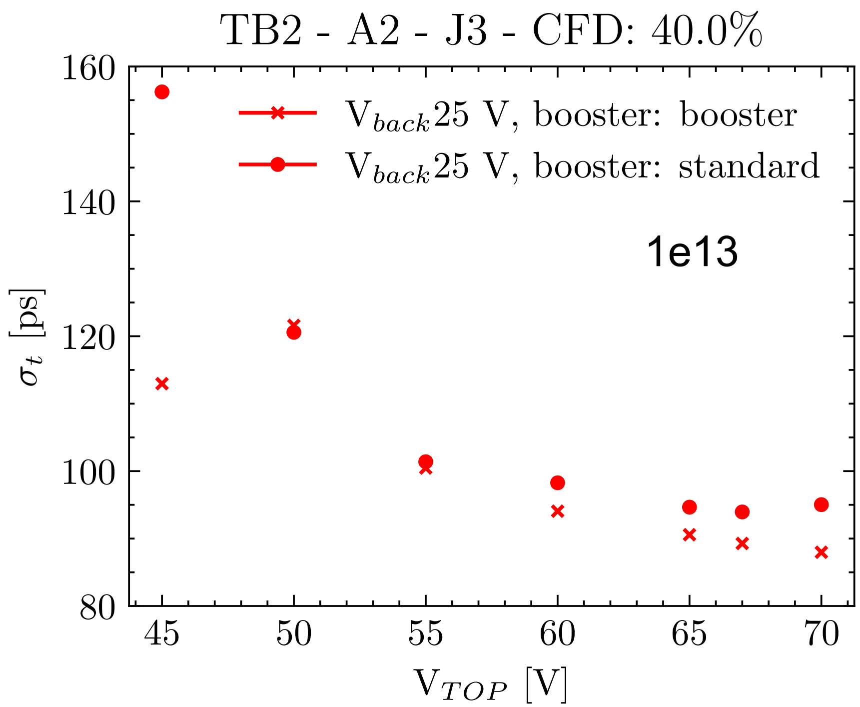
DESY beam tests: preliminary



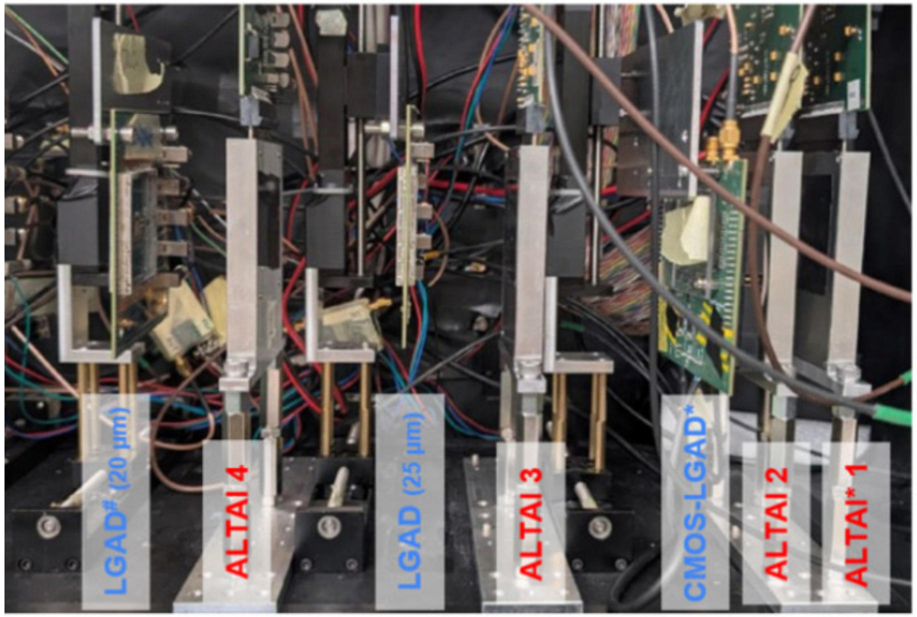


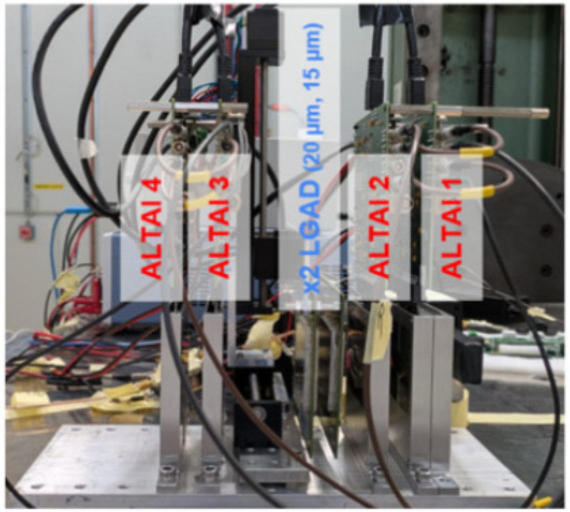
July CERN beam test with irradiated sensors (not even preliminary…)





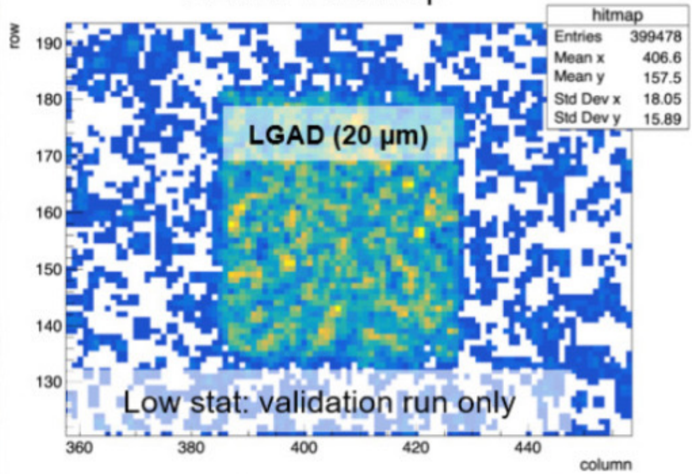
(CMOS-)LGADs w. ALTAI trackers



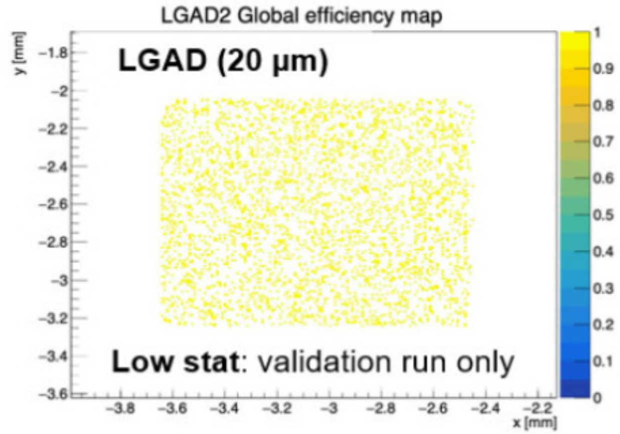


TRIGGER LGAD
* 48 µm (CMOS-LGAD)
* MAPS

ALTAI 4 hit map



Only 5 ktriggers here!
[>1 Mtriggers recorded]

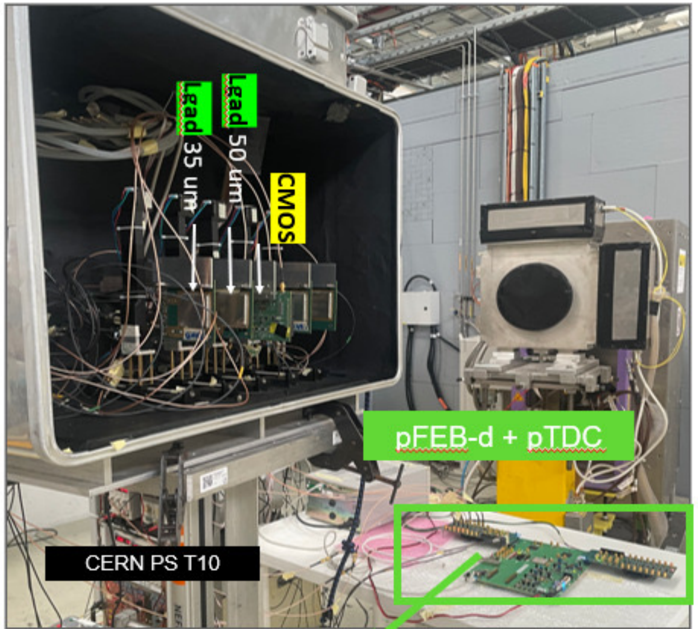


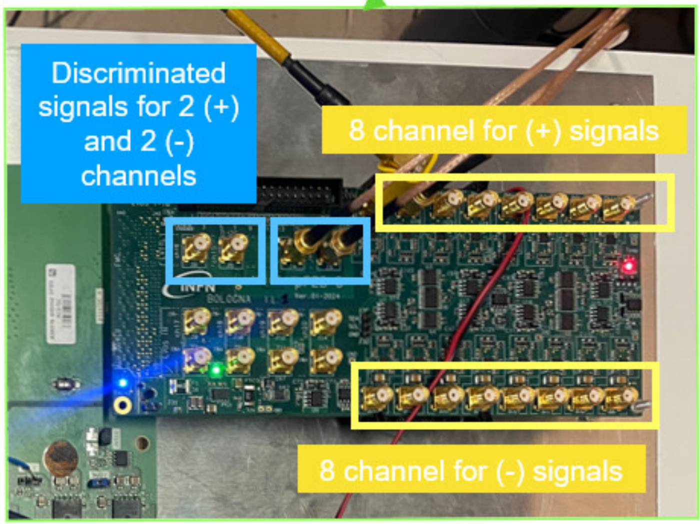
- Test beam at **CERN-PS** (ended yesterday) now equipped also with **ALTAI trackers** (on top of LGAD reference planes) for mapping the time resolution and efficiency of **CMOS-LGAD prototypes**
- Versatile setup, data acquired with π/p at 10 GeV/c (almost **top energy for minimizing the multiple scattering**)
- **Data being analysed looking into hybrid LGADs** (FBK prototypes) as a benchmark, being the **CMOS-LGAD the targeted DUT**
- Next: adding more tracker planes, next CMOS-LGAD prototypes; possibility to go to SPS (higher energy, more focused beam)

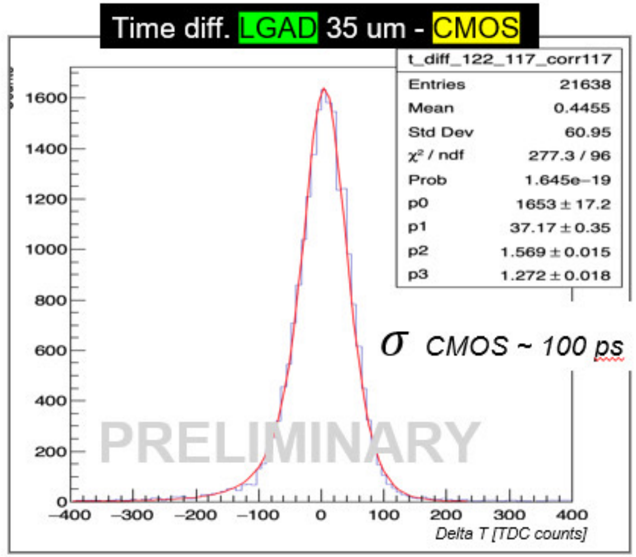
Beam test with digital acquisition of (CMOS)-LGAD sensors (25/06/25-09/07/25)

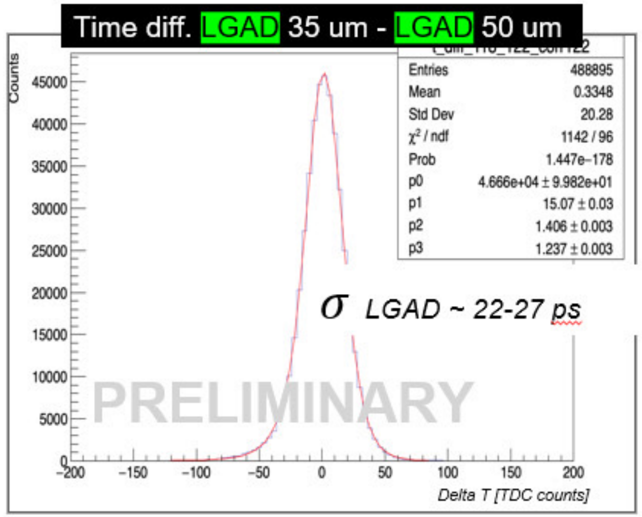
- DUTs: 2 **LGADs(35-50 um)** + 1 **CMOS-LGAD** prototypes
- **pFEB-d** board: **fast discriminator** (up to 16 positive and 16 negative signals)
- **picoTDC** (3.05 ps resolution)

Time resolutions acquired with the **oscilloscope** (analog DUT signals) **compatible** with the ones obtained **with the full readout chain** (DUT+disc.+TDC)!









The pFEB-d + pTDC readout was tested at different thresholds. The runs show promising results : time resolution near **~100 ps** for the **CMOS-LGAD** prototype and **~22-27 ps** for the **LGADs**.

To meet both the pFEB and the pTDC requirements on the input signal, amplifiers of ~45 dB were put on the LGADs in order to exploit the ToT correction at its best.

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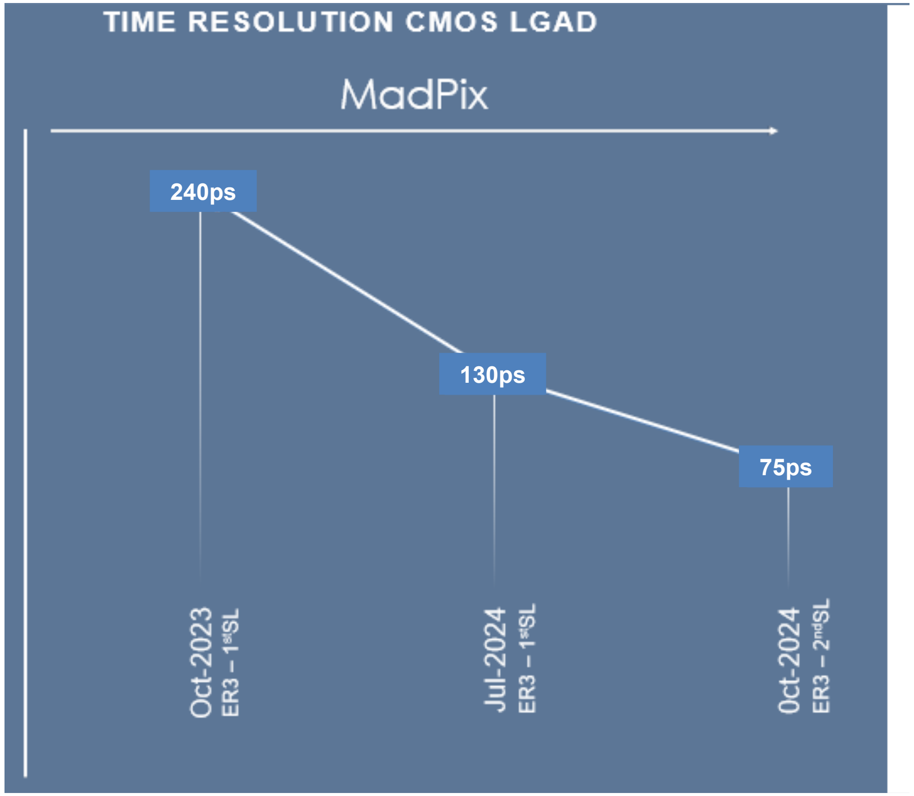
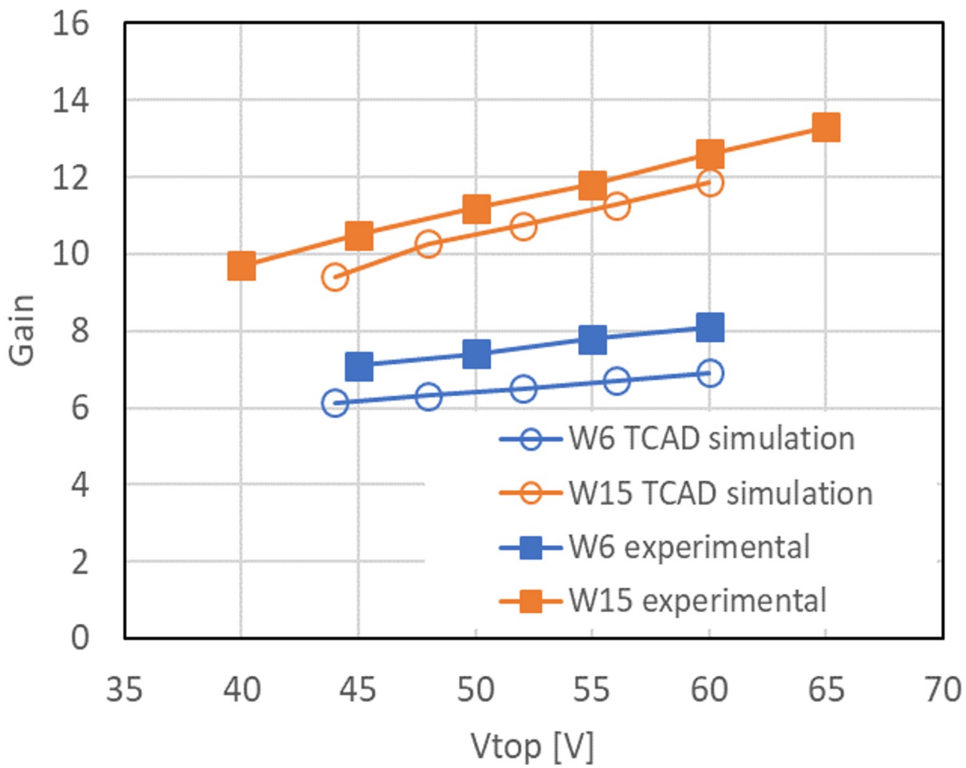
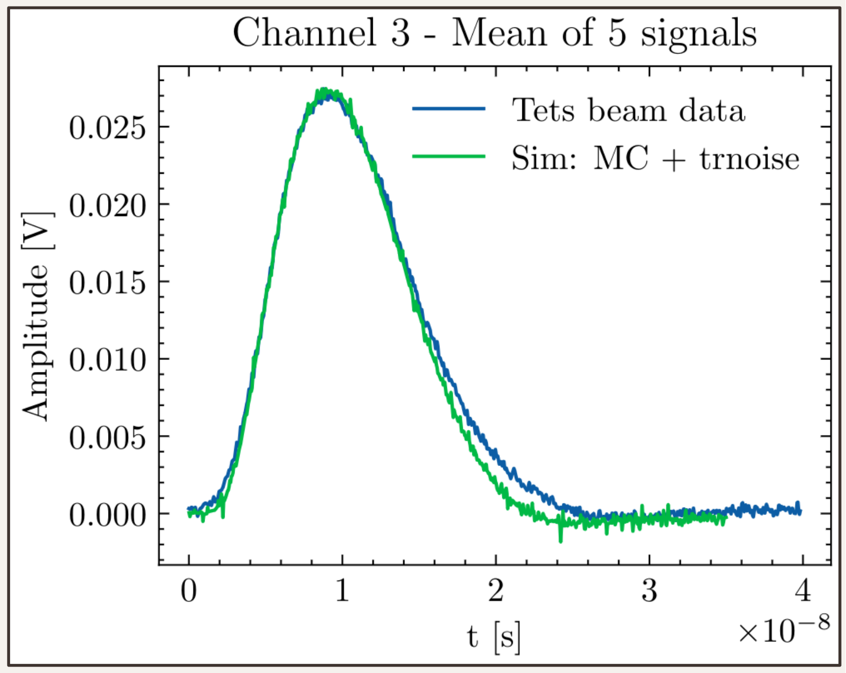
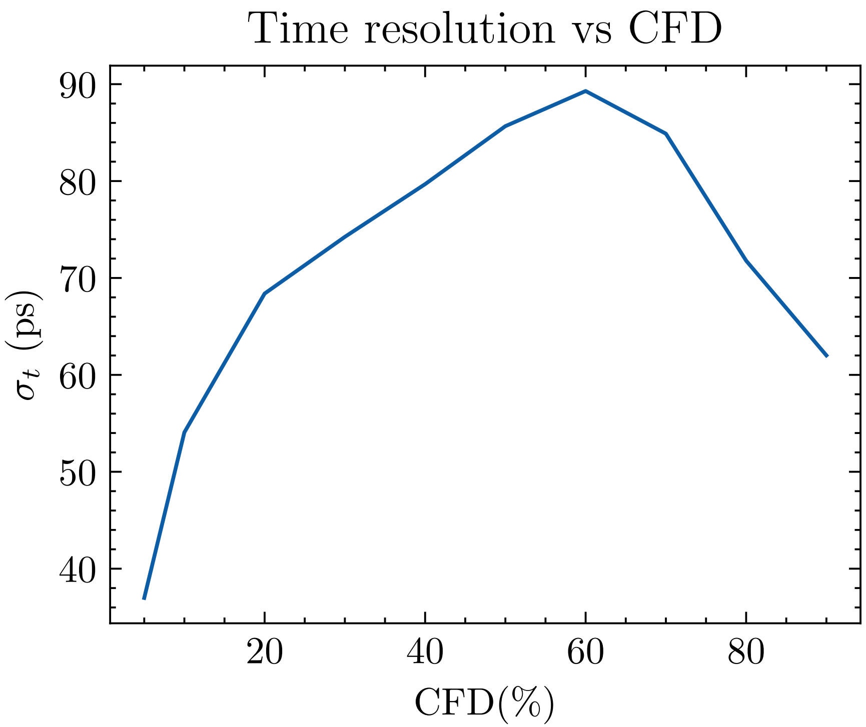
One year of improvements - 1





One year of improvements - 2

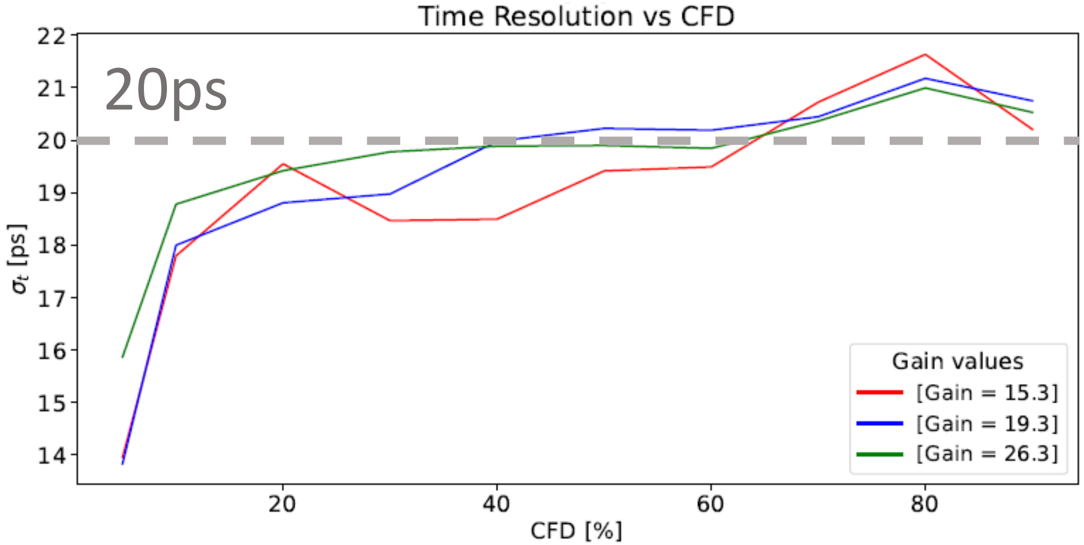




2025 Final short loop fabrication: wafer splittings and predicted performance

N. wafers	Starting material	P-gain implant dose
1	A (n 20um)	No gain
1	A (n 20um)	Gain dose 1
2	A (n 20um)	Gain dose 2
1	B (n 15um)	No gain
1	B (n 15um)	Gain dose 1
2	B (n 15um)	Gain dose 2
1	C (p 15um)	(no gain)
1	C (p 15um)	Gain dose 1
2	C (p 15um)	Gain dose 2

Total: 12 wafers



Monte Carlo simulations:

- Timing resolution close to 75ps for 48µm active thickness (also measured on devices currently available)
- Predicted timing resolution close to 20ps for 15µm active thickness

What next?

- Implementation of CMOS-LGAD has been very successful so far
- Initial hiccups not due to fundamental reasons and properly fixed
- The 2025 short loop is the last that makes sense with the ARCADIA masks
- Ultimate time resolution needed by ALICE3 can not be achieved due to pixel aspect ratio
- 2034 is (unfortunately…) tomorrow
- We need to move from a sensor-oriented R&D to a system-oriented design
- Impossible to make progress without a dedicated mask sets

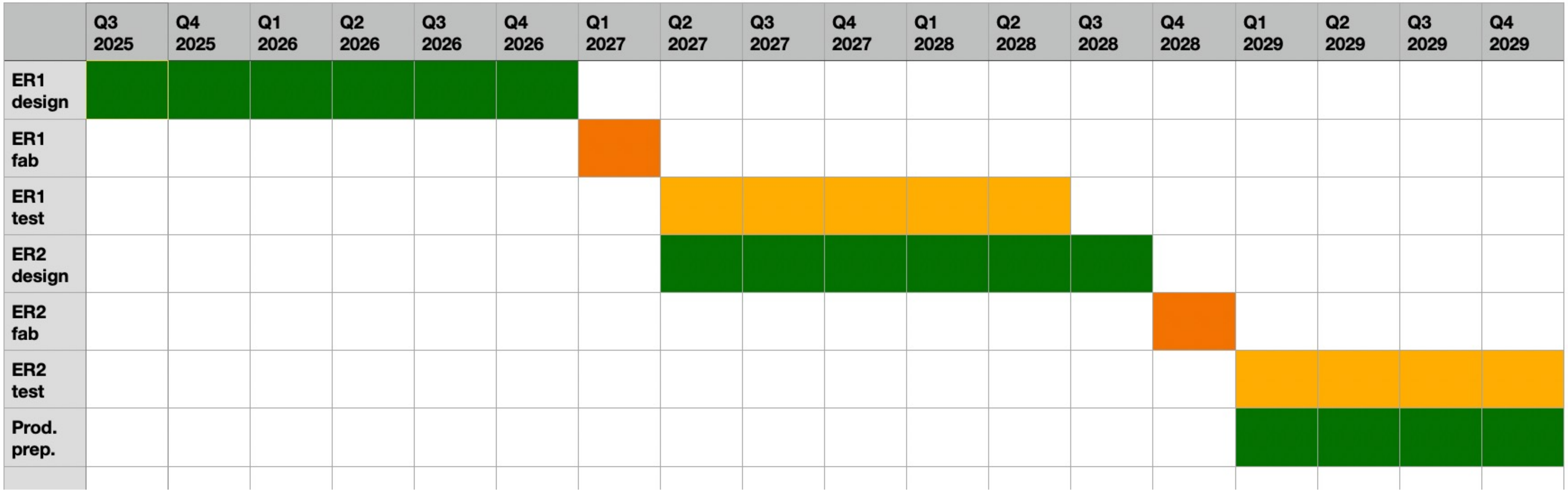
The timing budget

$$\sigma_t = \sqrt{\sigma_{sensor}^2 + \sigma_{preamp}^2 + \sigma_{TDC}^2 + \sigma_{clk}^2}$$

- TDC contribution: 3 ps (requires 10 ps binning)
- Clock jitter: 3 ps
- Preamplifier jitter: 10 ps rms
- Sensor budget: 17 ps rms
- Estimated power: 0.2 W/cm^2

- TDC and PLL do not require particular R&D, but very good engineering

An other timing budget



- Production, installation and commissioning take a big share
- We need to start working soon also on other engineering aspects (mechanics, etc..)
- Key commonality with tracking detectors

Milestones 2025

31/12/24 ALICE3 TOF - Caratterizzazione di sensori al silicio con Laser e fasci di particelle per lo studio della performance in termini di risoluzione temporale **100%**

30/06/25

Simulazioni TCAD, Garfield ++ e Allpix2 per ottimizzare, in termini di risoluzione temporale, il design dei sensori CMOS con guadagno sulla base dei risultati dei test in laboratorio e con fascio → completata e i risultati delle simulazioni sono serviti da input per il prossimo short loop run che è in fase di ordine **100%**

31/12/25

Caratterizzazione di sensori al silicio in laboratorio e con fasci di particelle per lo studio della performance in termini di risoluzione temporale → test beam al PS del CERN schedulati a fine giugno e fine ottobre. Sono stati già stati condotti dei test beam a DESY **50%**

Milestones e richieste 2026

1. (30/06/2026)
- Simulazioni TCAD e Monte Carlo per ottimizzare, in termini di risoluzione temporale, il design dei sensori in vista del primo Engineering run dedicato a CMOS-LGAD

2. (30/06/2026)
- Caratterizzazione di sensori del quarto short loop

3. (31/10/2026)
- Completamento del disegno dei dimostratori per ER1

Missioni per test beam

Sede	Importo k€
Bologna	23,5
Torino	23,5
Trento	9,5

Inventariabile, Licenze + Eng. Run

Sede	Importo k€
Bologna	42,5
Torino	42
Trento	5
ER	360

Sede	Importo	Descrizione
Bologna	6	**Inventariabile:** Strumentazioni per test su fascio: movimentatore a 2 assi, 2 LVPS
Bologna	4	**Inventariabile:** FPGA programmazione CMOS-LGAD
Bologna	18.5	**Inventariabile**: Strumentazione banco ottico: power meter, IR camera, focalizzatore, filtri, IR laser
Bologna	10	**Consumo:** Test board prototipi CMOS-LGAD
Bologna	4	**Licenze:** Tre postazioni per utilizzo del software applicativo CATIA per progettazione meccanica.
Trento	5	**Inventariabile:** obiettivo con elevata apertura numerica per setup TPA esistente
Torino	28	**Inventariabile**: setup per rendere pienamente funzionante TCT (finanziata nel 2024). Nel 2025 erano stati assegnati solo 8 kEuro dei 24 kEur richiesti. Reiteriamo parte della richiesta altrimenti la TCT non è utilizzabile.
Torino	12	**Inventariabile**: Custom board per testare i CMOS-LGAD del nuovo ER
Torino ++	360	**TOF- Engineering run**
Torino	2	**Licenza** TCAD e Xilinx Vivado (per ZDC, Ma mettiamo insieme)

ER organization

- Critical issue: signal and power propagation in the vertical direction
- To reduce time and risk: re-use IP already developed in the target or similar technologies and already very familiar to the designers
- ER1 chip final size in y and fully consistent. “Copy and repeat” to make ER2