# TEST SYSTEM FOR MLR1 and ER2 CHIPLETS

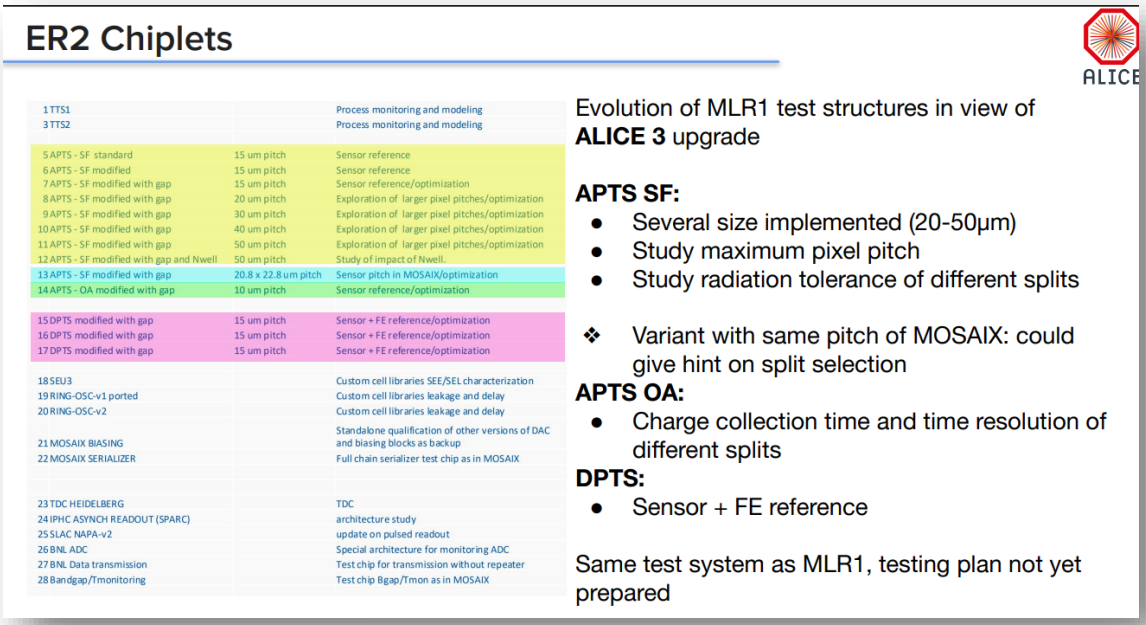
**MLR1**: First submission of MAPS in 65 nm. Used to validate the 65 nm technology (2021-2023). Three types of Test Structures (TS) characterized: APTS (Analog Pixel Test Structures), DPTS (Digital Pixel Test Structures), CE65 (Circuit Exploratoire 65 nm).

APTS: 4×4 matrix, 10-25 µm pixel, w/o process modification, analog readout

DPTS: 32×32 matrix, 15 µm pixel, modified with gaps, digital readout, time-encoded signal amplitude and position

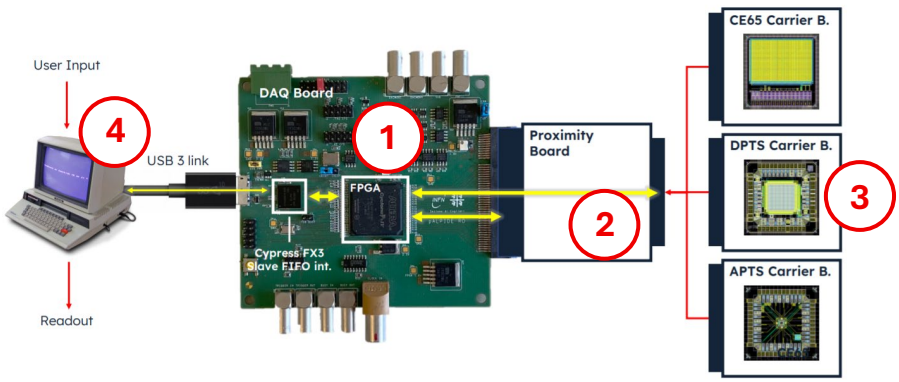
CE65: Rolling shutter readout, 3 submatrices, both amplifier and source-follower output buffers.

**ER2**: Production of MOSAIX, babyMOSAIX and chiplets. List of chiplets:




**SETUP**: Same test system for MLR1 and ER2 chiplets.

DAQ (1) + Proximity (depending on the specific test structure under test) (2) + carrier with the test structure bonded (3) + computer + power supply (4)




**COST ESTIMATION**:

- DAQ: provided by CERN

- Proximity: ~ 1000 CHF
- Computer: for example HP Elite Mini 800 G9 Desktop PC 5M981EA#ABZ (i7) ~ 1200 euro
- Power supply: R&S®NGC100 Power supply series ~ 1200 EUR

**REFERENCE PUBLICATIONS**:

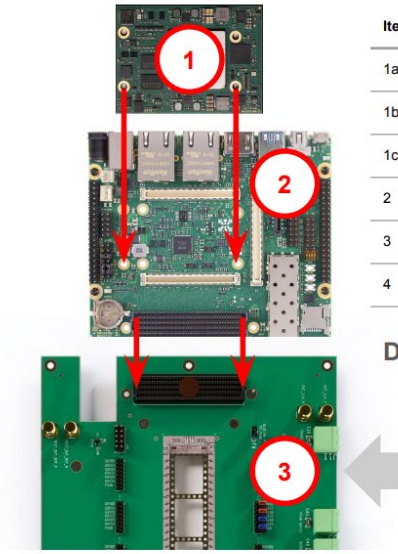
- DPTS: https://doi.org/10.1016/j.nima.2023.168589
- APTS-SF: https://doi.org/10.1016/j.nima.2024.169896
- APTS-OA: https://doi.org/10.1016/j.nima.2024.170034

**RECENT SUMMARY OF ITS3 CHARACTERISATION ACTIVITIES @ INFN**:

https://agenda.infn.it/event/46163/

# TEST SYSTEM FOR BABY-MOSAIX (ER2)

## Mosaix Test System




| Item | | Unit price (CERN via EDH) | Reference |
|---|---|---|---|
| 1a | FPGA module | 666,60 CHF | Enclustra ME-AA1-270-3E4-D11E-NFX3 |
| 1b | FPGA module rework | 200,00 CHF | Enclustra-provided BoM & placement |
| 1c | Heat sink | 29,70 CHF | Enclustra ACC-HS4-SET |
| 2 | Base board | 289,30 CHF | Enclustra ME-ST1-W |
| 3 | (baby)MOSAIX carrier | - | Design: A. Junique / J. Morant |
| 4 | Power supply (2x) | 1241,00 EUR | Rhode & Schwarz NGC103 |

**Distribution and support coordinator: G. Usai @ CERN**


With respect to small TS test system, you need a FPGA module + rework (1), an Enclustra board (2), the carrier (3) and an additional power supply (4) → ~ +2500 euro