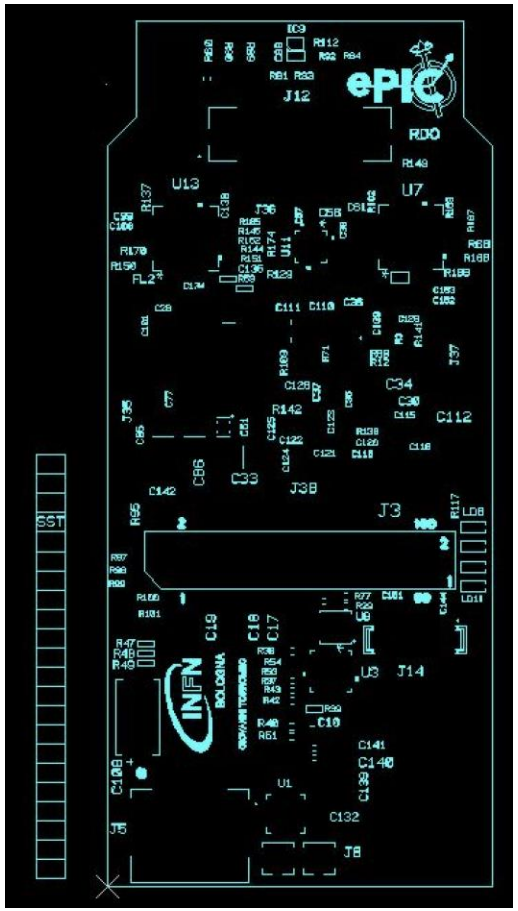
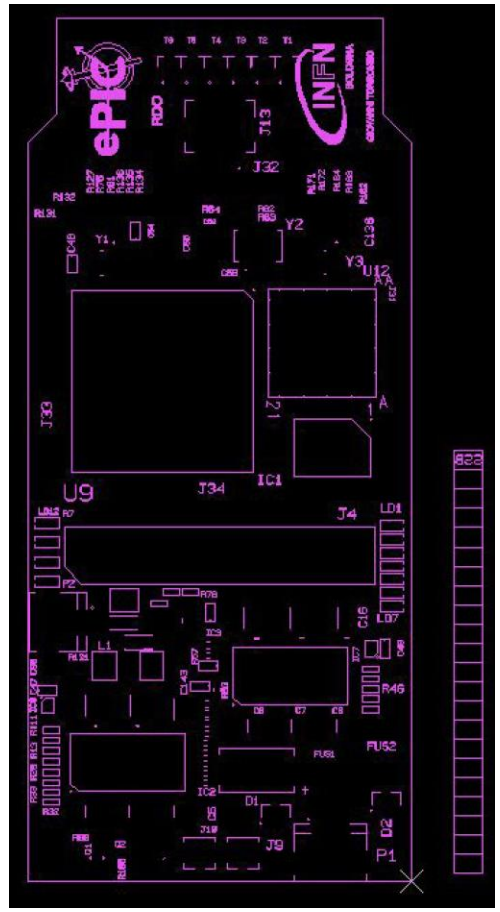


Consumi RDO

P. Antonioli , D. Falchieri, S. Geminiani,
L. Rignanese, G. Torromeo (INFN Bologna)

dRICH Power Day
Ferrara 10 June 2025



Other news about RDO

- arrivo PCB a ARTEL: 20 giugno 2025
- prime due schede dovrebbero arrivarci 30/6
- stima produzione: 489 k€ (1500 + montaggio) + 256 k€ (ARTIX) + 187 k€ (PF) = 932 k€ + IVA = **1.1 M€**
- progressi su fw
- lista di test per prima validazione (per go per altre 8) durante luglio discussa a meeting martedi' due settimane fa

RDO next steps for go for production (8 RDOs)

1. Mechanical pairing with fake-FEB
2. Power-up : 2.5 / 1.4 jumper to avoid power to other sections
3. Prg uC via external connector
4. Power-up with uC (post-programming uC): check Vout LDO
5. Prg Artix via external connector
6. Prg Polarfire via external connector
7. Prg Artix → SkyWorks (programming 125 MHz of Si5319)
8. Check consumptions
9. Check UFL I/Os
10. Link IPBUS via VTRX+ [MT-MPO adapter + "polipo"]
11. Prg ALCOR via fake-FEB (via IPBUS → VTRX+)
12. ALCOR readout (via IPBUS → VTRX+)

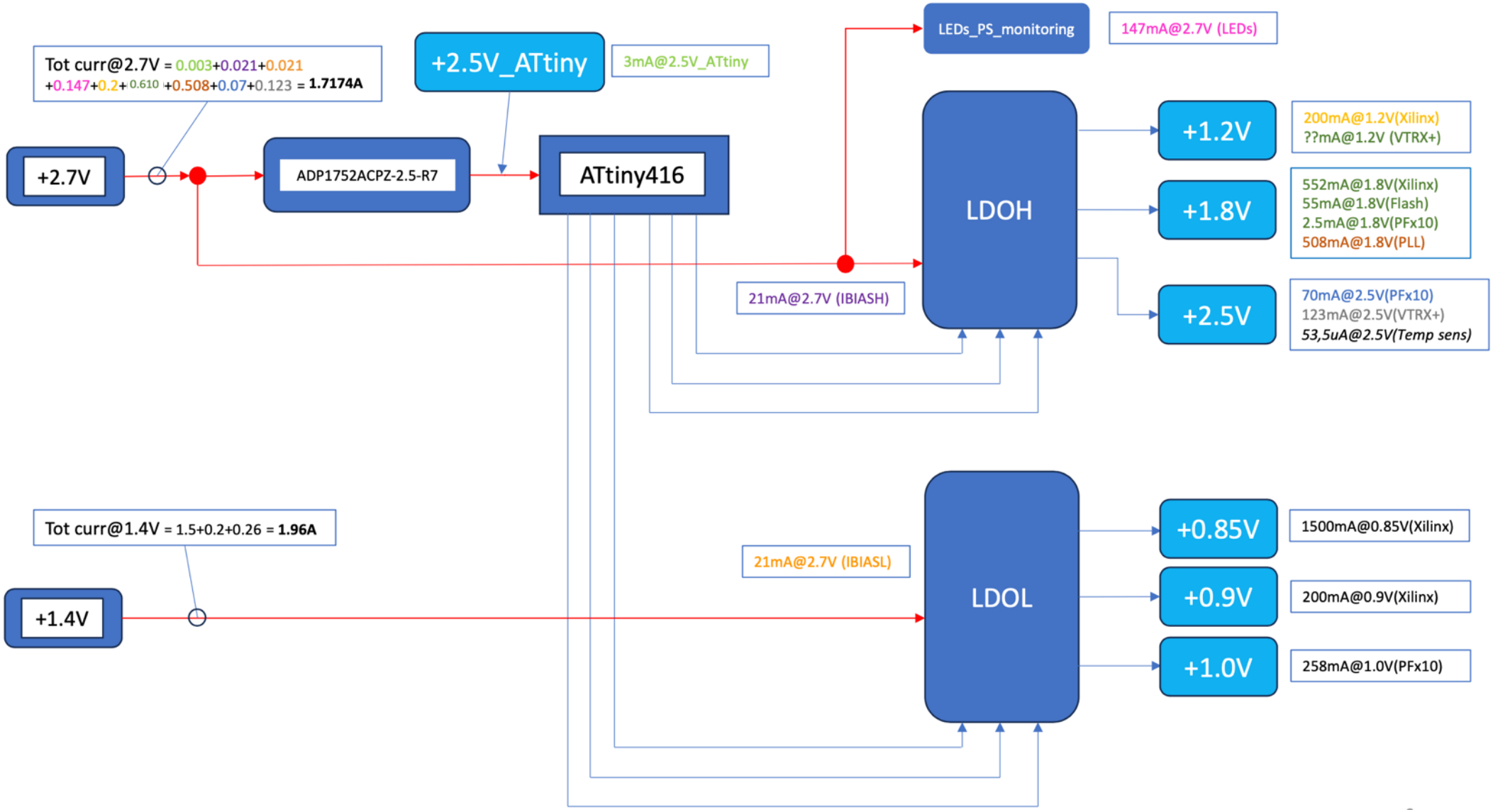
Note: we can't test everything before give the "go" for next 8 RDOs...
Note: we should get 2 first RDO by 10 June...

30 June

Stime consumi: assunzioni / fonti

- FPGA Polarfire: stima con FW "minimal" moltiplicata di un fattore 10
- FPGA Artix: basato su ultima versione FW (inclusa lettura ALCOR + link ottico) + “abbondanza”
- VTRx+ da TWEPP PoS 2019 (L. Olantera et al.) → scritto al CERN
- e in generale datasheet vari componenti (es. SI5319 + Si5326 = 500 mA!)
- progettazione Giovanni!

Correnti RDO (I)



Consumi RDO (II)

LV Channel	Device	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
LVH 2.7 V	AUX15P	LTM4709-1H	2.7	1.20	0.2000	1.50	0.540	0.240	0.300
		LTM4709-2H	2.7	1.80	0.5520	0.90	1.490	0.994	0.497
		LTM4709-3H	2.7	2.50	0.0150	0.20	0.041	0.038	0.003
	MPF050T	LTM4709-2H	2.7	1.80	0.0025	0.90	0.007	0.005	0.002
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	VTRX+	LTM4709-1H	2.7	1.20	0.0000	1.50	0.000	0.000	0.000
		LTM4709-3H	2.7	2.50	0.1224	0.20	0.330	0.306	0.024
	MT25QU01	LTM4709-2H	2.7	1.80	0.0550	0.90	0.149	0.099	0.050
	Si5326	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	Si5319	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	TMP119	LTM4709-3H	2.7	2.50	0.0005				
	ATtiny417	ADP1752	2.7	2.50	0.0030	0.20	0.008	0.008	0.001
	LED		2.7	2.70	0.1470	0.00	0.397	0.397	0.000
	IBIAS-LDOH		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	IBIAS-LDOL		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	Total LV 2.7				**1.7174**		**4.64**	3.29	1.35
LVL 1.4 V	AUX15P	LTM4709-1L	1.4	0.85	1.5000	0.55	2.100	1.275	0.825
	AUX15P	LTM4709-2L	1.4	0.90	0.2000	0.50	0.280	0.180	0.100
	MPF050T	LTM4709-3L	1.4	1.00	0.2580	0.40	0.361	0.258	0.103
	Total LV 1.4				**1.9580**		**2.741**	1.713	1.028

- LED
- 4 TX+1 RX
- PF x 10

Consumi RDO (III)

LV Channel	Device	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
LVH 2.7 V	AUX15P	LTM4709-1H	2.7	1.20	0.2000	1.50	0.540	0.240	0.300
		LTM4709-2H	2.7	1.80	0.5520	0.90	1.490	0.994	0.497
		LTM4709-3H	2.7	2.50	0.0150	0.20	0.041	0.038	0.003
	MPF050T	LTM4709-2H	2.7	1.80	0.0025	0.90	0.007	0.005	0.002
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	VTRX+	LTM4709-1H	2.7	1.20	0.0000	1.50	0.000	0.000	0.000
		LTM4709-3H	2.7	2.50	0.0624	0.20	0.168	0.156	0.012
	MT25QU01	LTM4709-2H	2.7	1.80	0.0550	0.90	0.149	0.099	0.050
	Si5326	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	Si5319	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	TMP119	LTM4709-3H	2.7	2.50	0.0005				
	ATtiny417	ADP1752	2.7	2.50	0.0030	0.20	0.008	0.008	0.001
	LED		2.7	2.70	0.0000	0.00	0.000	0.000	0.000
	IBIAS-LDOH		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	IBIAS-LDOL		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	Total LV 2.7				**1.5104**		**4.08**	2.74	1.34
LVL 1.4 V	AUX15P	LTM4709-1L	1.4	0.85	1.5000	0.55	2.100	1.275	0.825
	AUX15P	LTM4709-2L	1.4	0.90	0.2000	0.50	0.280	0.180	0.100
	MPF050T	LTM4709-3L	1.4	1.00	0.2580	0.40	0.361	0.258	0.103
	Total LV 1.4				**1.9580**		**2.741**	1.713	1.028

- no LED
- 1 TX +1 RX
- PF x 10

Consumi RDO (II)

Canale primario	Corrente totale (A)	Consumo (W)	Commenti
2.7 V	1.51	4.08	no LED 1 TX
1.4 V	1.96	2.74	
Grand Total	3.46	**6.7**	in det. box. O(1.3 kW) per 208 RDO

Device	Total Power (W)
AUX15P	2.726
MPF050T	0.438
LDOH	1.335
LDOL	1.028
SI5326	0.457
SI5319	0.457
VTRX+	0.156

- margins on AUX15P → see next slide
- x 10 on PF

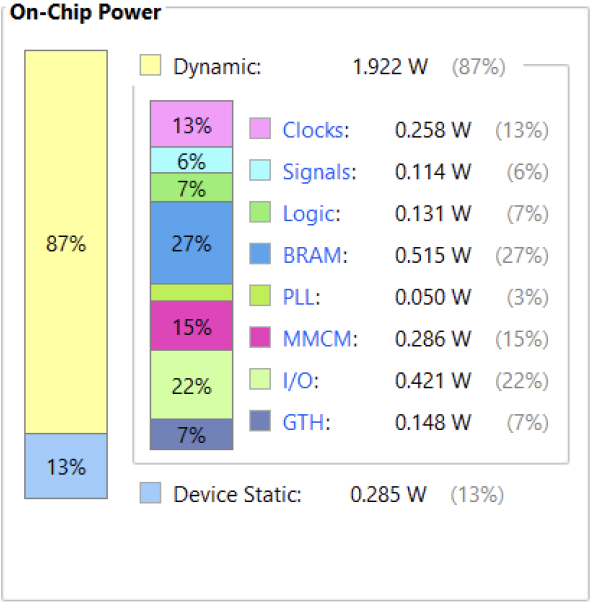
Last fw update and power consumption: AUX15P (I)

LV Channel	Device	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
LVH 2.7 V	AUX15P	LTM4709-1H	2.7	1.20	0.1070	1.50	0.289	0.128	0.161
		LTM4709-2H	2.7	1.80	0.4820	0.90	1.301	0.868	0.434
		LTM4709-3H	2.7	2.50	0.0060	0.20	0.016	0.015	0.001
	MPF050T	LTM4709-2H	2.7	1.80	0.0025	0.90	0.007	0.005	0.002
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	VTRX+	LTM4709-1H	2.7	1.20	0.0000	1.50	0.000	0.000	0.000
		LTM4709-3H	2.7	2.50	0.0624	0.20	0.168	0.156	0.012
	MT25QU01	LTM4709-2H	2.7	1.80	0.0550	0.90	0.149	0.099	0.050
	Si5326	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	Si5319	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	TMP119	LTM4709-3H	2.7	2.50	0.0005				
	ATtiny417	ADP1752	2.7	2.50	0.0030	0.20	0.008	0.008	0.001
	LED		2.7	2.70	0.0000	0.00	0.000	0.000	0.000
	IBIAS-LDOH		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	IBIAS-LDOL		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	Total LV 2.7				**1.3384**		**3.61**	2.48	1.13
LVL 1.4 V	AUX15P	LTM4709-1L	1.4	0.85	1.3650	0.55	1.911	1.160	0.751
	AUX15P	LTM4709-2L	1.4	0.90	0.0430	0.50	0.060	0.039	0.022
	MPF050T	LTM4709-3L	1.4	1.00	0.2580	0.40	0.361	0.258	0.103
	Total LV 1.4				**1.6660**		**2.332**	1.457	0.875

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.207 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**31,0°C**
Thermal Margin:	69,0°C (24,7 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	2,7°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



With last version of AUX15P FW (certainly still incomplete: not yet interface with PF etc., no EIC link but IPBUS, clock at 320 MHz) we have 2.2 W on AUX15P instead of 2.7 W and we are below 6 W. BRAM is used at 97% (FIFO on ALCOR lanes)

Current estimation “ad abudantiam” (2.7 W) about AUX15P is not so big (5.9 W vs 6.7 W impact on RDO)

But: how much conservative designing the power system?

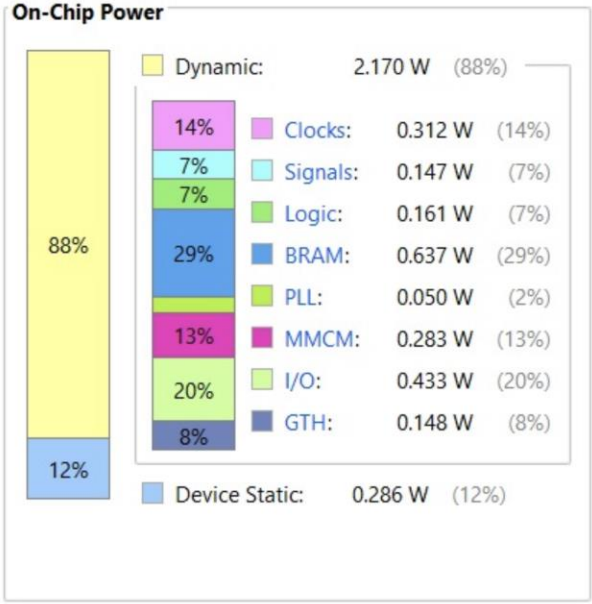
Last fw update and power consumption: AUX15P (II)

LV Channel	Device	LDO	Vin (V)	Vout (V)	Iout (A)	Vdrop (V)	Ptotal (W)	Pdevice (W)	Ploss (W)
LVH 2.7 V	AUX15P	LTM4709-1H	2.7	1.20	0.1070	1.50	0.289	0.128	0.161
		LTM4709-2H	2.7	1.80	0.4820	0.90	1.301	0.868	0.434
		LTM4709-3H	2.7	2.50	0.0060	0.20	0.016	0.015	0.001
	MPF050T	LTM4709-2H	2.7	1.80	0.0025	0.90	0.007	0.005	0.002
		LTM4709-3H	2.7	2.50	0.0700	0.20	0.189	0.175	0.014
	VTRX+	LTM4709-1H	2.7	1.20	0.0000	1.50	0.000	0.000	0.000
		LTM4709-3H	2.7	2.50	0.0624	0.20	0.168	0.156	0.012
	MT25QU01	LTM4709-2H	2.7	1.80	0.0550	0.90	0.149	0.099	0.050
	Si5326	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	Si5319	LTM4709-2H	2.7	1.80	0.2540	0.90	0.686	0.457	0.229
	TMP119	LTM4709-3H	2.7	2.50	0.0005				
	ATtiny417	ADP1752	2.7	2.50	0.0030	0.20	0.008	0.008	0.001
	LED		2.7	2.70	0.0000	0.00	0.000	0.000	0.000
	IBIAS-LDOH		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	IBIAS-LDOL		2.7	2.70	0.0210	0.00	0.057	0.057	0.000
	Total LV 2.7				**1.3384**		**3.61**	2.48	1.13
LVL 1.4 V	AUX15P	LTM4709-1L	1.4	0.85	1.6530	0.55	2.314	1.405	0.909
	AUX15P	LTM4709-2L	1.4	0.90	0.0430	0.50	0.060	0.039	0.022
	MPF050T	LTM4709-3L	1.4	1.00	0.2580	0.40	0.361	0.258	0.103
	Total LV 1.4				**1.9540**		**2.736**	1.702	1.034

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.456 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**31,7°C**
Thermal Margin:	68,3°C (24,5 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	2,7°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

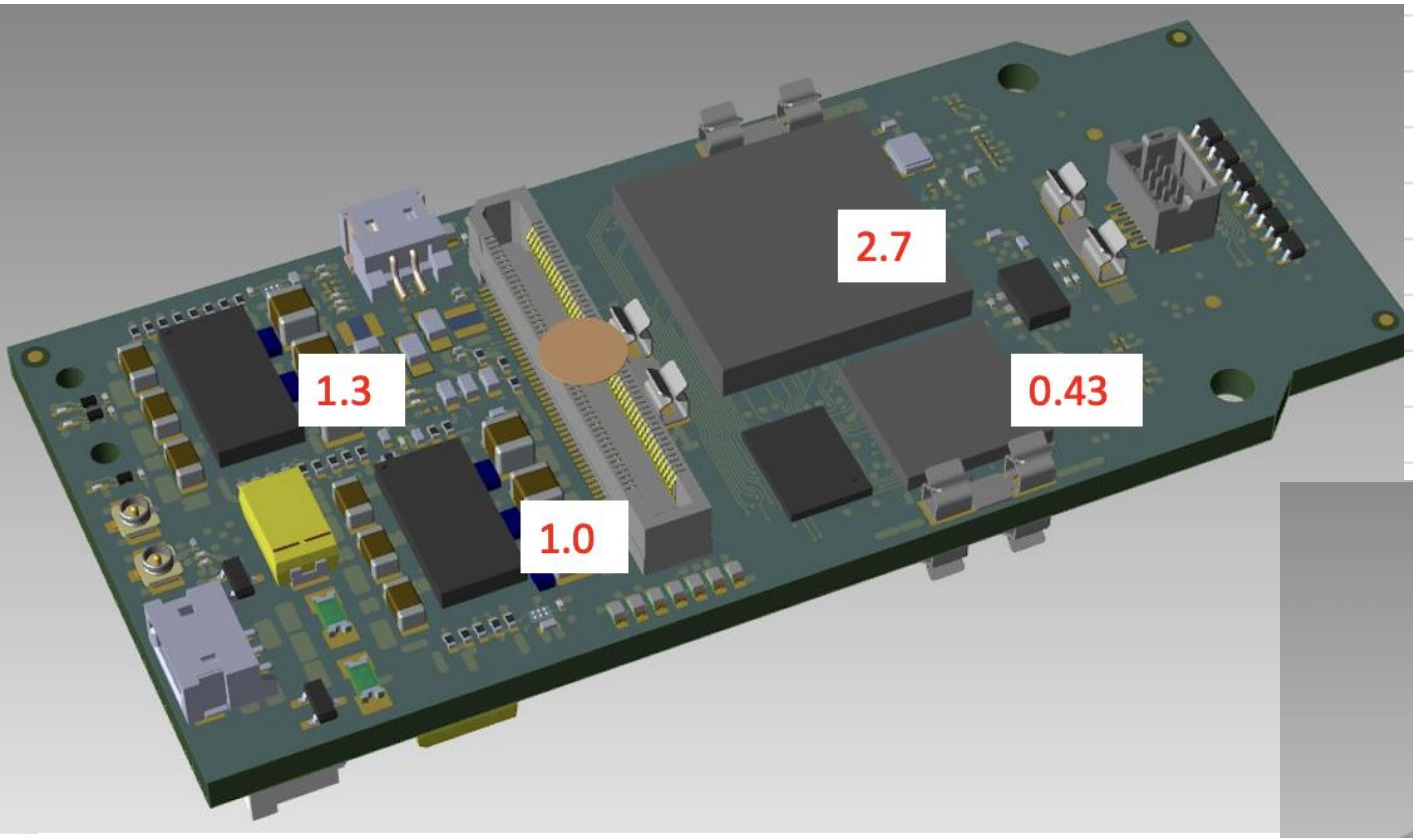
Launch Power Constraint Advisor to find and fix invalid switching activity



As previous slide but with clock at 400 MHz to read ALCOR: impact is a 21% increase of 0.85V core current (consistent with a 400/320= 25% clock increase) → 1.945 A on 1.4 V

So margins further reduced

Hot points



Device	Total Power (W)	Area (mm2)	W/mm2
AUX15P	2.726	361	7.55
MPF050T	0.438	121	3.62
LDOH	1.335	72	18.54
LDOL	1.028	72	14.28
SI5326	0.457	36	12.70
SI5319	0.457	36	12.70
VTRX+	0.156	100	1.56