BULLKID-DM Readout Electronics Updates

Collaboration Meeting Ferrara, 02.07.2025

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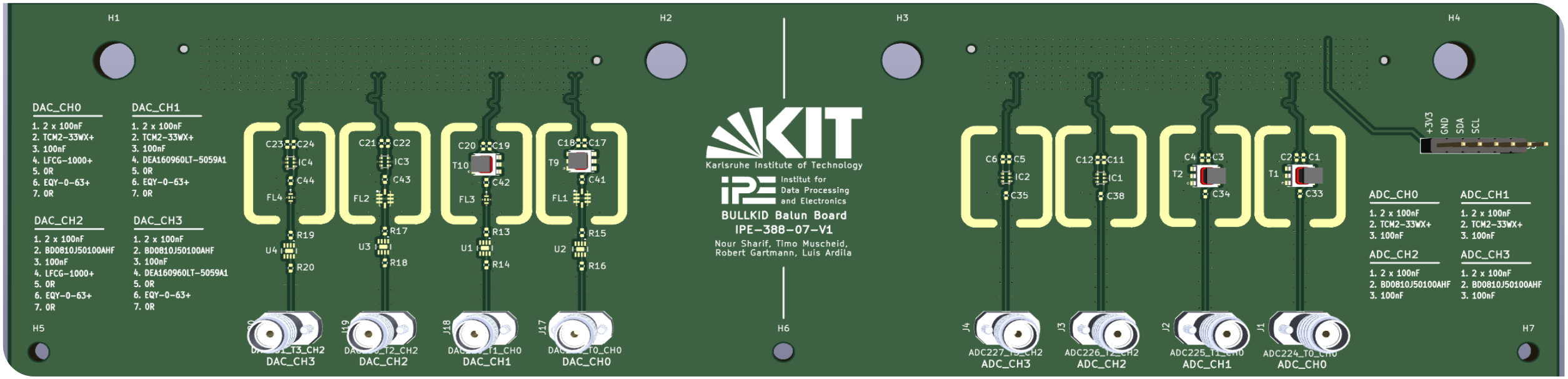
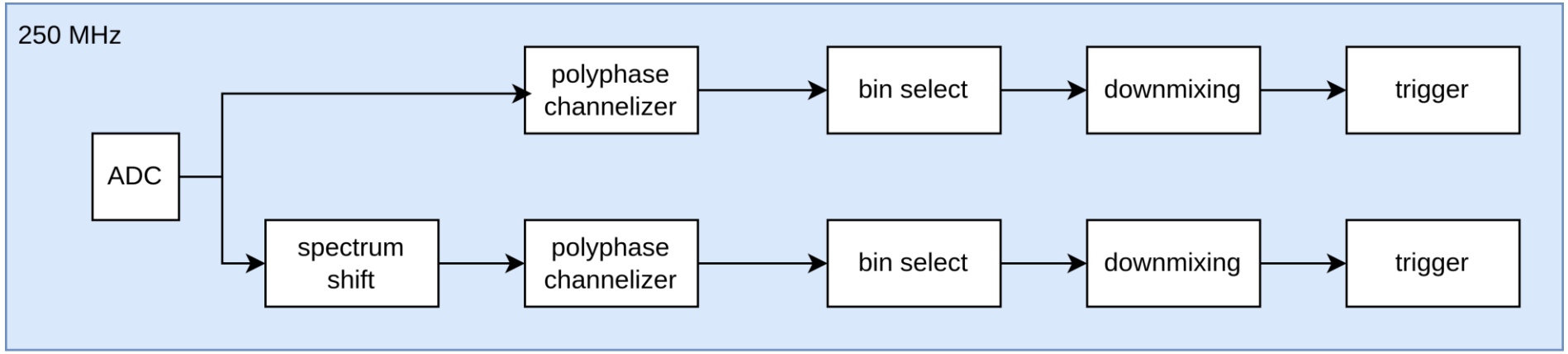


Agenda

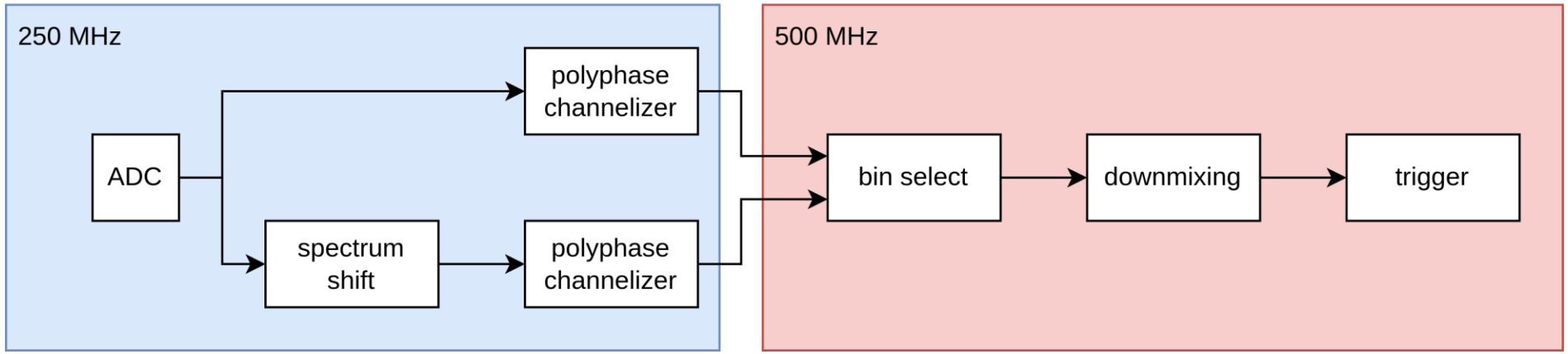
- Updates
  - Firmware
  - Build System
  - Hardware
- Intermediate noise characterization results
- Integration of the active veto
- Next steps

Firmware optimization

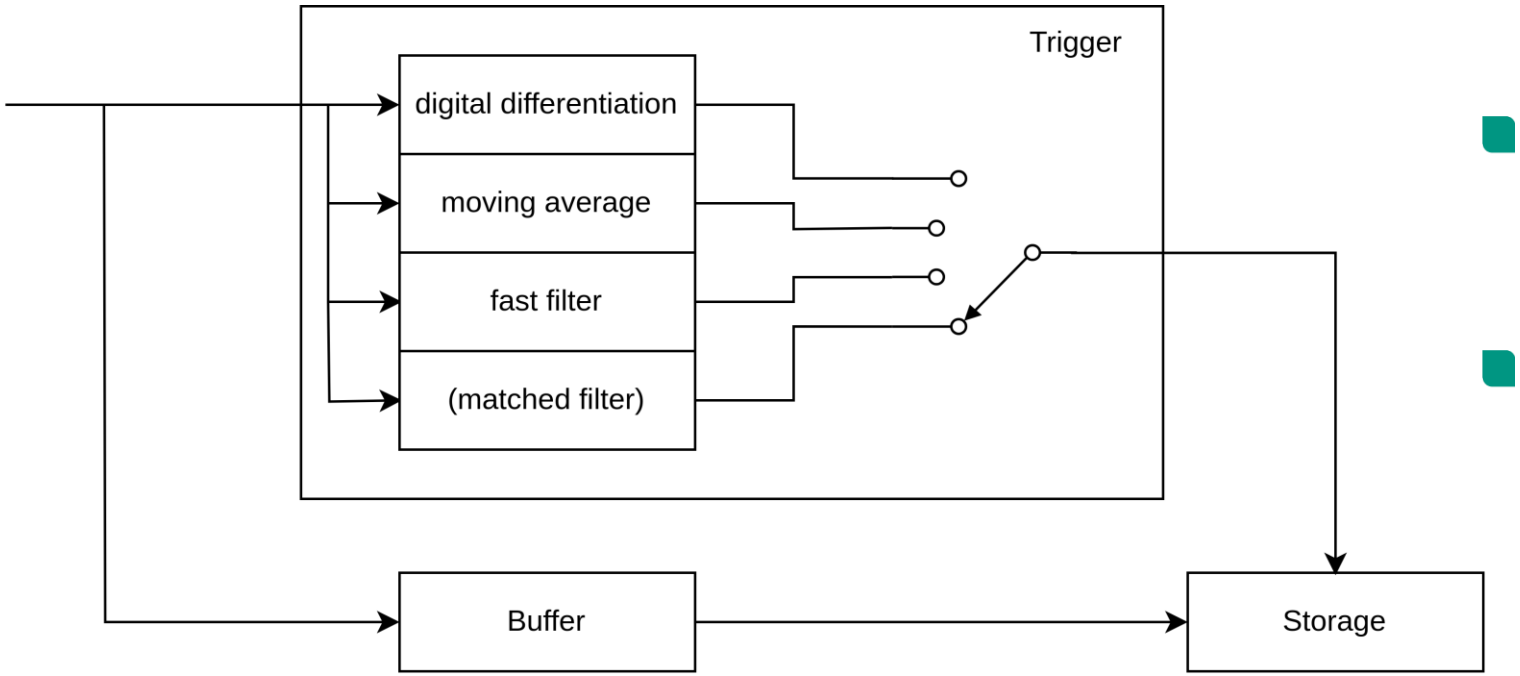
Old:



New:

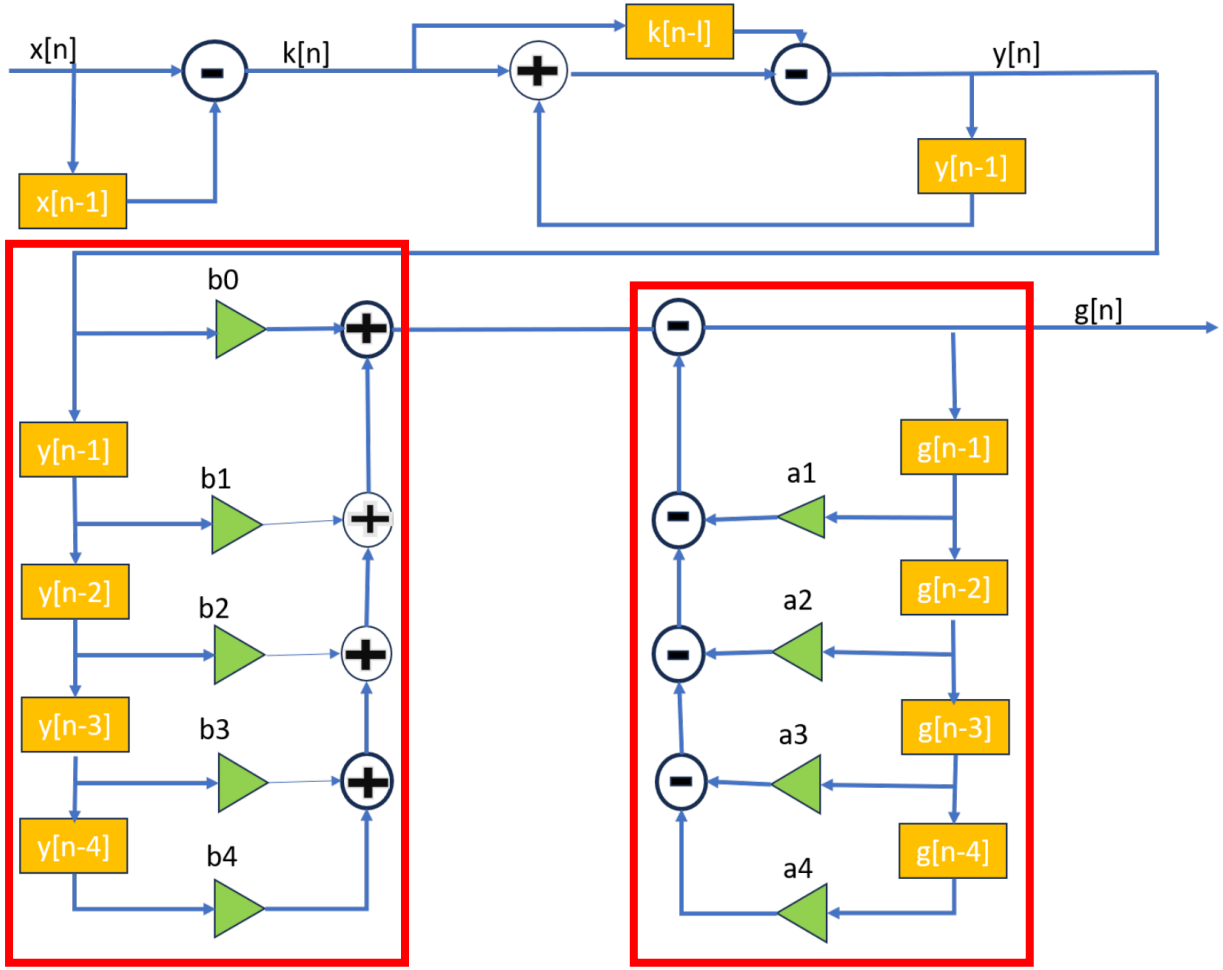


Trigger architecture



- Easy to extend with new triggers
- IIR „Fast Filter“ implemented
  Testing in progress
- Matched filter drafted,
  implementation pending

Implementation of Fast Filter Algorithm



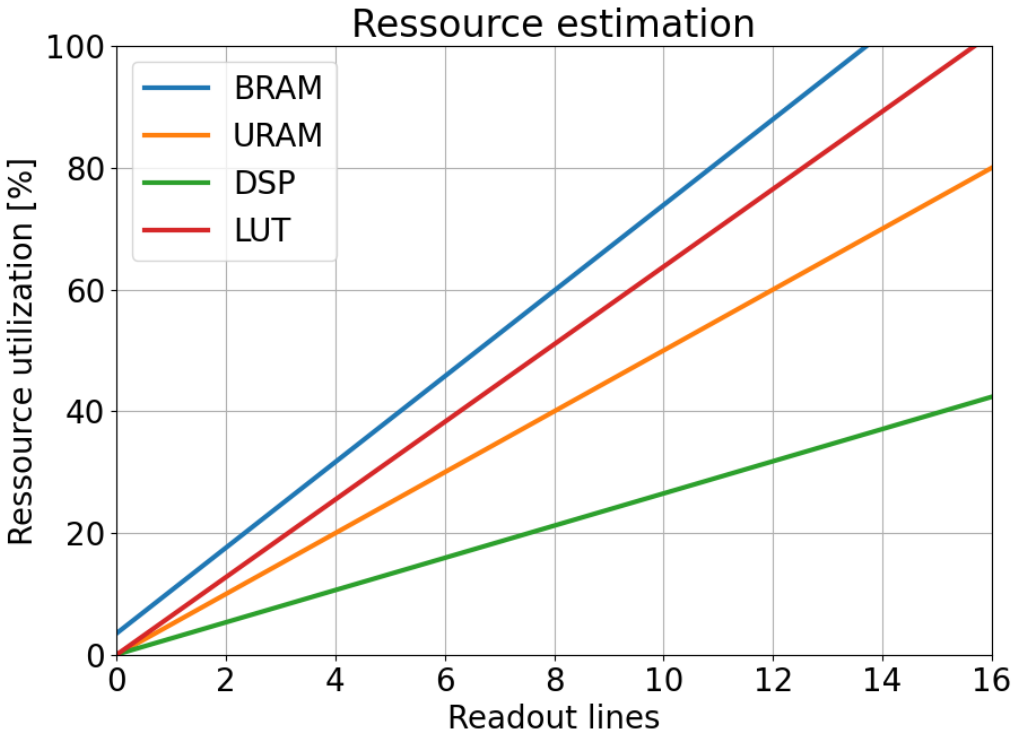
- IIR part of filter implemented as two FIR (possible due to TDM)
- „Simple“ FIR filter with custom taps also possible
- Works in simulation, some bugs in hardware

Further firmware updates

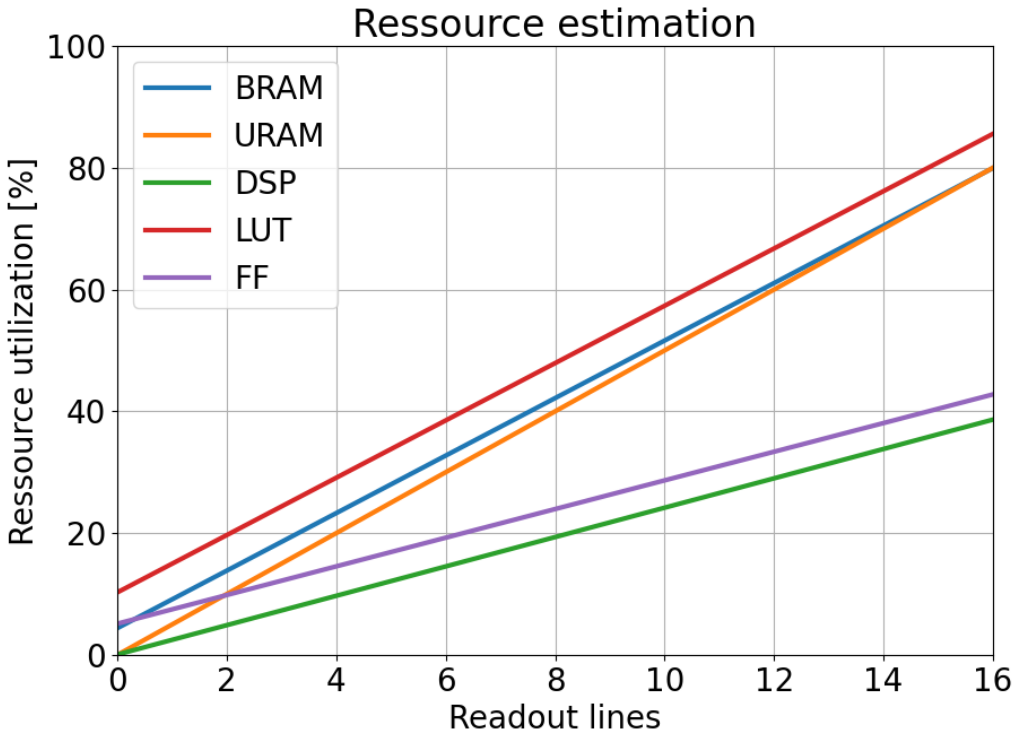
- Lots of bugfixing
  - trigger system
  - data storage -> Continuous streams to a file now possible
- Updated tooling: Vivado 2020.2 -> Vivado 2022.2
  - Faster synthesis & implementation time
  - Improved IP cores for converter interface & back-end infrastructure

Updated full-scale firmware estimation

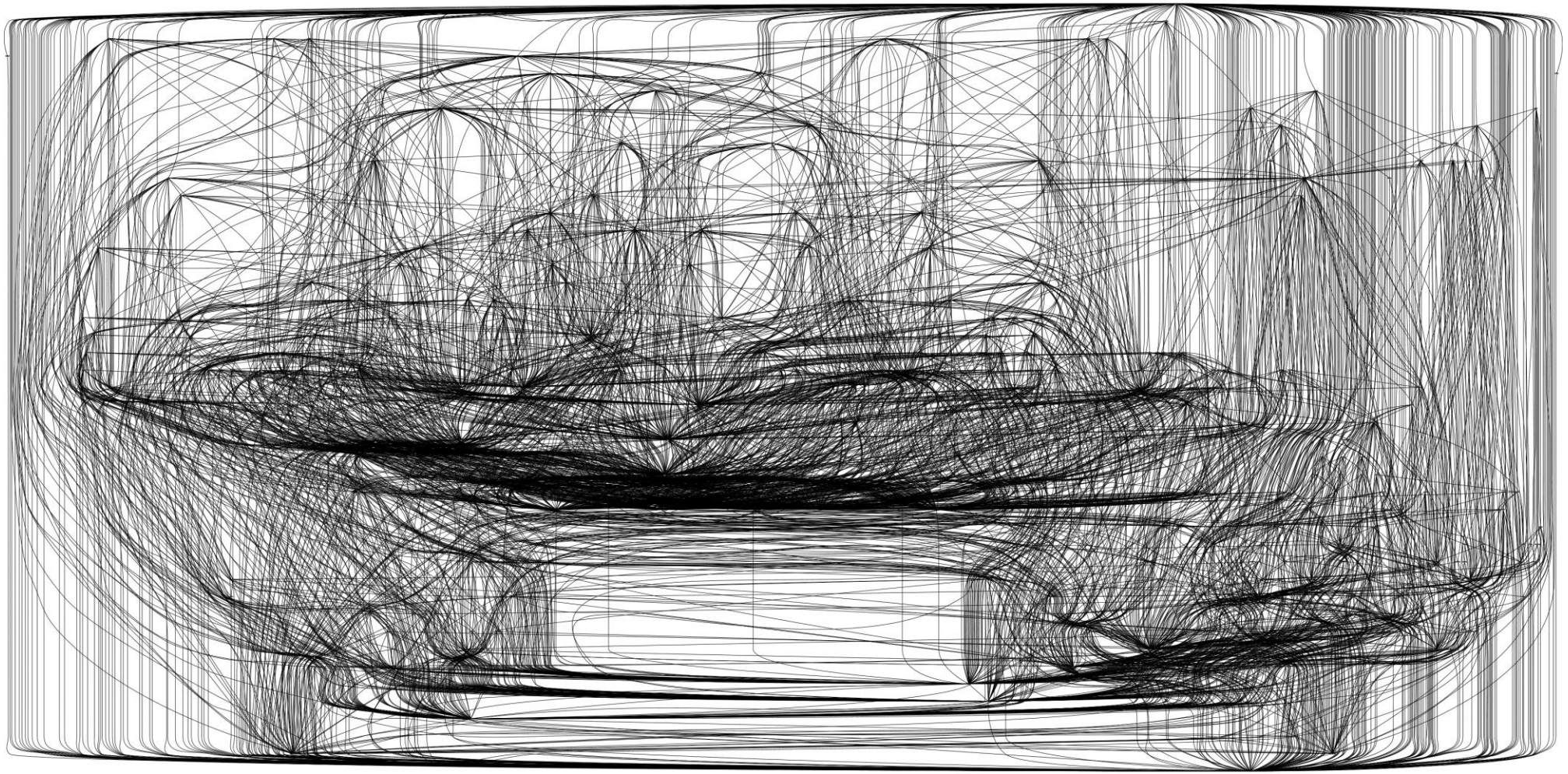
14.05.2025:



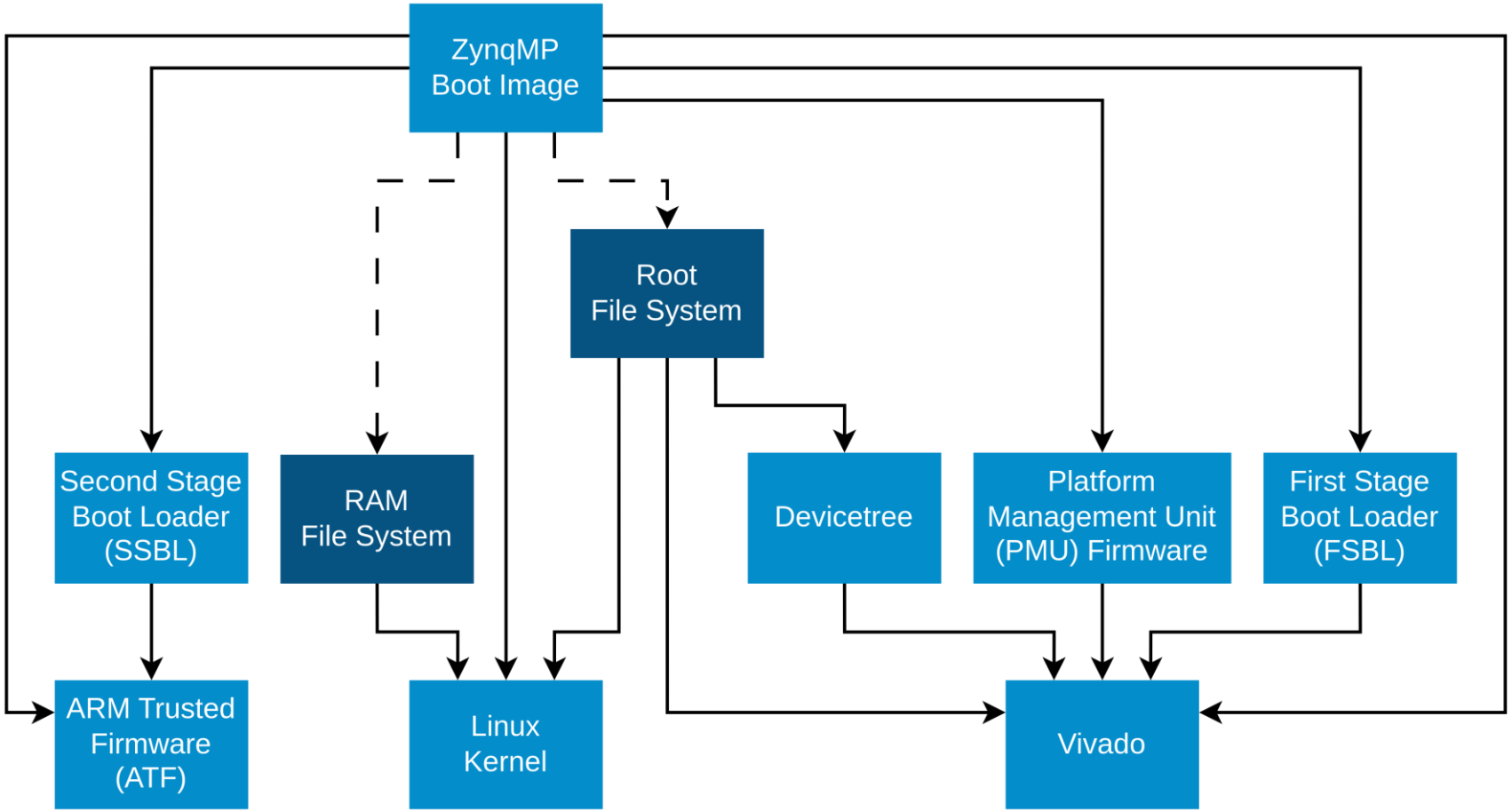
27.06.2025:



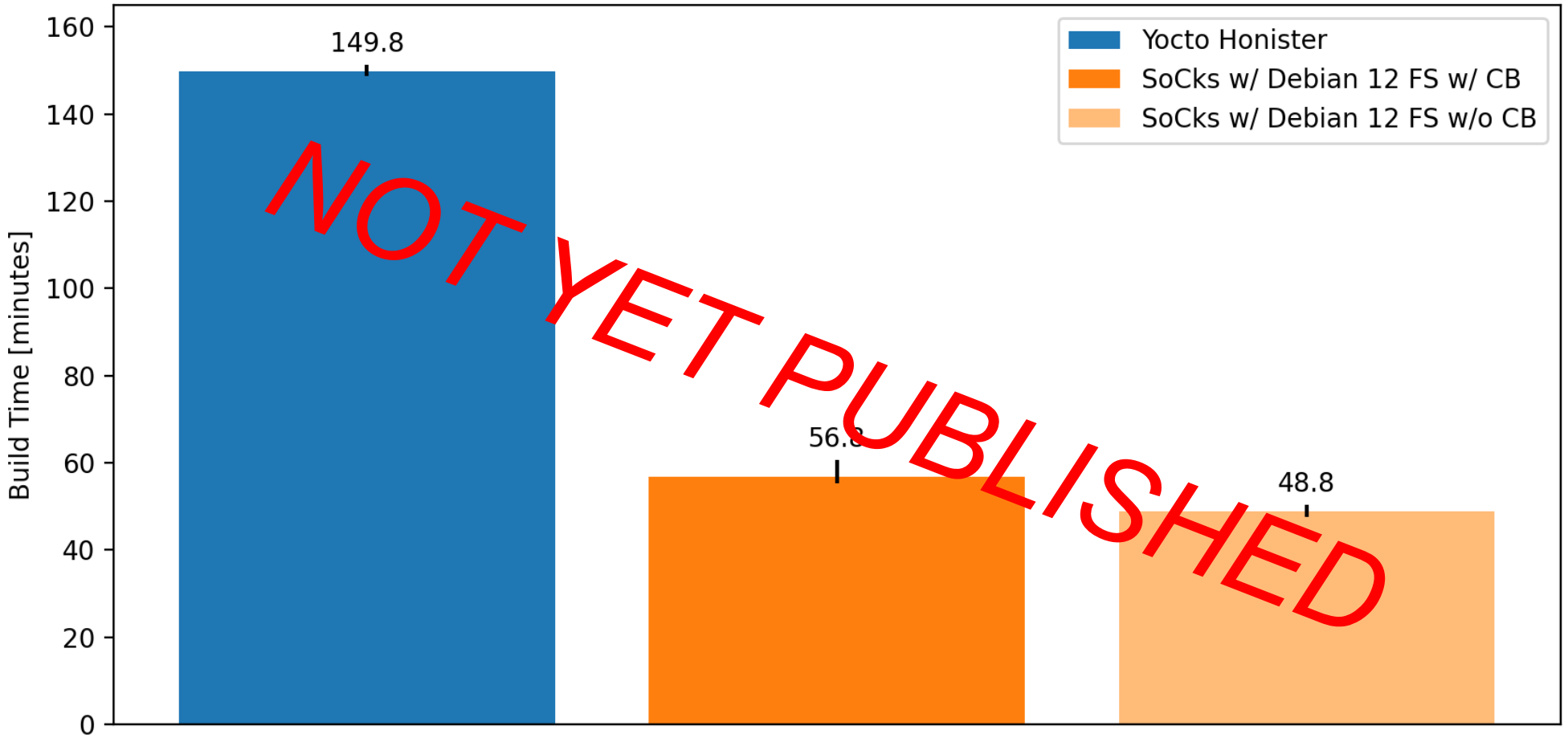
Dependencies of old build system (Yocto)



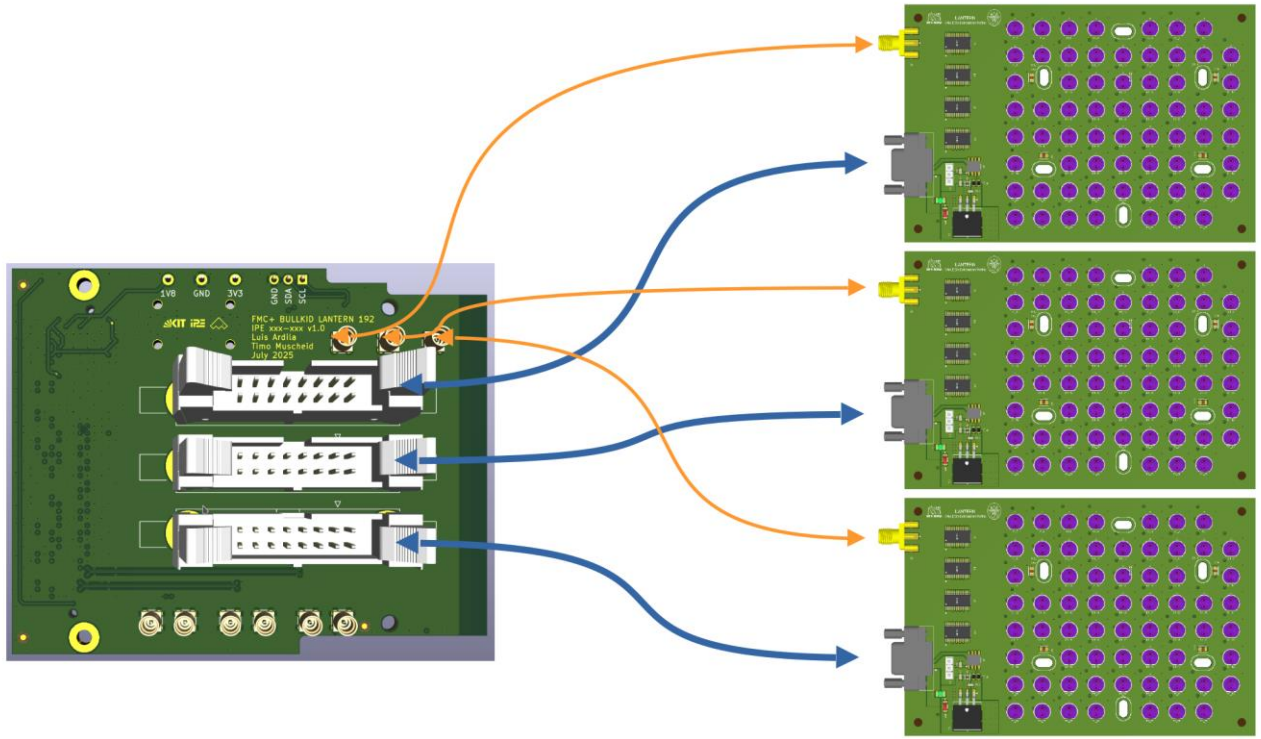
Dependencies of new build system (SoCks)



Improvement of new build system



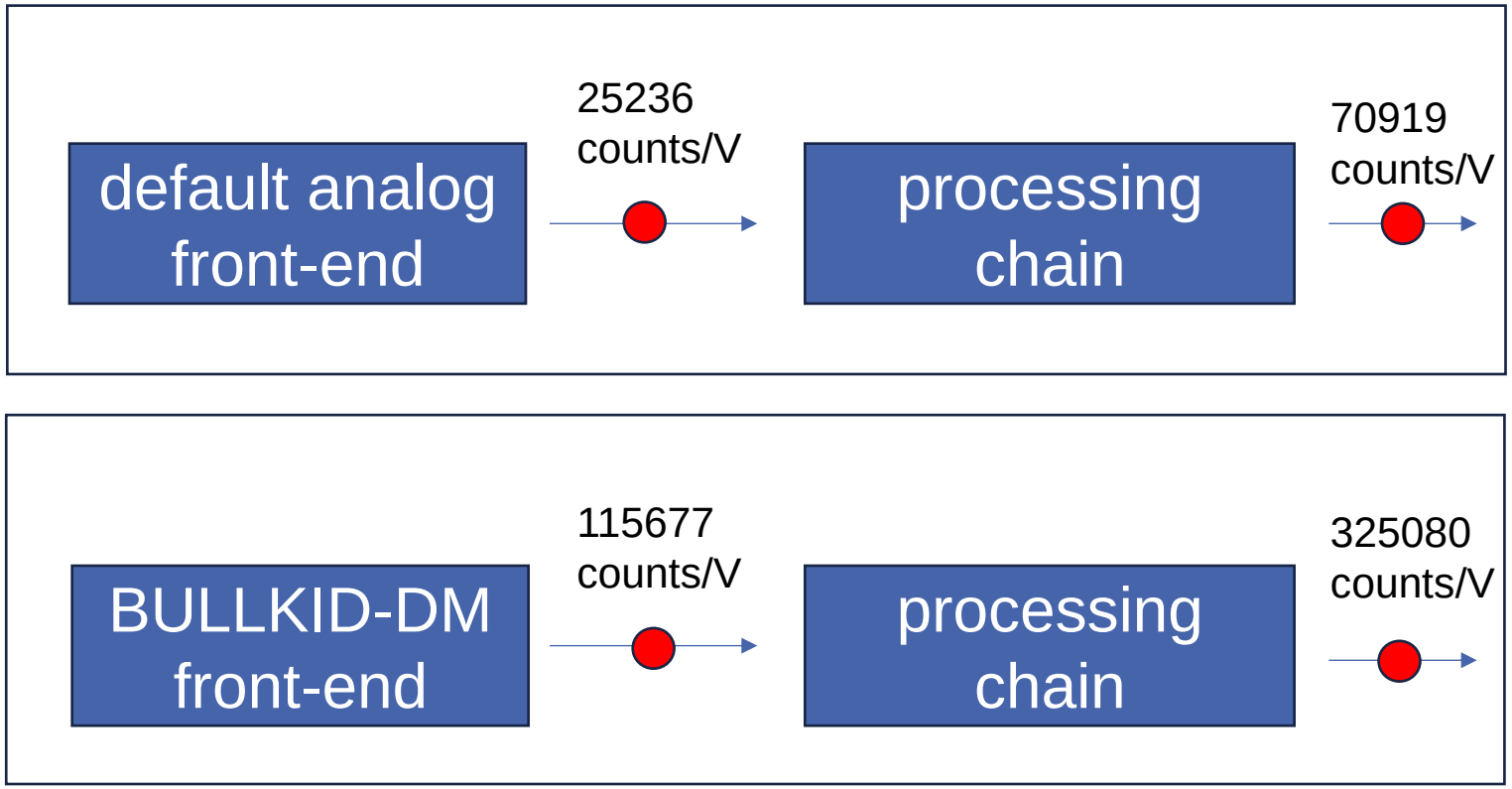
Integration of the calibration system



- Design of extension board for ZCU216 (FMC+ connector)
- Generation of control signals and trigger directly from DAQ system
- Support for up to 3 LANTERN boards

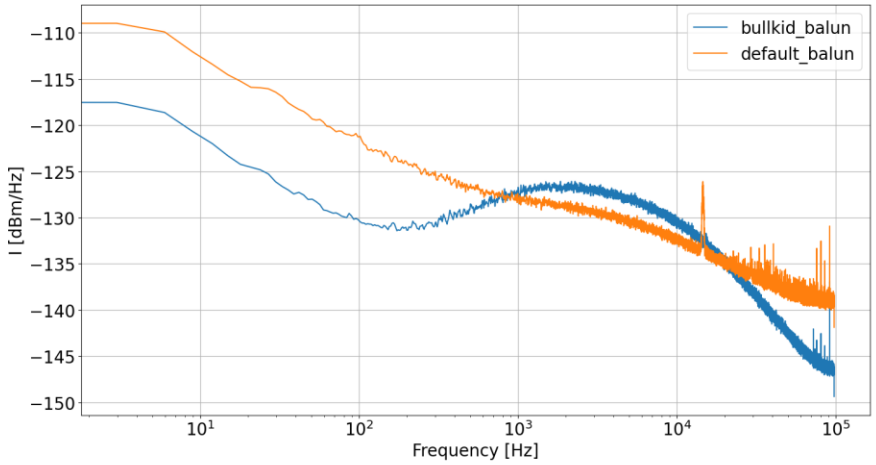
Noise performance

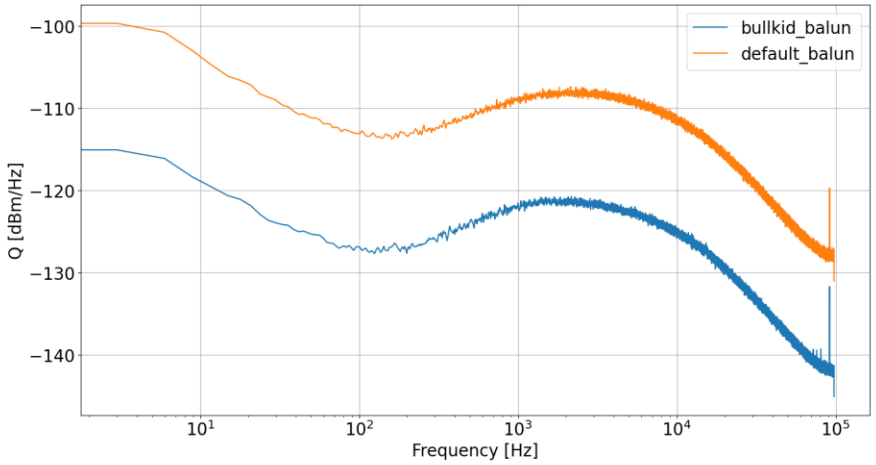
Signal generator:

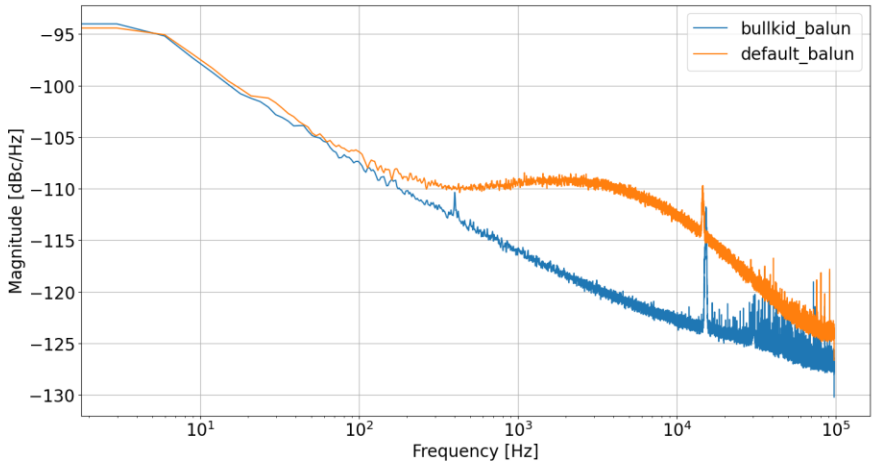


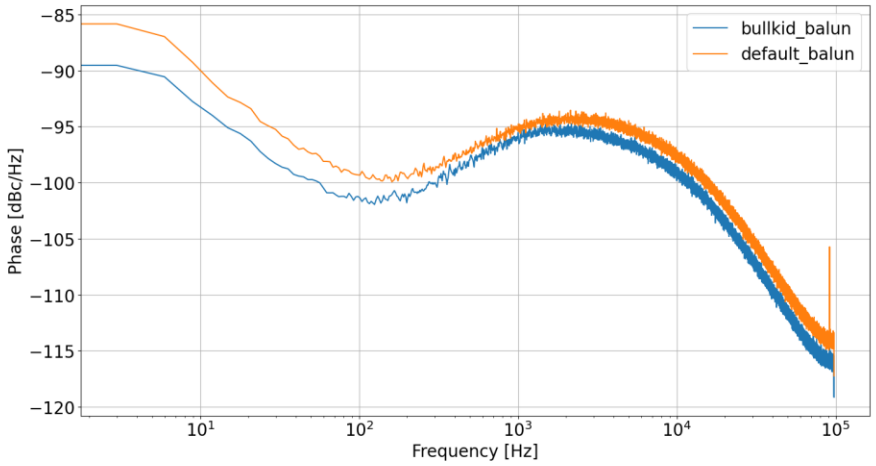
Evaluation of conversion factors: ADC counts / V

System noise



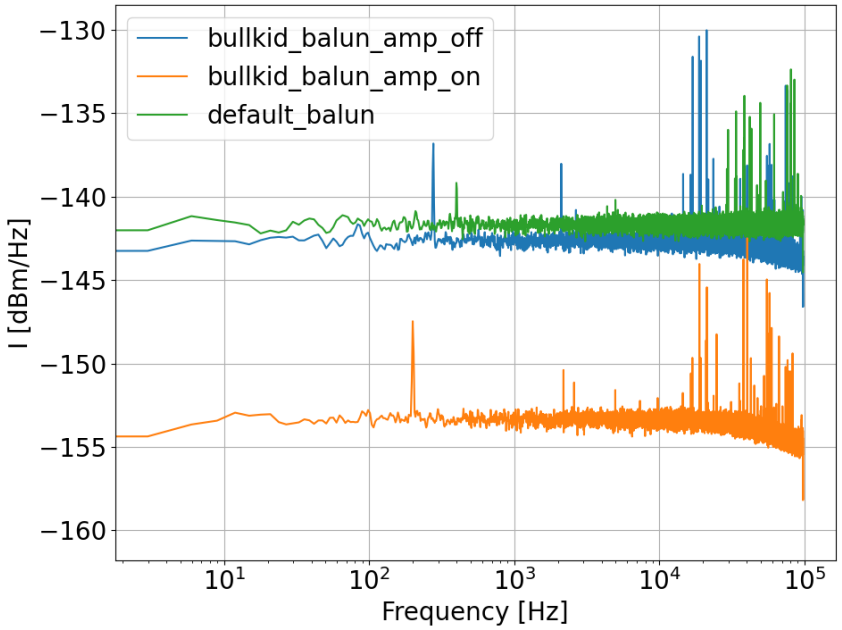


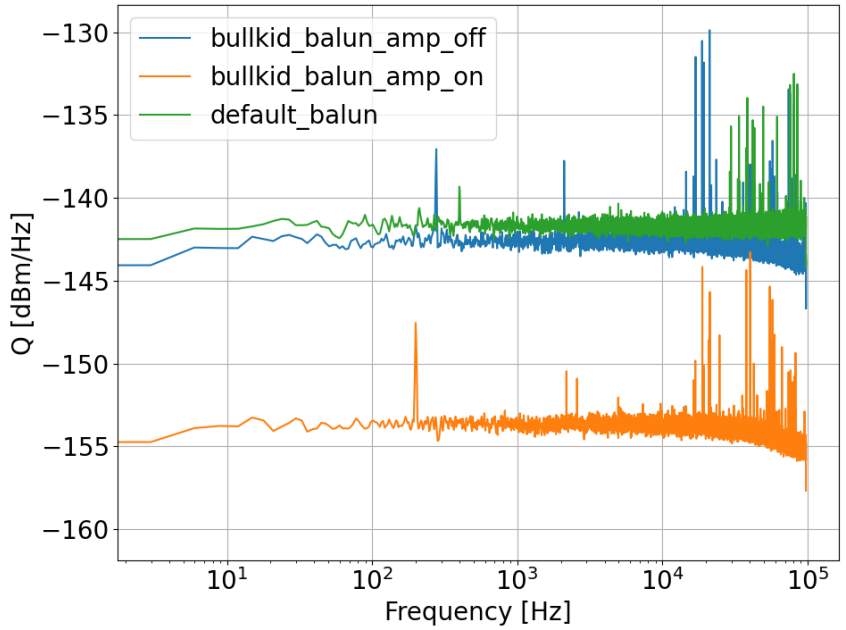




- Single tone
  - 830 MHz
  - -10 dBm
- Operation in loopback
- Measurement after the DDC

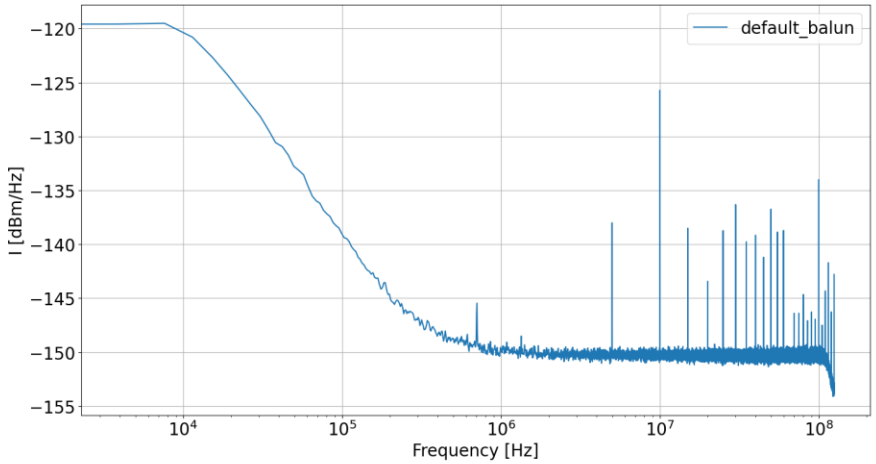
Noise of amplifier and ADC

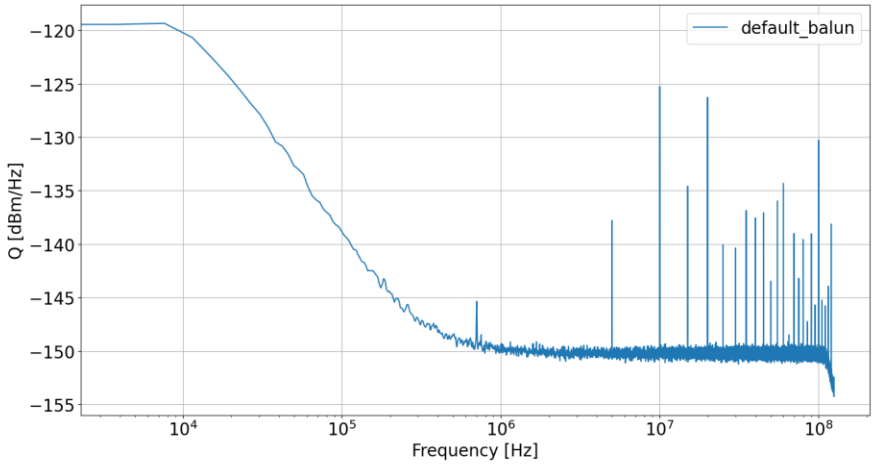


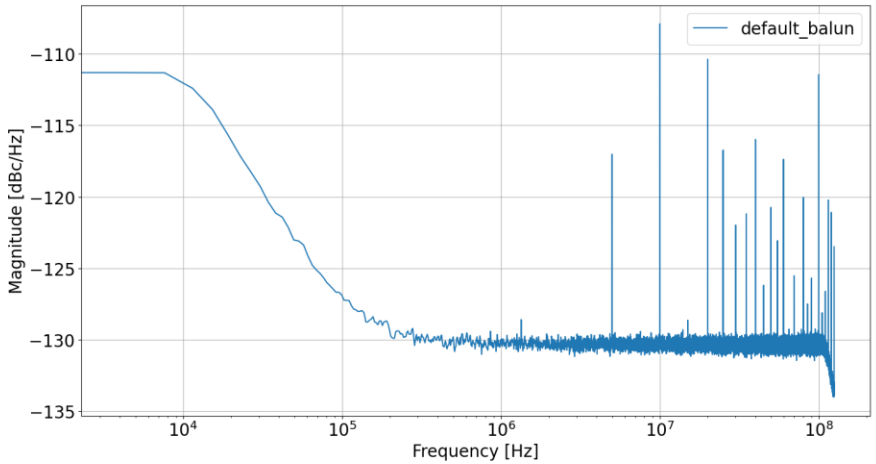


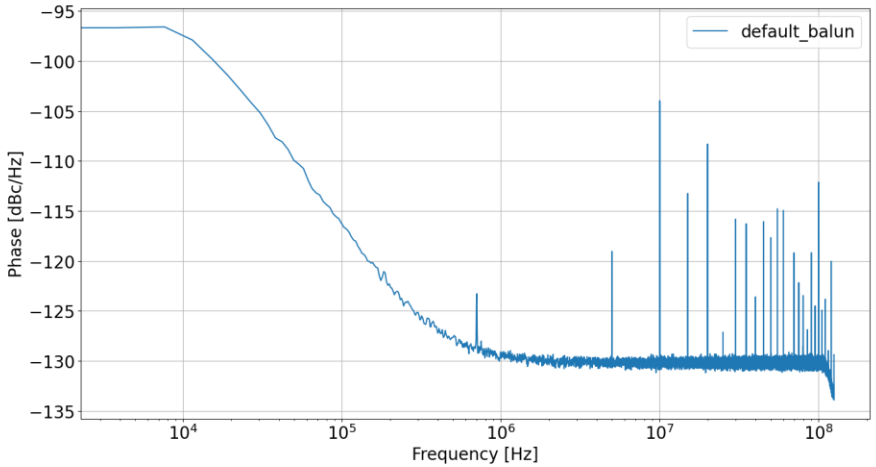
- 50 Ohm termination at ADC input
- Noise measurement after the DDC
- Quantization noise becomes dominant without amplifier

Loopback noise









- Single tone
  - 830 MHz
  - -10 dBm
- Operation in loopback
- Measurement directly after the ADC downmixing

Noise Evaluation

- Without amplification, quantization noise becomes apparent
- Custom analog front-end is better than default despite amplifier noise
- Noise influence of ddc chain needs to be investigated further
  - Where does the hump in the phase noise come from?
  - Analyse different parts of the ddc chain individually

Discussion: Integration of active veto

Integrated approach

Use one of the 16 TX/RX pairs of the RFSoC and existing analog frontend

- Easier system design
- Ready to use

- Support for max.15 wafers

Modular approach

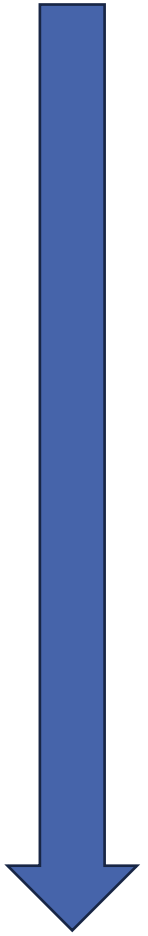
External DAC/ADC pair connected to FPGA

- Components could be specifically set for desired frequency range

- More complex hardware architecture

Next steps

- Later this week:
  - Continuation of noise analysis in Rome
  - Integrate DAQ into measurement scripts
- This summer:
  - Implementation of Matched Filter
  - Optimization of channelization chain
- Later this year:
  - Multi-wafer readout (3 stack demonstrator)
  - Readout of 145 pixels



Short term

Long term