

No Image  
Available (yet, but...)

# RDO roadmap

(+ some news from ePIC DAQ)

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1

- Ok for 8 RDO production (July 2025)

2

- Readiness for test beam (Nov. 2025)

3

- Radiation tests @ Trento (Dic. 2025)

4

- Towards ePIC DAQ (... [production in 2027 anyway!])





# RDO next steps for go for production (8 RDOs)

1. Mechanical pairing with fake-FEB
2. Power-up : 2.5 / 1.4 jumper to avoid power to other sections
3. Prg uC via external connector
4. Power-up with uC (post-programming uC): check Vout LDO
5. Prg Artix via external connector
6. Prg Polarfire via external connector
7. Prg Artix → SkyWorks (programming 125 MHz of Si5319)
8. Check consumptions
9. Check UFL I/Os
10. Link IPBUS via VTRX+ [MT-MPO adapter + "polipo"]
11. Prg ALCOR via fake-FEB (via IPBUS → VTRX+)
12. ALCOR readout (via IPBUS → VTRX+)

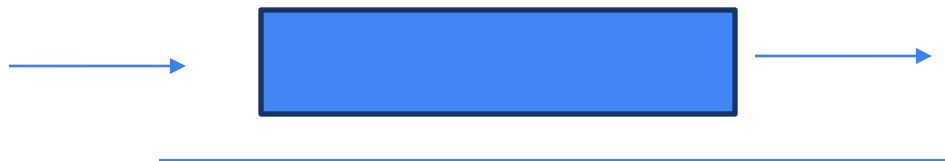
Note: we can't test everything before give the "go" for next 8 RDOs...  
Note: we should get 2 first RDO by 10 June...



1. External clock processed by SI5326 (note: we need 16 SMA-UFL cables)
2. Readout of all I2C sensors
3. I2C programming of regulators on fake-FEB
4. Manage different IP (without jumpers)
5. Cooling ?!
6. A mini rack: 8 RDO + fake-feb on both sides etc...

Optional (bonus):

1. IPBUS + UDP streaming





1. Writing QSPI Flash via SPI (writing via JTAG)
2. Scrubbing
3. Communication between PolarFire and Artix
4. Current monitor via uC
5. Communication between uC and ARTIX

Optional (bonus):

1. Polarfire program ARTIX at boot
2. QSPI Flash writing via IPBUS (Remote Programming!)
3. During the test: one fake-feb connected and we read 2 ALCOR32? (note: ALCOR not exposed to radiation)



- Check noise from charged pump
- Check noise (light) from VTRX+ / engineer “shield”
- Link EIC → clock reconstruction (need project input)
- Clock at 394 MHz/ ALCOR@394 MHz (can we do that with ALCOR32?)
- Polarfire program Artix at boot
- Remote programming (writing PolarFire via VTRX+)
- Remote programming (writing Flash memory via VTRX+)
- IPBUS → EIC link over VC709/707
- Data format // buffering // “frame”
- Test with ALCOR64 + FEB
- Test with FELIX
- test in campo magnetico (PDU)
- PDU in detector box etc...
- **pre-production** during 2026 (if we don't need it before) “RDO26”
- test card for testing RDO

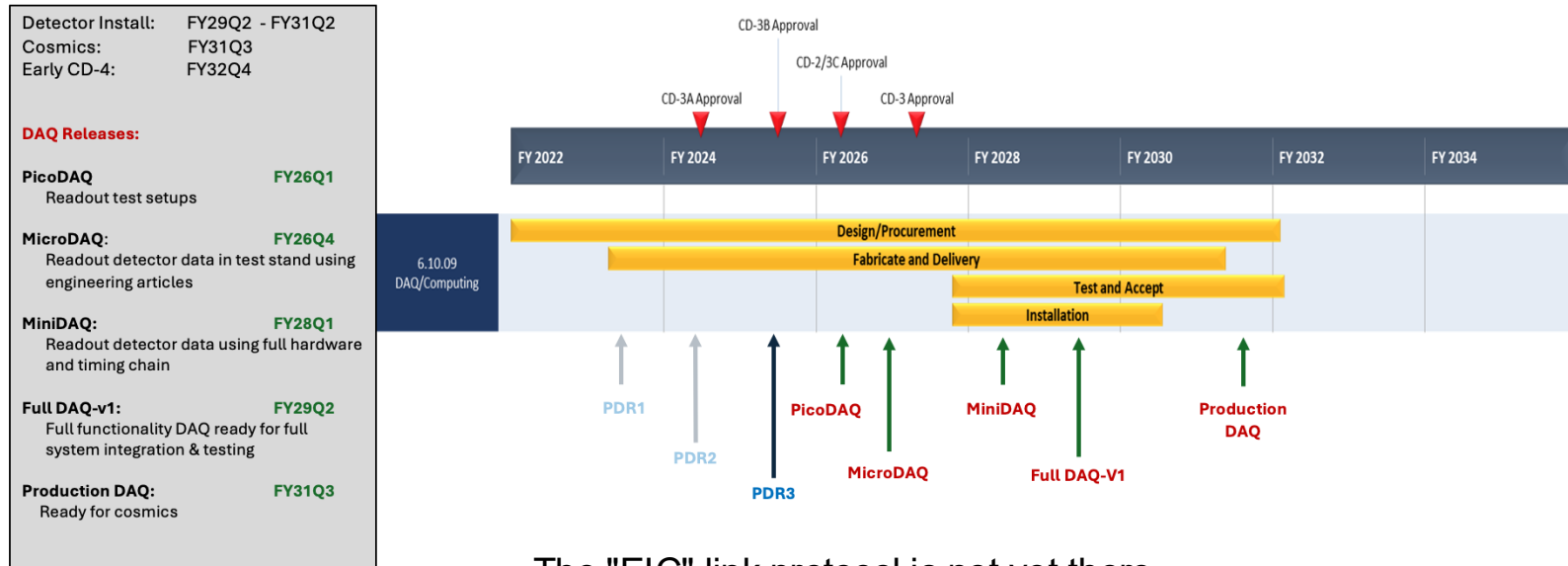
TB2026: dismount leds!!

TB2026: le FEB sono compatibili con RDO25



# Some news from ePIC DAQ (I)

## PicoDAQ development --- Streaming DAQ Milestones



- The "EIC" link protocol is not yet there
- "MicroDAQ" will not provide that
- ALINX AUX15P is now popular and there are ideas to use it as "proto-RDO", proto-DAM and proto-GTU

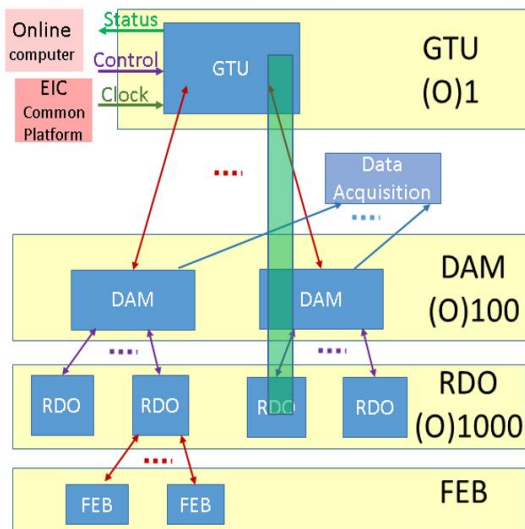


# Some news from ePIC DAQ (II)

this is to support detectors with IpGBT, but per se we could consider to use IpGBT protocol (Rome1 would be in favour...)

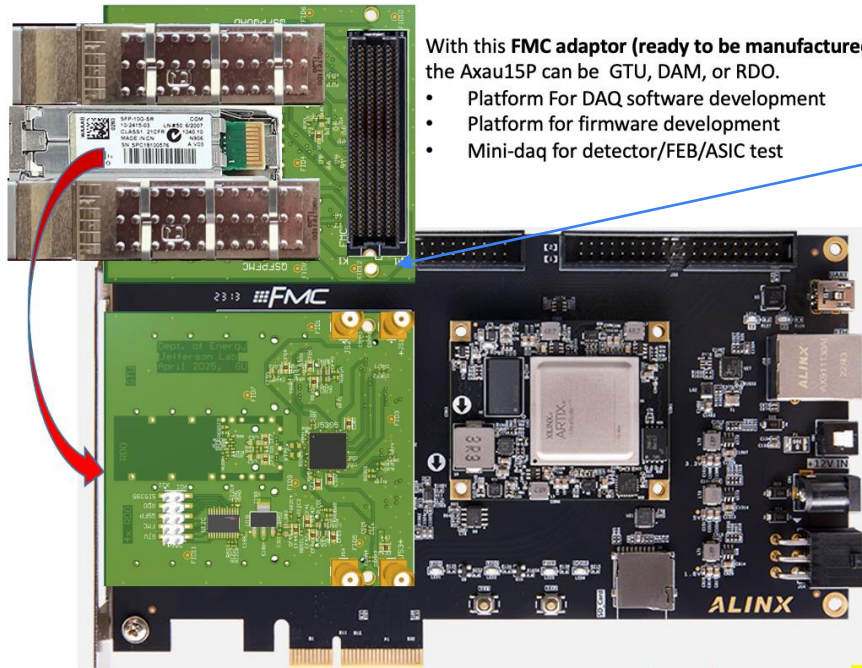
## 1. The ePIC designs

System Clock: **19.7 MHz** (1/5 of BX 98.5MHz)



Mini\_DAQ, functionally includes GTU, DAM, and RDO

## 2. FMC/(Q)SFP adaptor



With this **FMC adaptor** (ready to be manufactured) the Axau15P can be GTU, DAM, or RDO.

- Platform For DAQ software development
- Platform for firmware development
- Mini-daq for detector/FEB/ASIC test

Once this piggy back card is produced (by Jlab), this would allow to use a pair of ALINX/AUX15P to mimic a "RDO" and "FELIX" link

And we could use our RDO at that point...