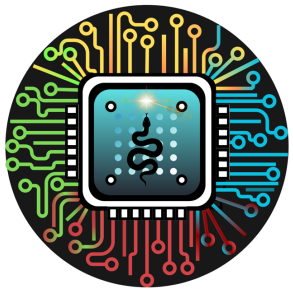
ASPiDeS
A CMOS SPAD and Digital SiPM platform for High Energy Physics

Lodovico Ratti

Università di Pavia and INFN Pavia

(lodovico.ratti@unipv.it)



WP2 meeting

https://cern.zoom.us/j/6401428621

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Digital SiPM characterization

- DCR
  - SPAD enalble/disable; output of the counter or of the NAND/NOR tree (400 ps pulse from the internal monostable circuit)
- Cross-talk
  - SPAD enalble/disable; output of the counter
- After-pulsing
  - SPAD enalble/disable; output of the NAND/NOR tree (distribution of the number of counts, a counter could be added)
- PDE
  - SPAD enalble/disable; output of the NAND/NOR tree or counter
- Counter output delay
  - SPAD enalble/disable; test signal; counter output
- NAND/NOR tree jitter/dispersion (fixed pattern jitter)
  - SPAD enalble/disable; test signal: NAND/NOR tree output

I/O signals

- GLOBAL RESET (fast): resets in pixel memory (and counter)
- GATE (fast): enables front-end electronics
- ENABLE/DISABLE (slow): enables/disables both front-end electronics and SPAD
- TEST (fast)
- COUNTER OUTPUT (11 bit)
- NAND/NOR OUTPUT