Design of a multi-function ASIC for reading out large SiPM-based systems

Università di Siena & INFN Sezione di Pisa
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FCC Pisa , May 29, 2025

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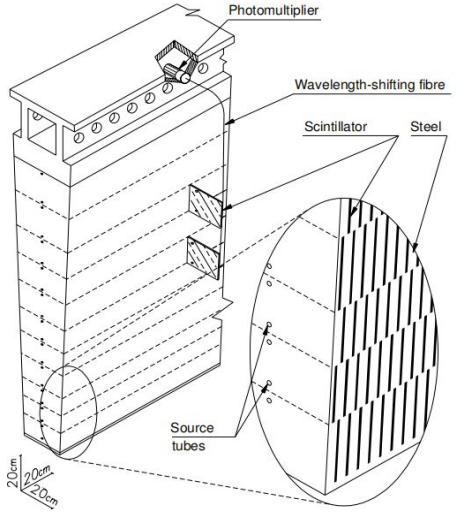
Introduction

- The idea of developing a new device for handling analog inputs from a multichannel photo-sensor arose from TileCal need to enhance readout granularity for the HL-LHC era by replacing single-anode PMTs with MA-PMTs, while minimizing the increase in digital readout channels.
- Unfortunately, the timing and commitment of the institutes in the upgrade phase of the experiments for HL-LHC make it impossible to enhance the readout granularity of TileCal during the high luminosity phase.
- **Still, the concept remains valuable for future calorimeters that will benefit from a fully configurable readout system.**



Just a few examples

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Configurable sums of energy deposit would allow to use the same device for defining trigger towers in different regions (barrel/forward/end-cap) and for different calorimeter sections (e.m./hadronic).

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3) Hadron sampling calorimeters à TileCal (ALLEGRO HCAL barrel), with SiPM readout

Dynamics definition of Regions of Interest (ROIs) for energy deposits would improve both the separation of small radius jets and the definition of the contour of merged jets in hadronic decays of boosted particles.

General architecture for the new device

- The solutions currently available on the market involve the digitization of all channels *

*MUSIC ASIC architecture

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Advantages:

Apply digital filters to dump the noise

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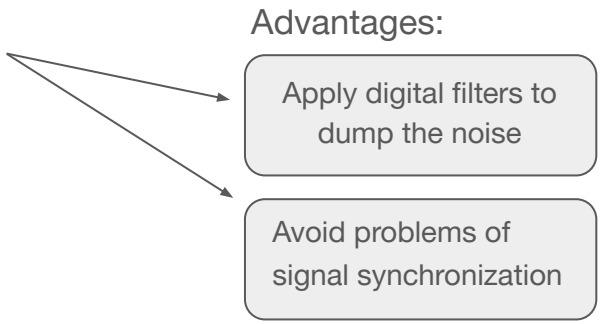

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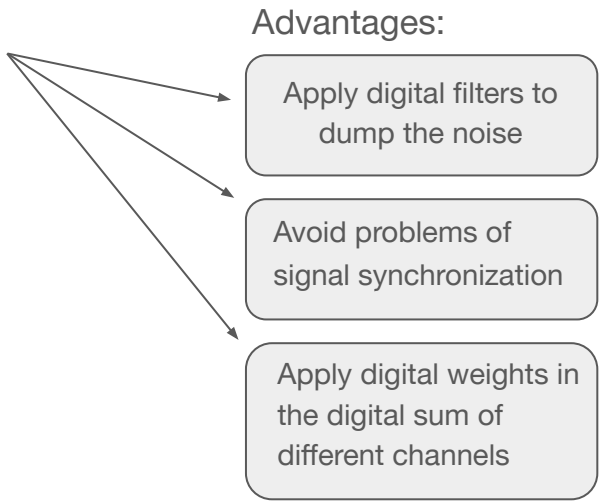

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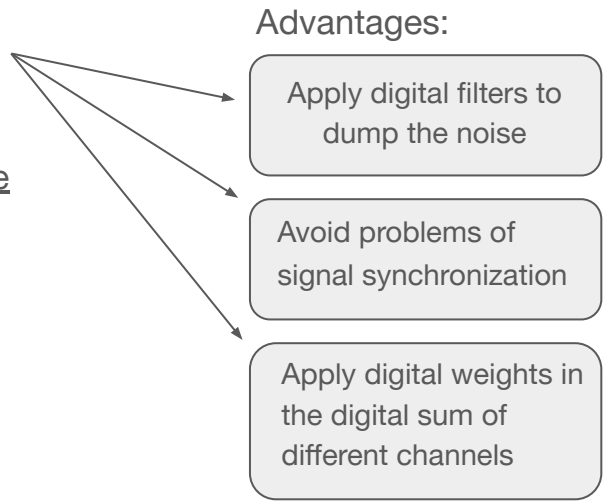

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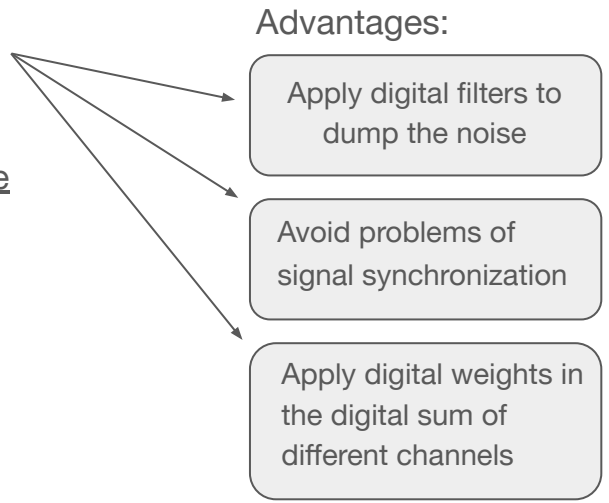

- We want to invert the concept flow chart:

  ➡ **first make an analog sum of selected subsamples of readout channels, than convert only the desired sum(s)**

- The challenge is to avoid distortions of the time profile in the resulting analog sum and to keep at the same time all configuration flexibility that the other concept allows.

*MUSIC ASIC architecture

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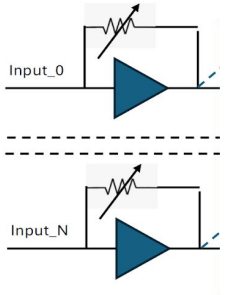

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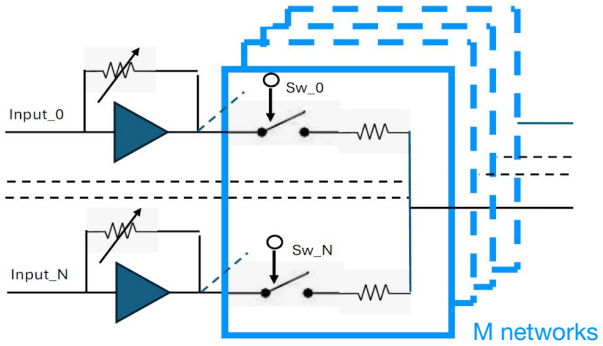

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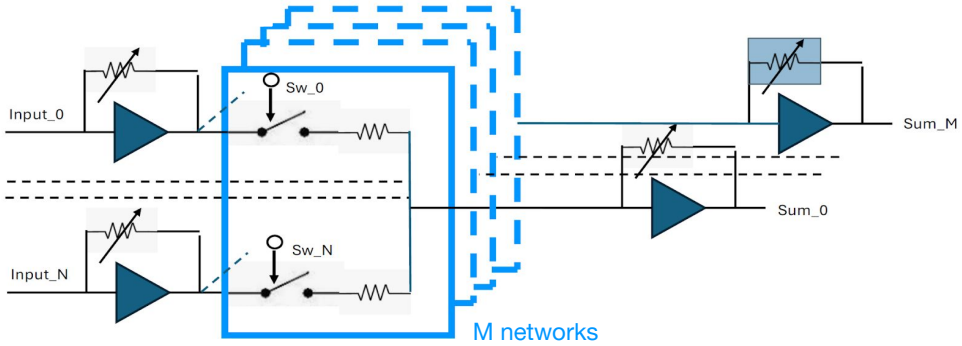

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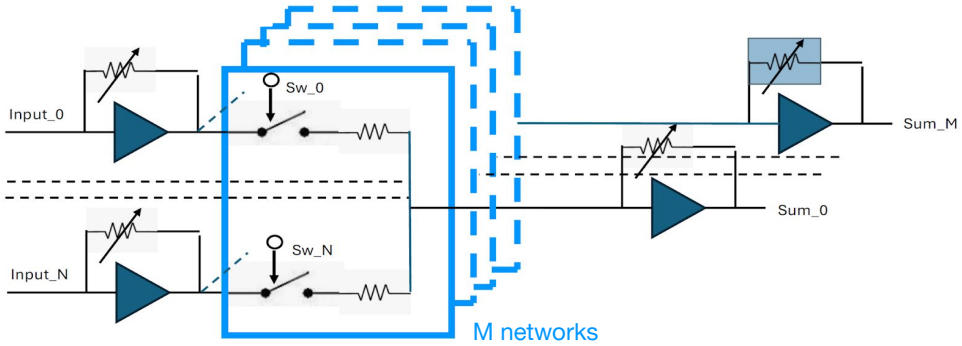
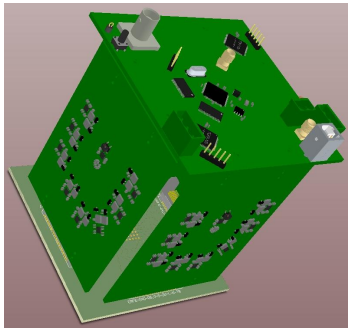


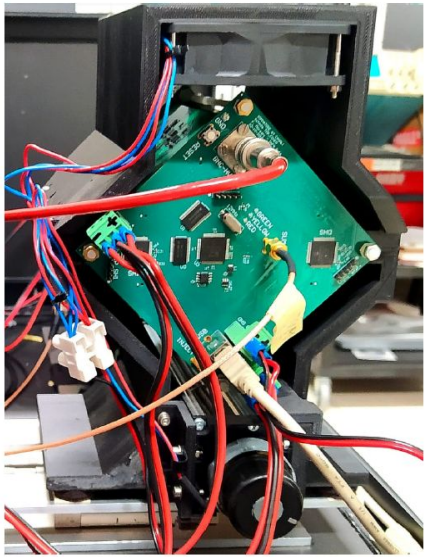
What was done?
A prototype for this type of readout with high-bandwidth integrated circuits was designed, built and tested at INFN Pisa.

Prototype description

- Designed and developed by Dr. Fabio Morsani
- The system is composed by **6 Printed Circuit Boards** (PCBs), built with high-bandwidth Integrated Circuits (ICs).

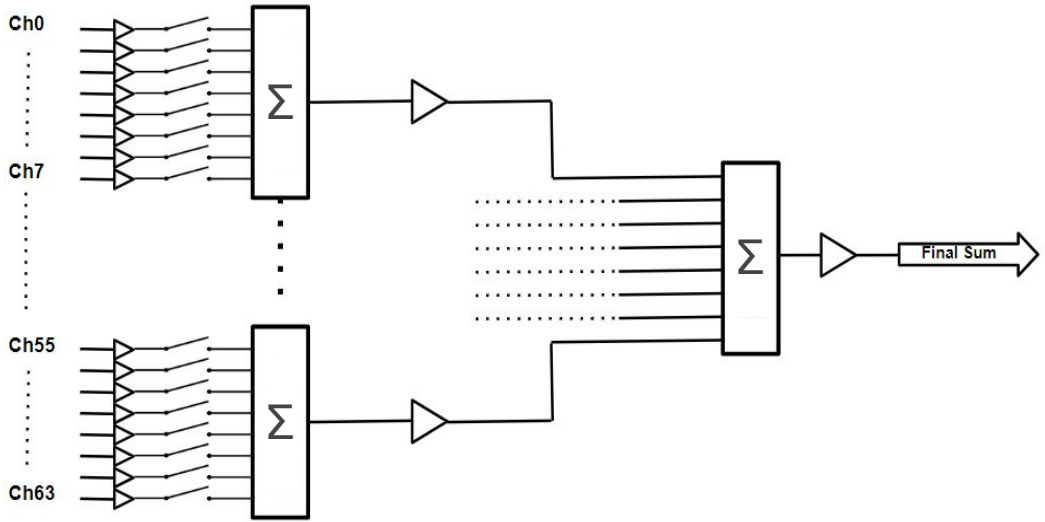


- As a first proof of feasibility no constraint on system dimensions, nor on power consumption (25 W) was applied.
- The 6 PCBs are arranged to form the faces of a parallelepiped with a square base and are assembled inside a metal support structure which also houses a cooling system.



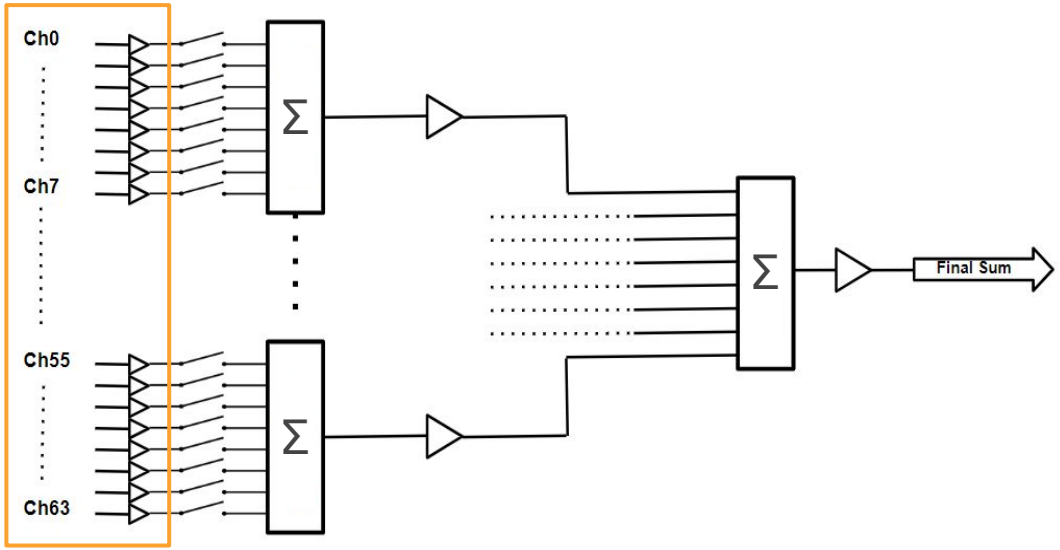
Description of the prototype functioning (I)

Circuit schematic of the prototype



Description of the prototype functioning (II)

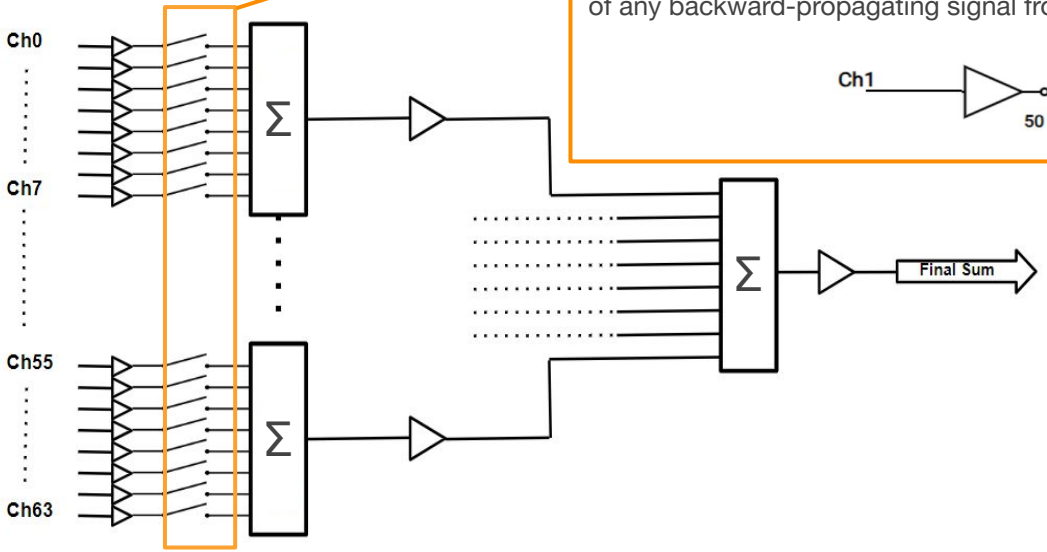
Circuit schematic of the prototype



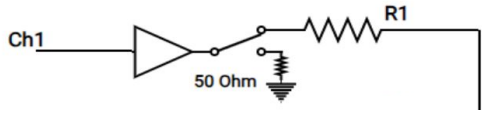
➡ Channels are first amplified with a configurable gain in a range between -6 dB and 26 dB (first amplification stage, equalization).

Description of the prototype functioning (III)

Circuit schematic of the prototype



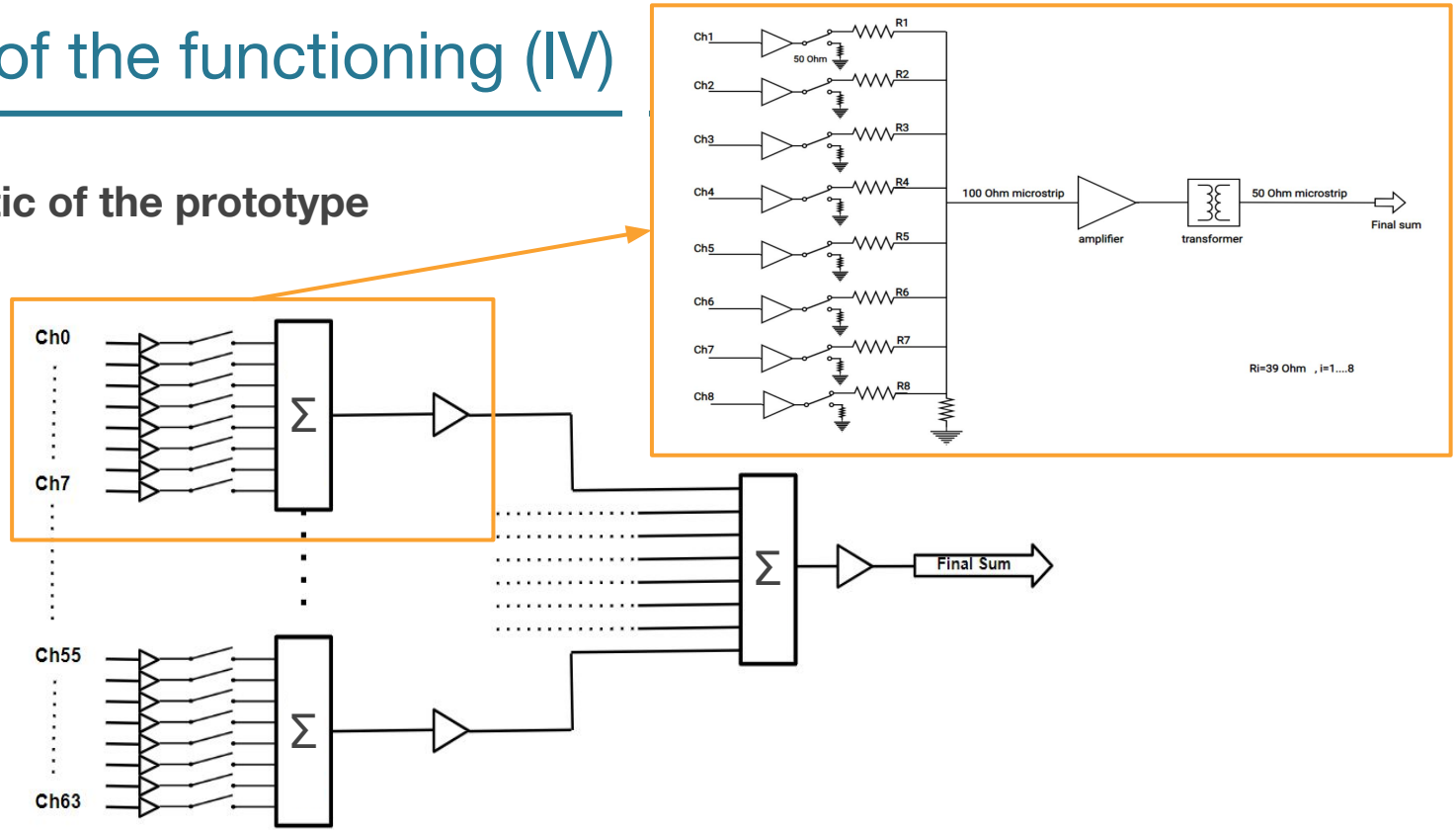
More info: The switches enabling the channels to enter the analog sum are SPDT switches (Single Pole, Double Throw) with a bandwidth of 3 GHz and high isolation. In the OFF mode, a 50 Ω resistor is switched onto the output line to ensure minimal reflections of any backward-propagating signal from the summing network.



➡ The channels participating in the final sum are activated via switches.

Description of the functioning (IV)

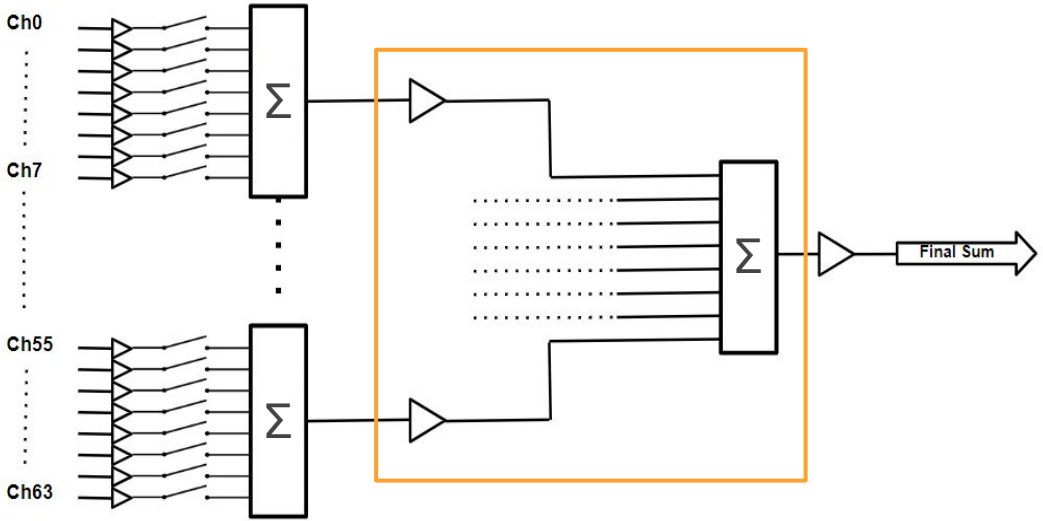
Circuit schematic of the prototype



➡ The 64 amplified readout channels are fed to eight 8-channel resistive summing networks.

Description of the prototype functioning (V)

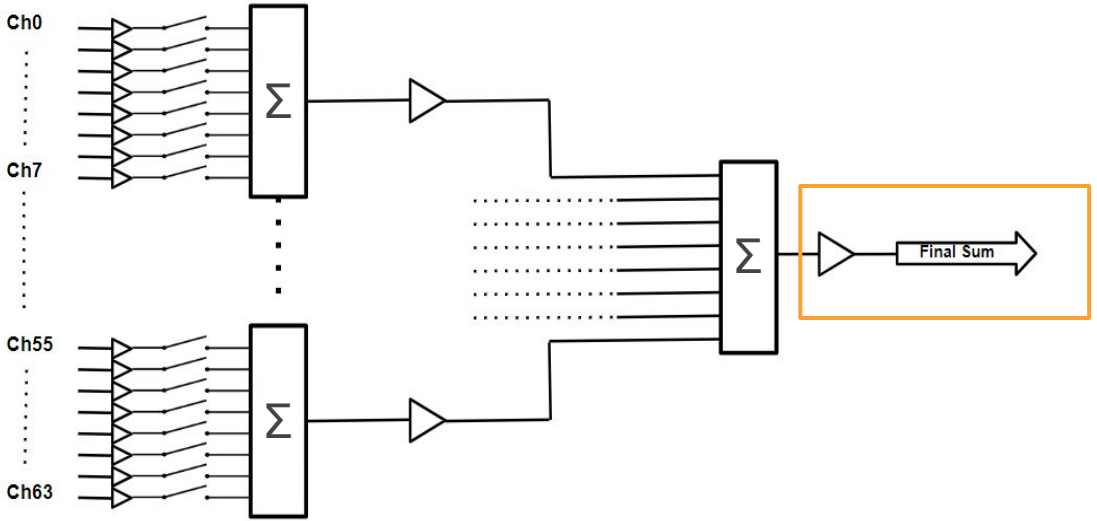
Circuit schematic of the prototype



➡ The output of each 8-channel network is amplified before being fed into a resistive network for the final sum.

Description of the prototype functioning (VI)

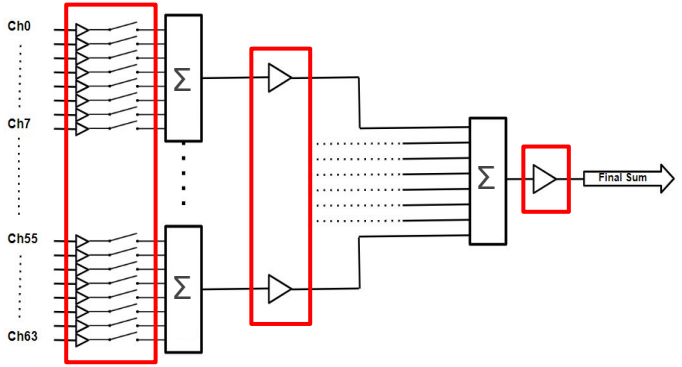
Circuit schematic of the prototype

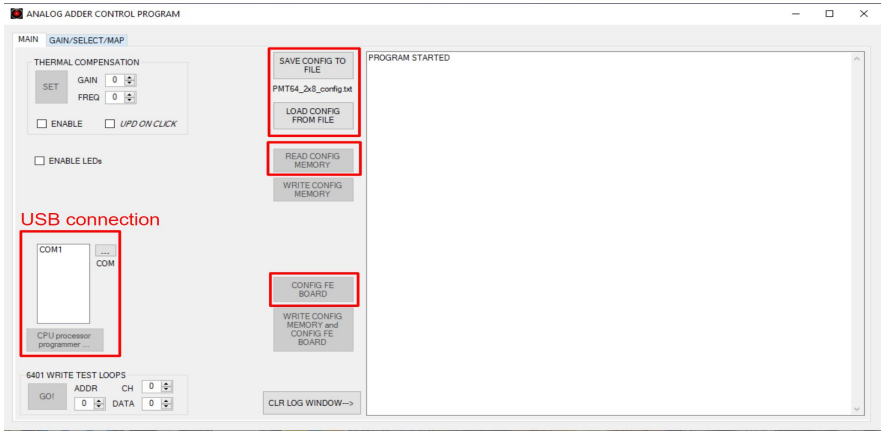


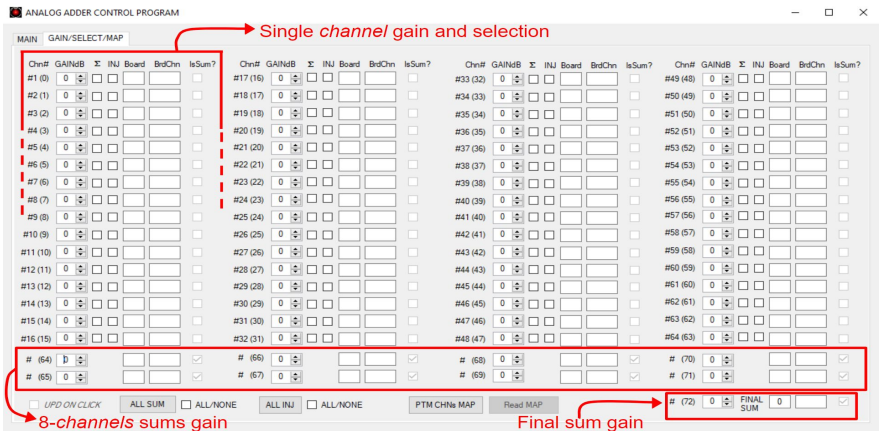
➡ The final analog sum can be further amplified to match the dynamic range of the ADC used for signal digitization. The gains of the three steps are configurable in a range from -6 to 26 dB.

GUIs

- The selected channels and all amplifications can be set through a GUI, allowing to establish USB connection with the prototype and to upload the selected configuration for the final sum.

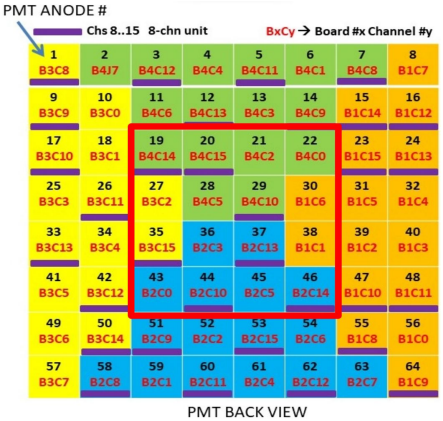






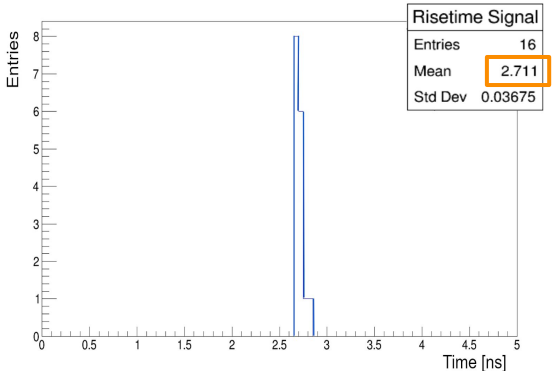
Prototype tests: introduction

- The prototype has been tested in Pisa in terms of pulse shape stability and linearity of the analog sum of an arbitrary number of channels.
- Various tests were done with two different experimental setups:
  - test of the 16 central readout channels injecting an input signal
  - test of the readout system using a MAPMT and a laser system



Prototype tests results

- The readout prototype guarantees pulse shape stability and linearity in the analog sum of the signals (rise times ~ 2.7 ns);



Single channel rise time distribution

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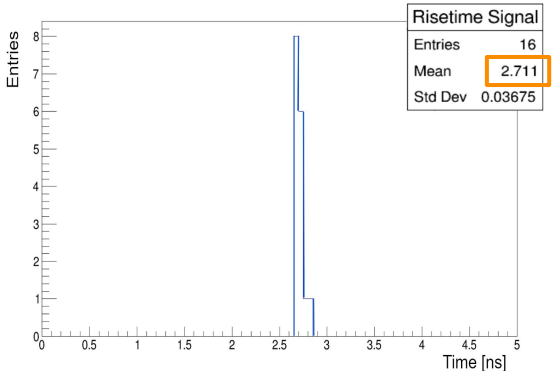

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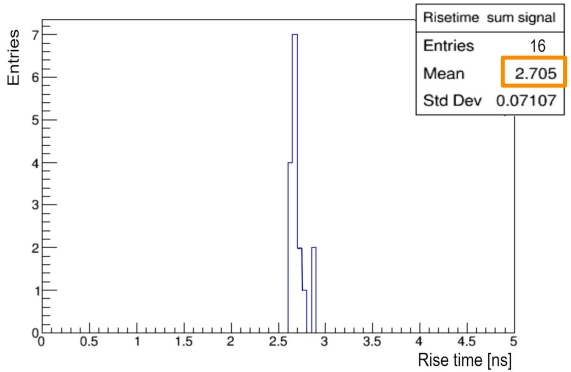

Distribution of the rise time of the analog sum for an increasing number of channels

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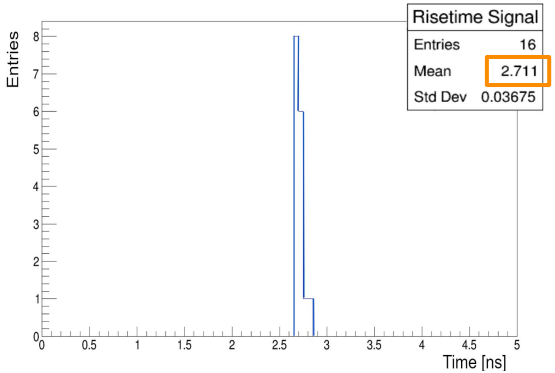
- Jitter time ~ 40 ps, good data transmission;



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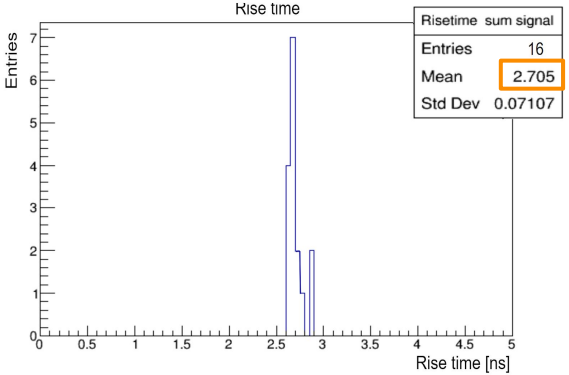

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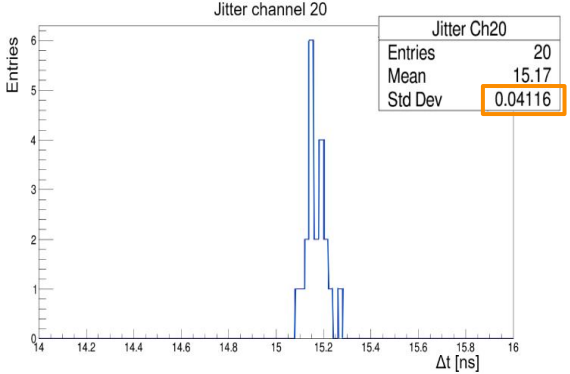
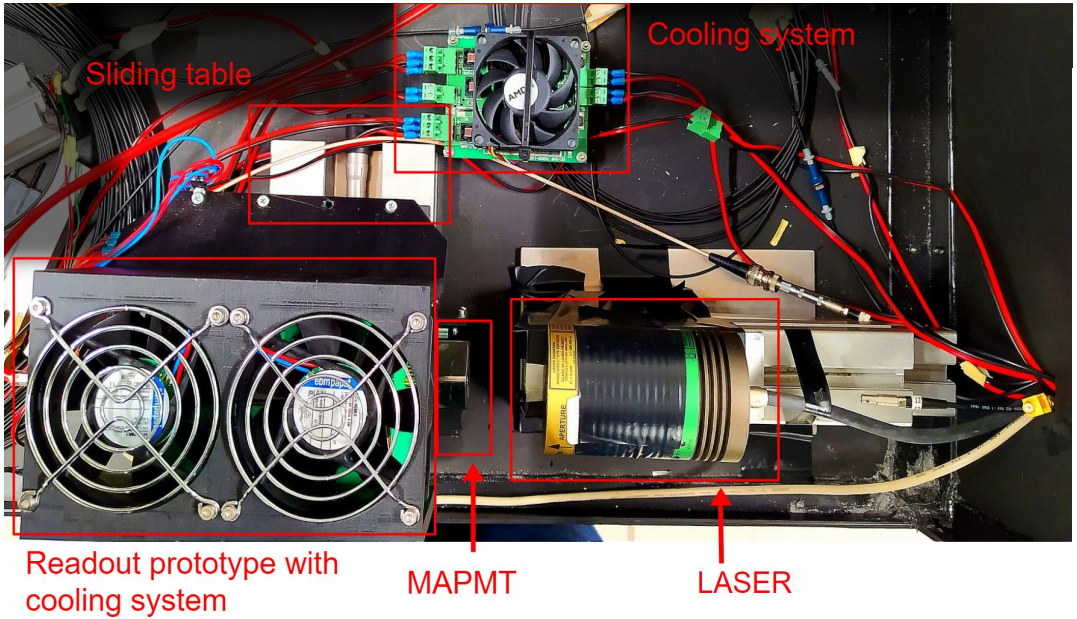
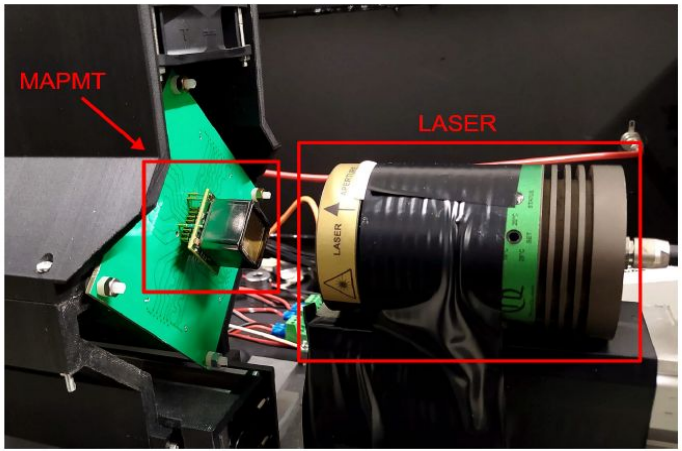


Channel 20 Δt distribution for jitter estimation

Tests with a MAPMT and a laser

- Observed coupling effects between channel testing the prototype with a MAPMT, whose channels are excited with a laser.

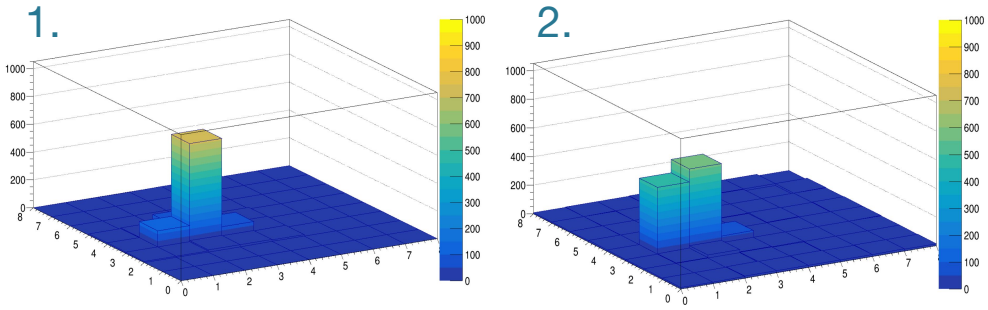


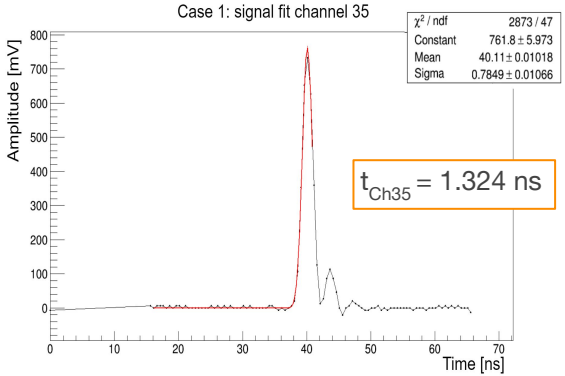


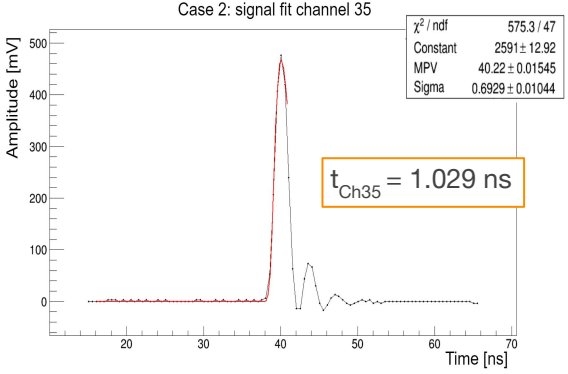
Two specific cases

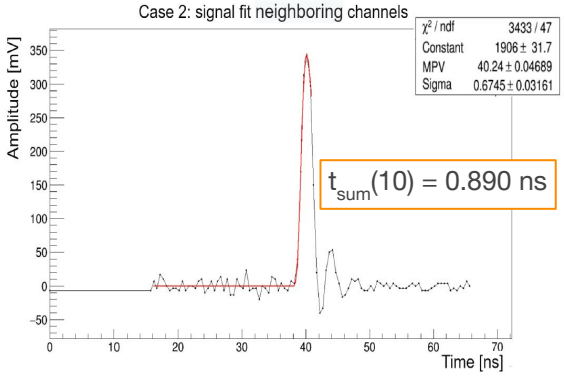
1. The laser spot is centered on a given anode pixel of the MAPMT.

2. The laser spot is almost equally shared on two adjacent channels.







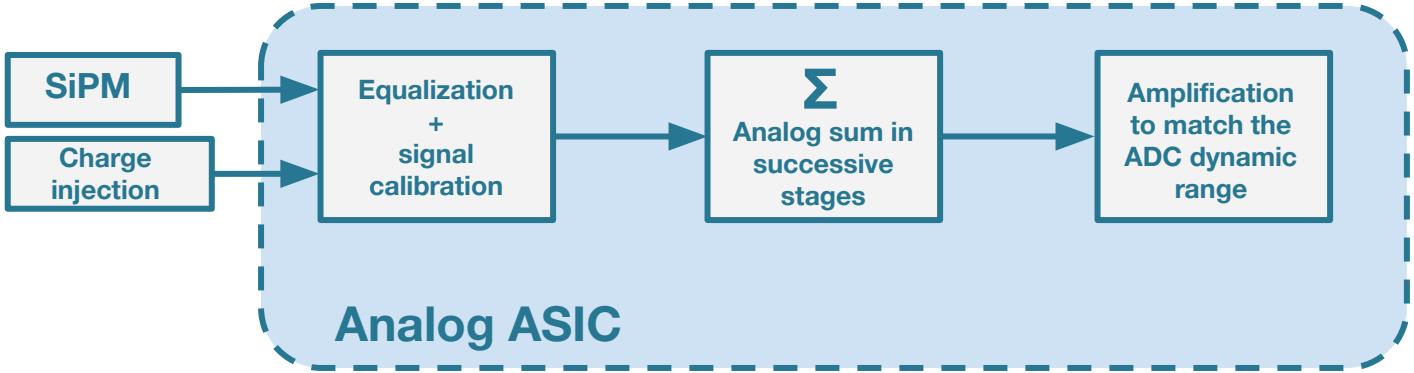


- **Observed coupling effects between channel → minimal effect that does not alter the correct functioning.**

Ongoing activities

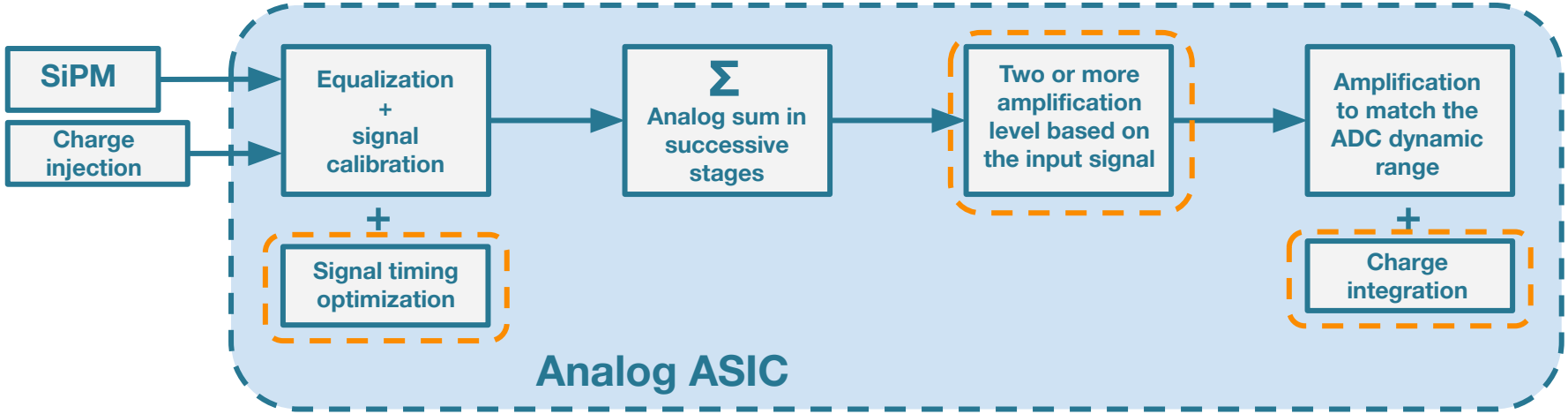
A new analog ASIC

- **The aim is to design a new ASIC device to readout multi-channel photodetectors, with the same features as the prototype, namely based on the equalization and on the analog sum of a programmable number of channels.**
- The idea is to design a first basic prototype for an ASIC 64-channels version of the device.



A versatile analog ASIC

- The basic version can be enriched with additional features to meet the needs of future users.
- For example: signal timing optimization, two amplification level and charge integration for **ALLEGRO HCAL**



Interested italian institutes

- We are working to form a collaboration of Italian institutes interested in the development of a 64-channel ASIC version of this device.
- **At this stage, we are defining the potential roles of the institutions within the collaboration and identifying the ASIC characteristics based on the readout requirements of the relevant DRD6 projects.**

Italian institutes	Field of interest
INFN Pisa	Architecture development
Università di Siena	Architecture development
INFN Torino	ASIC design
INFN Pavia	Interface to HiDRa application
INFN Milano e Università dell'Insubria	Interface to HiDRa application

➡ The table represents a possible division of tasks if the project moves forward. The institutions are already officially part of DRD6.

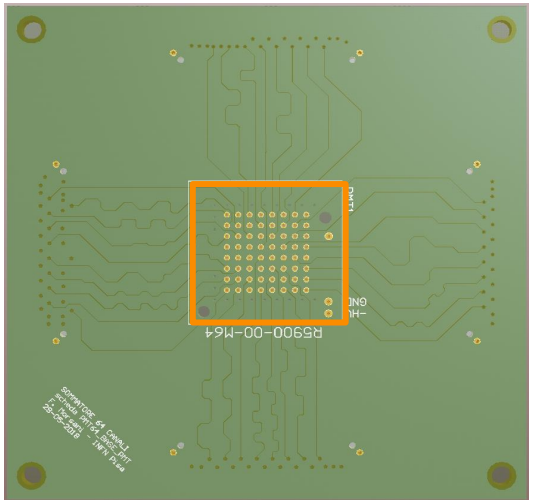
International institutes	Expertise
CERN	ALLEGRO project
Prague, Uni Bergen/ Gottingen, FOTON	SiPM readout
University of Valencia	RF amplifiers for SiPM readout

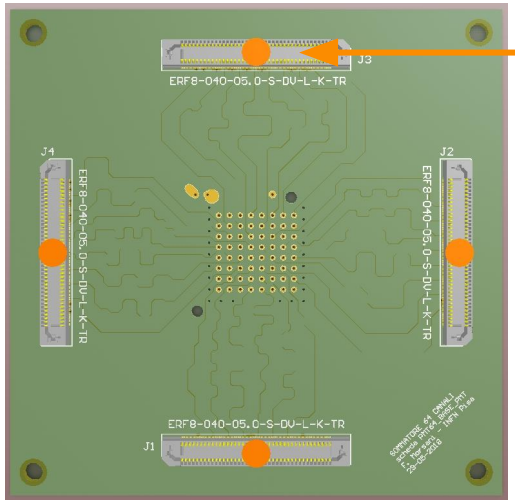
Conclusions and next steps

- A prototype of a new analog device for the readout of SiPMs has been designed and tested by INFN Pisa. The tests on the prototype yielded excellent results in terms of pulse shape stability, linearity and time stability in the case of summing an arbitrary number of channels.
- Encouraged by the results of the prototype we want to propose an ASIC with the same features for reading 64-channel SIPMs.
- To gain hands-on experience, we initiated the first tests last week focused on the readout of a single SiPM.
- **Next steps:**
  - Conduct tests on individual channels of the prototype using a single-channel SiPM (FBK);
  - Design a PCB that allows the prototype input to be adapted to a 64-channels SiPM (Hamamatsu S13361-3050AE);
  - Test the 64-channel SiPM with the prototype, also in preparation for a possible test beam in 2028, should the ASIC not be ready by then.

Backup

Prototype description (1)



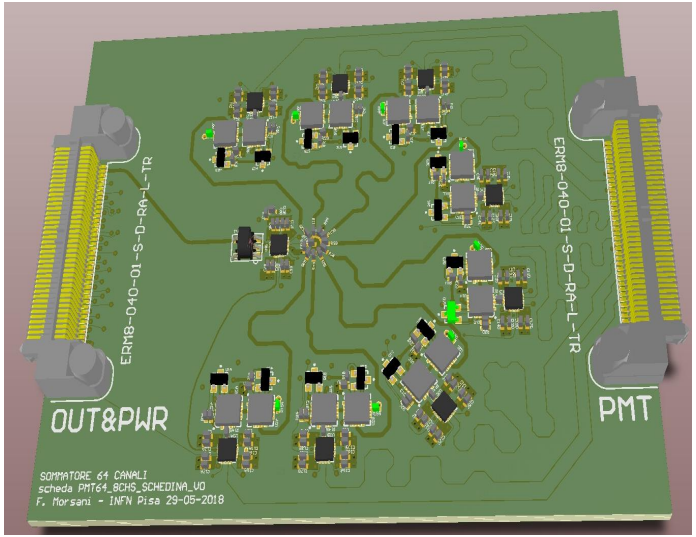


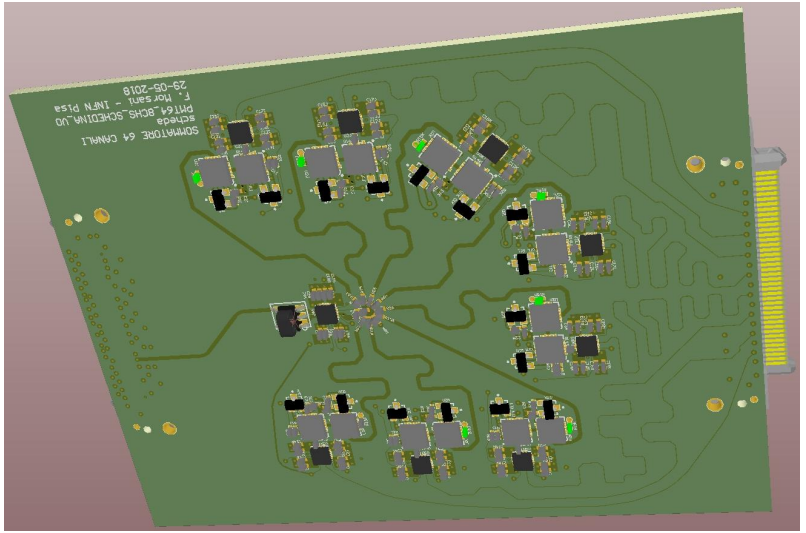
Board-to-board connector

First base board (front and back)

- The prototype is designed to host a 64-channel MAPMT with a sensitive area of 18 × 18 mm^2 and an anode pitch of 2.54 mm.

Prototype description (2)

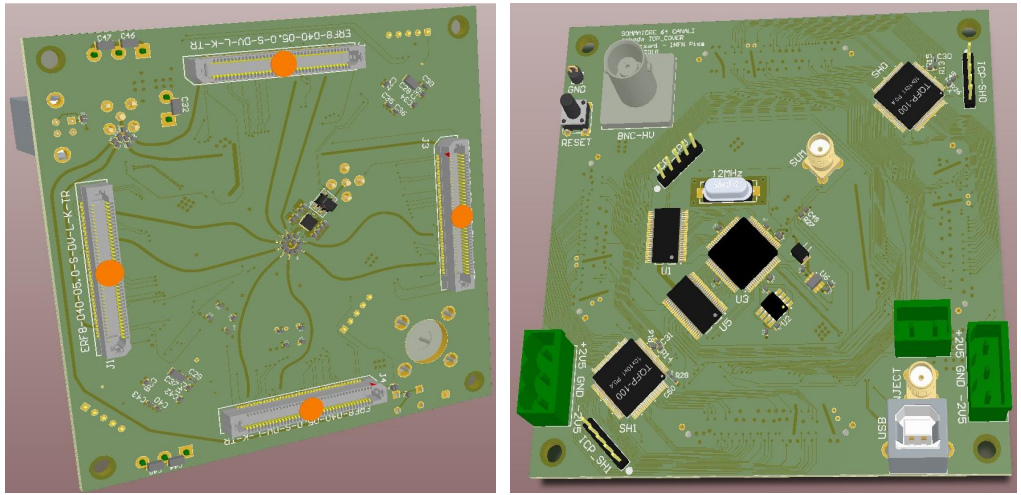




Lateral board

- 8 single-channel amplification systems
- 1 resistive network to perform analog sum of 8 channels

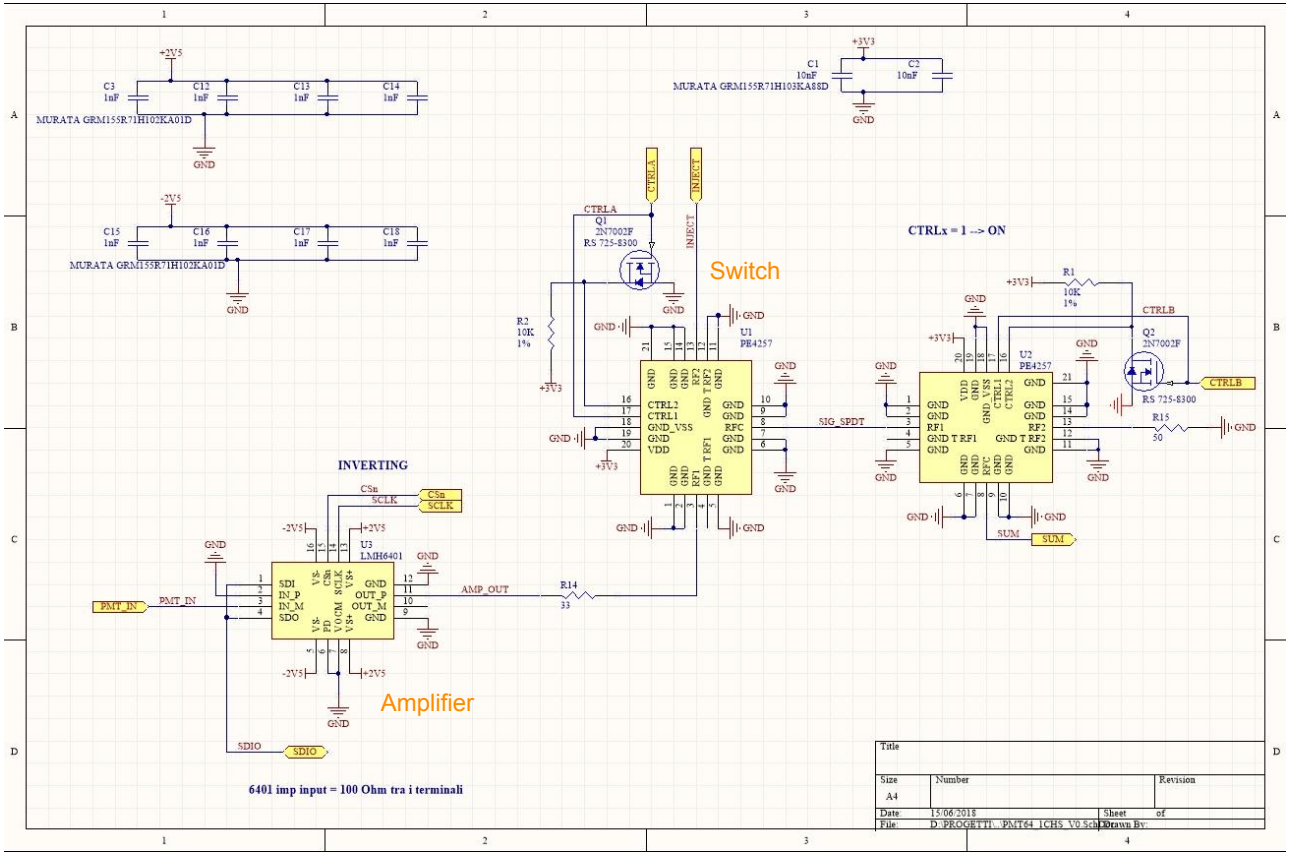
Prototype description (3)



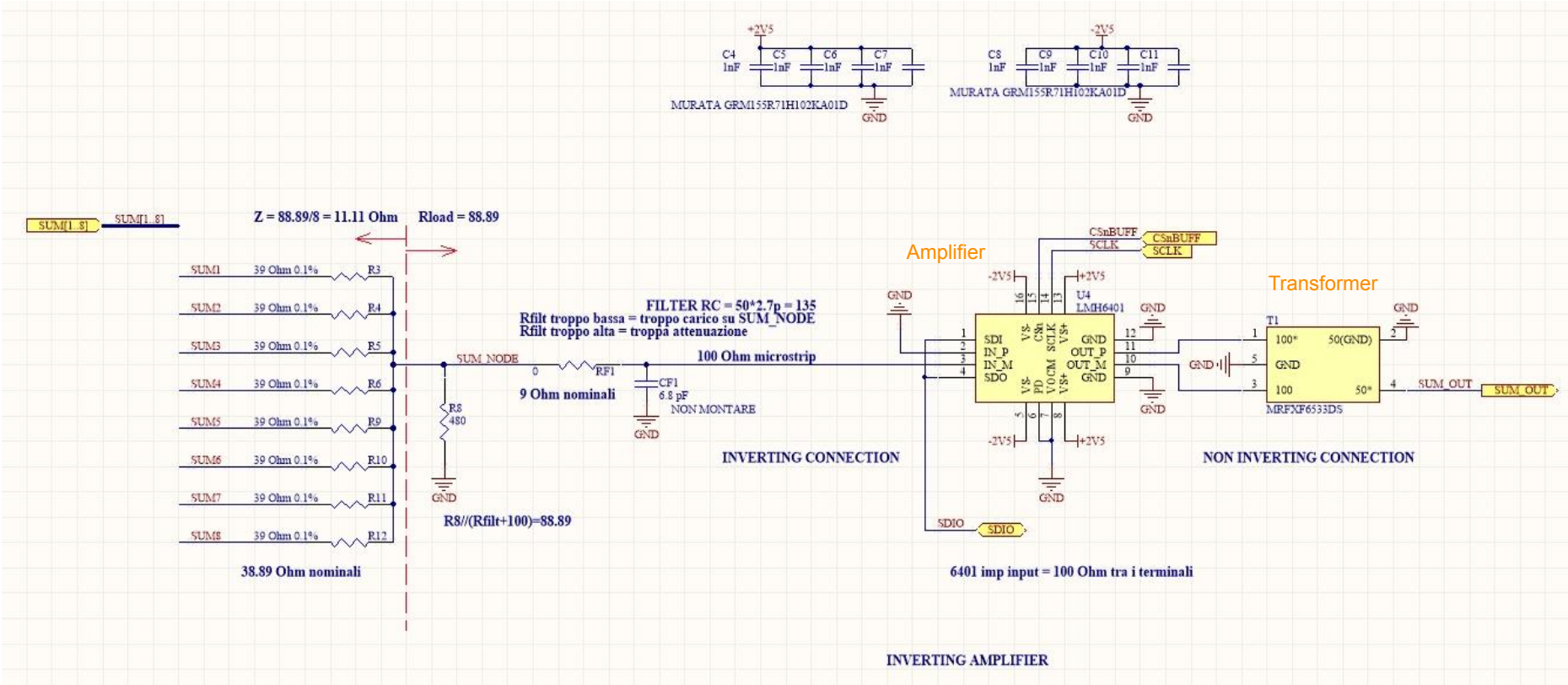
Second base board (front and back)

- Final sum stage (final resistive network + amplifier)
- Microcontroller and logic level shifters
- USB interface
- BNC-HV

Single channel amplification circuit



8-channels summing network



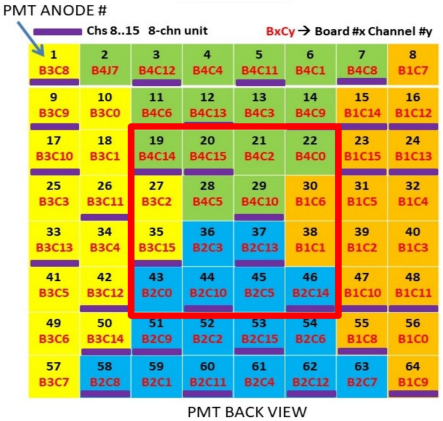
Prototype tests: introduction

- The prototype has been tested in Pisa in terms of pulse shape stability and linearity of the analog sum of an arbitrary number of channels.

- Various tests were done with two different experimental setups:

  ➡ test of the 16 central readout channels injecting an input signal

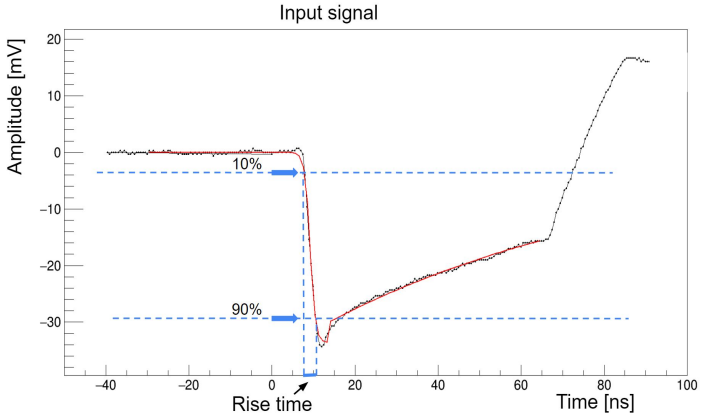
  ➡ test of the readout system using a MAPMT and a laser system



Readout prototype tests with signal injection

Input signal

- Input signal used to test the 3 readout prototype amplification stages.
- Generated by differentiating a square pulse with a 60 pF capacitor to simulate the signal produced by a PMT.



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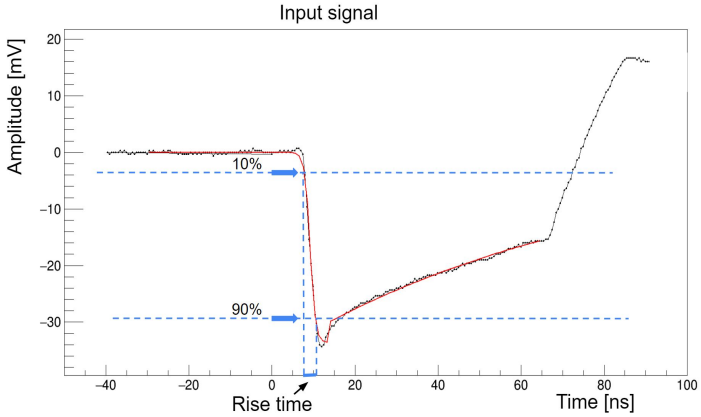
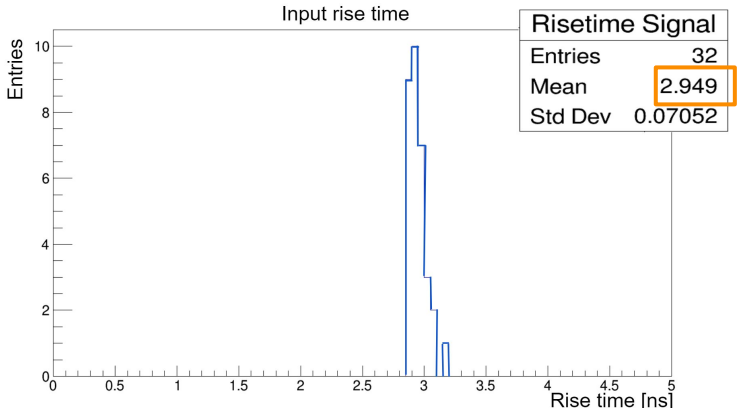
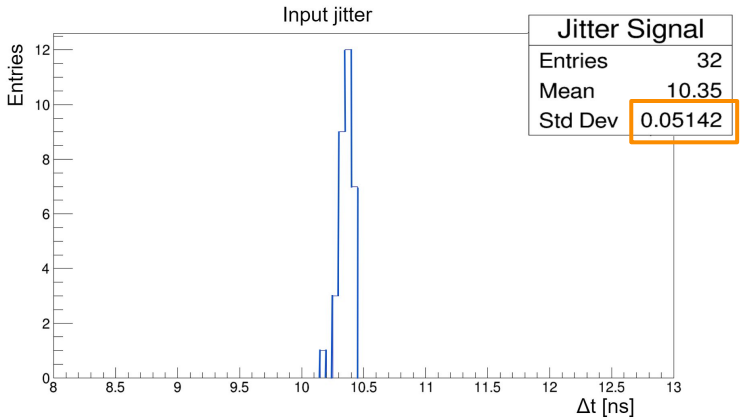
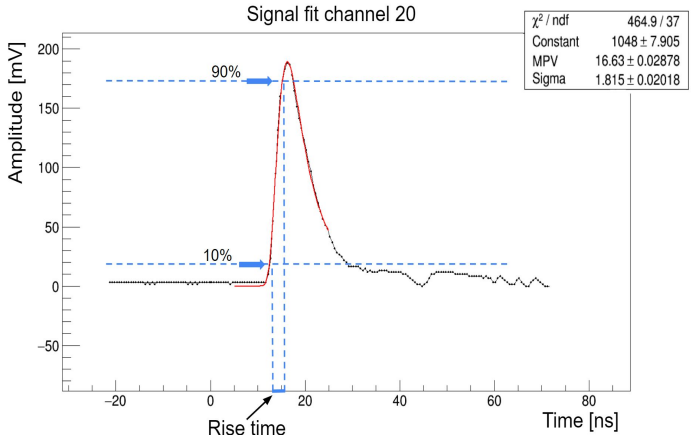




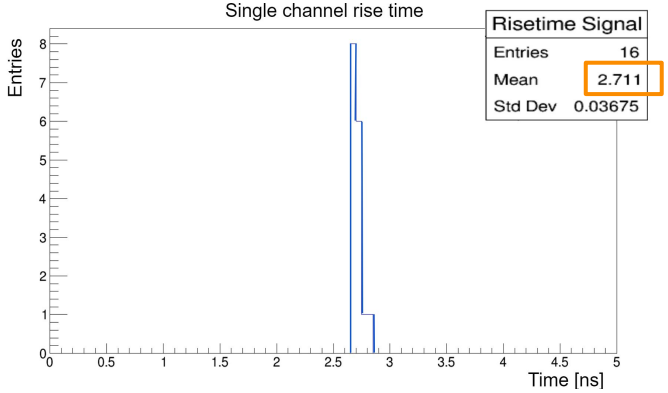


Single channel output signals: rise time

- Landau fit function to calculate the amplitude and the baseline of the signal for the rise time evaluation.

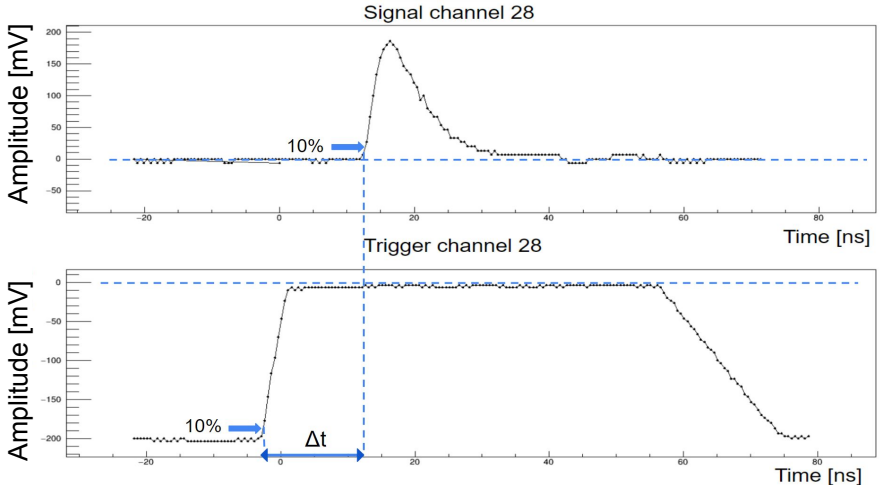


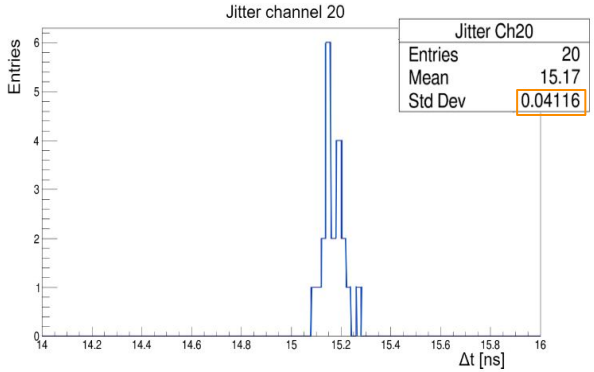
- Output signal rise times are ~ 2.7 ns.

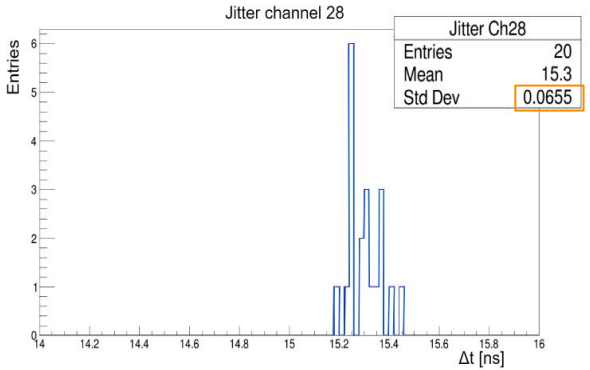


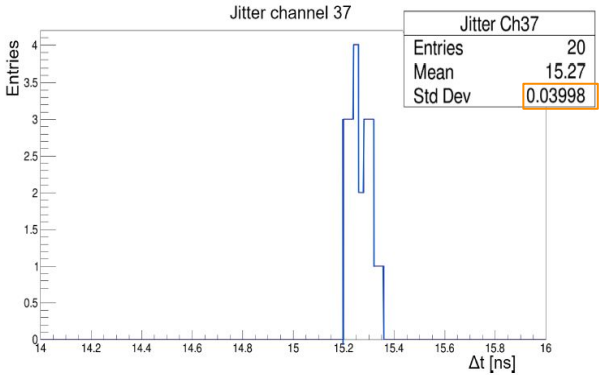
Single channel output signals: jitter time

- Jitter values ~ 50 ps.
  - ➡ Good temporal stability for this type of readout system;
  - ➡ Output jitter compatible with the input jitter ⟶ good data transmission through the readout prototype.

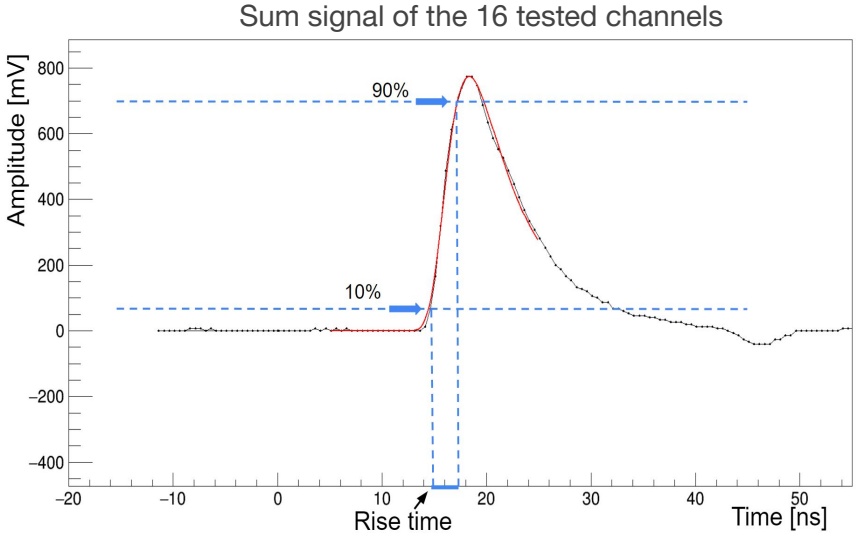


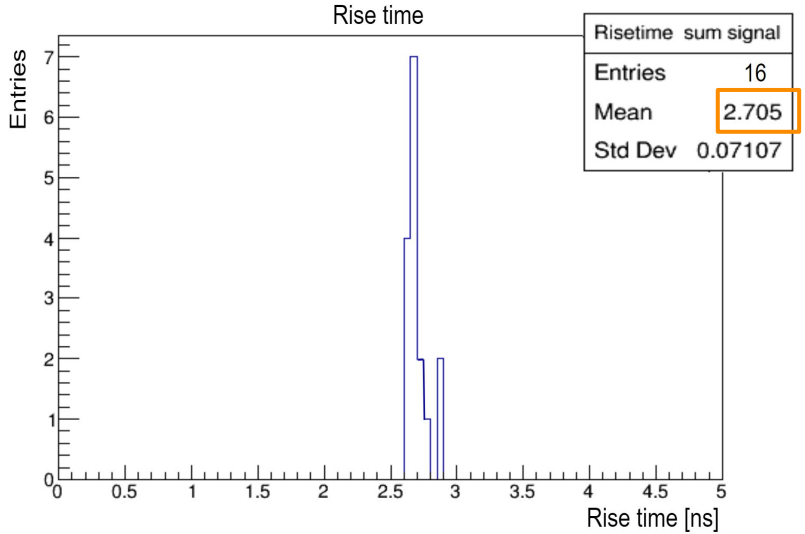






Signal stability as a function of the number of channels

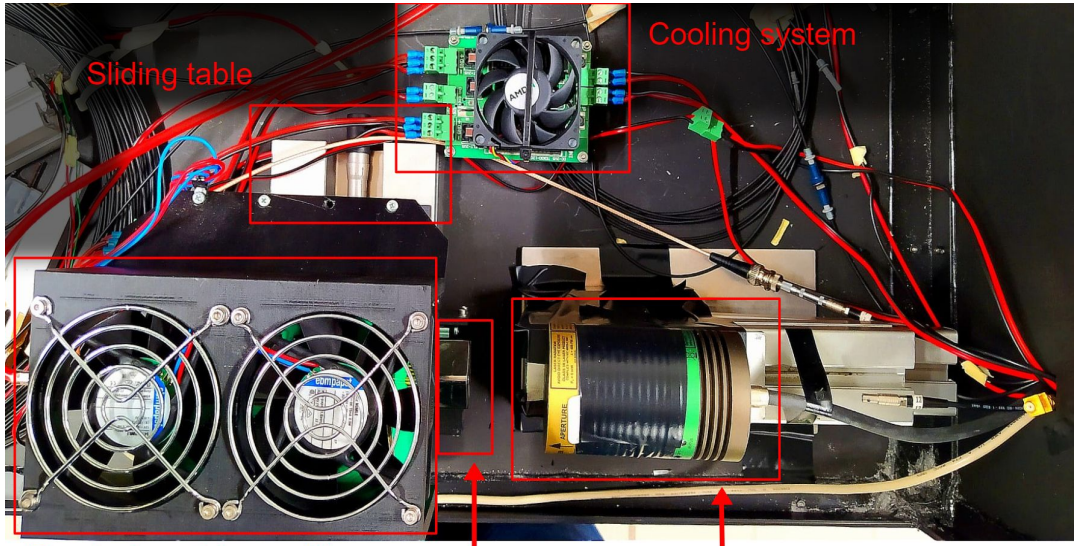


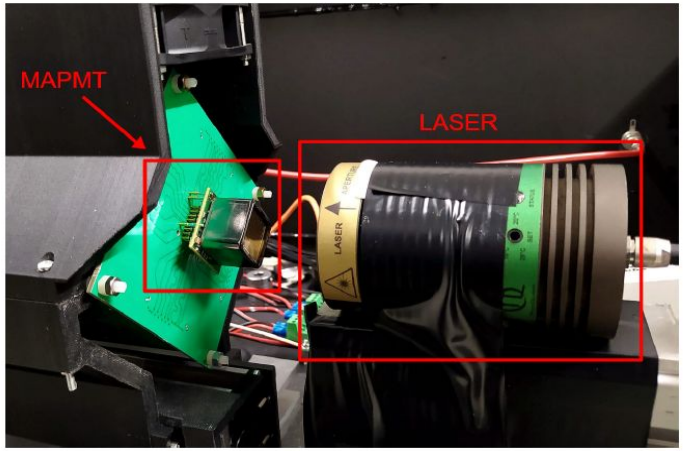


- Rise time value compatible within one standard deviation with the rise time of the individual channels.
- The operation carried out by the resistive networks to sum the analog signals does not alter the shape of the outputs.

Readout prototype tests with a MAPMT and a laser system

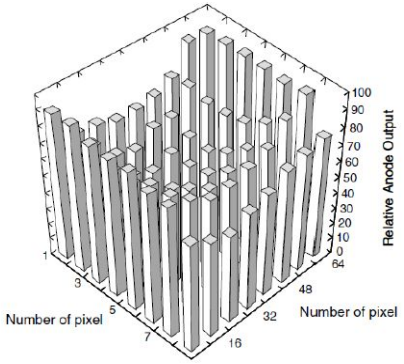
Test with MAPMT and laser: experimental setup

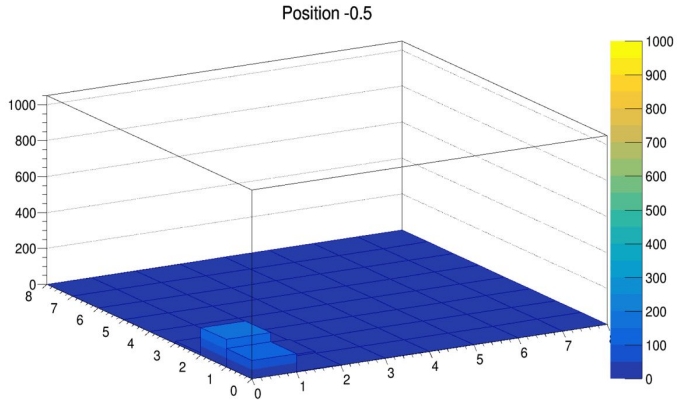


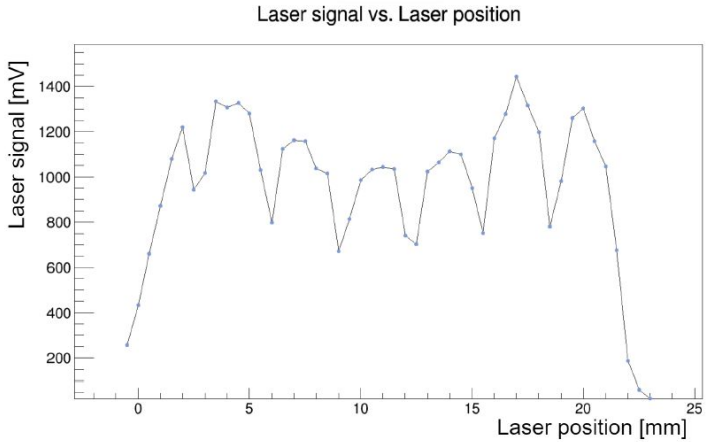


Scan of the MAPMT photocatode with a laser system

- The beam spot moves along the photocathode diagonal.
- Acquired the signal amplitudes for all 64 channels across 48 positions of the laser spot along the diagonal.
- Spot dimensions and optical crosstalk → the laser signal spreads in more than 1 channel.







Prototype tests conclusions

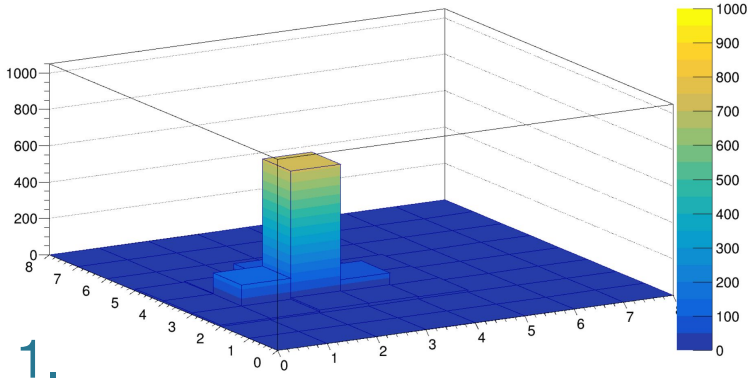
- The readout prototype guarantees shape stability, in the analog sum of the signals (rise times ~ 2.7 ns);
- The resistive summing networks do not alter the shape of the outputs;
- Jitter time ~ 51 ps, good data transmission;
- Observed coupling effects between channel → minimal effect that does not alter the correct functioning.

More information: https://etd.adm.unipi.it/t/etd-02052024-191133/

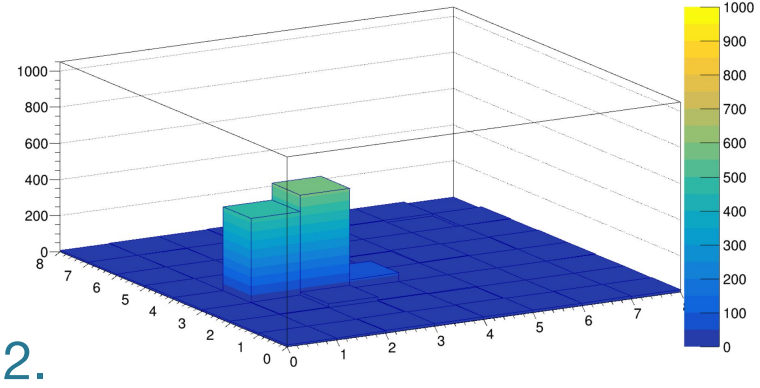
Two specific cases

1. The laser spot is centered on a given anode pixel of the MAPMT.

2. The laser spot is almost equally shared on two adjacent channels.



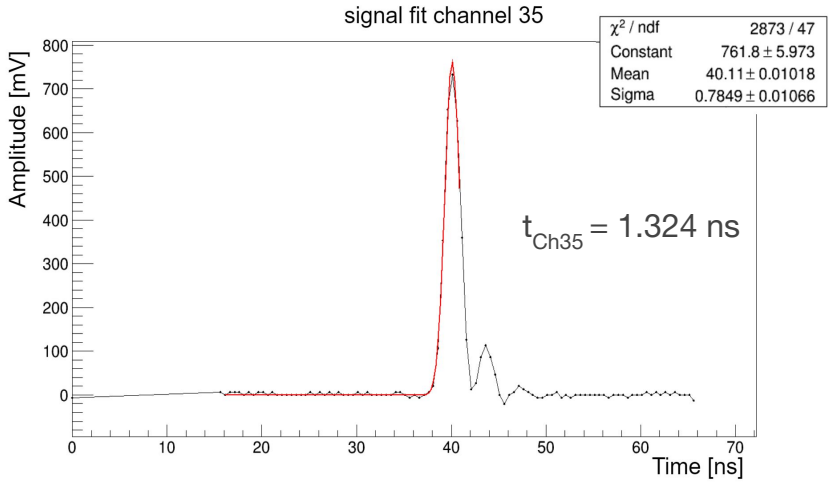
1.



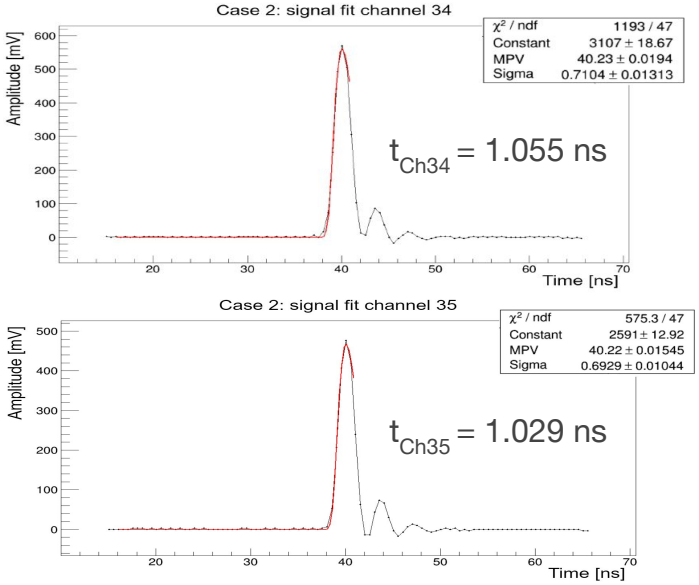
2.

Single channel signals

1.



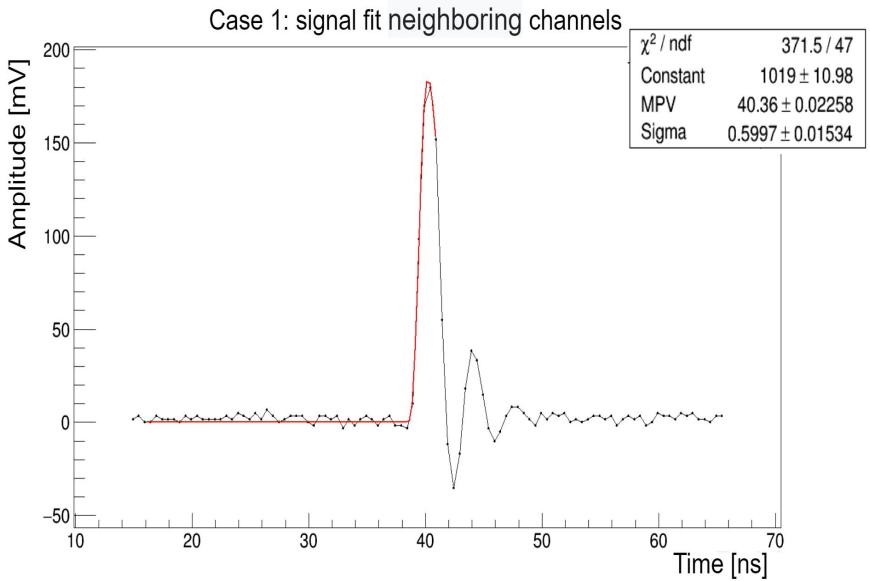
2.



The rise time of *Ch35* is larger when it alone receives the most signal relative to the case when the signal is almost equally shared between *Ch34* and *Ch35*.

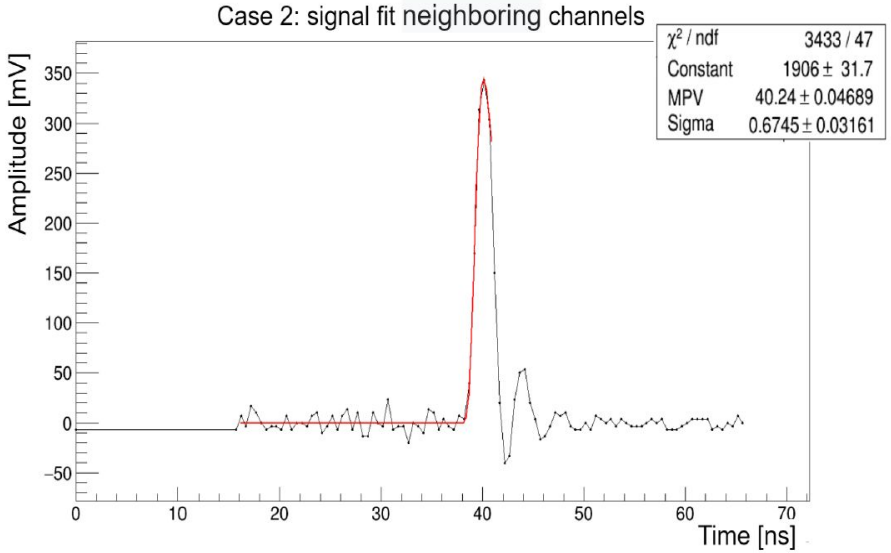
Analog sum of neighbouring channels

1.



$t_{sum}(8) = 1.002$ ns

2.



$t_{sum}(10) = 0.890$ ns

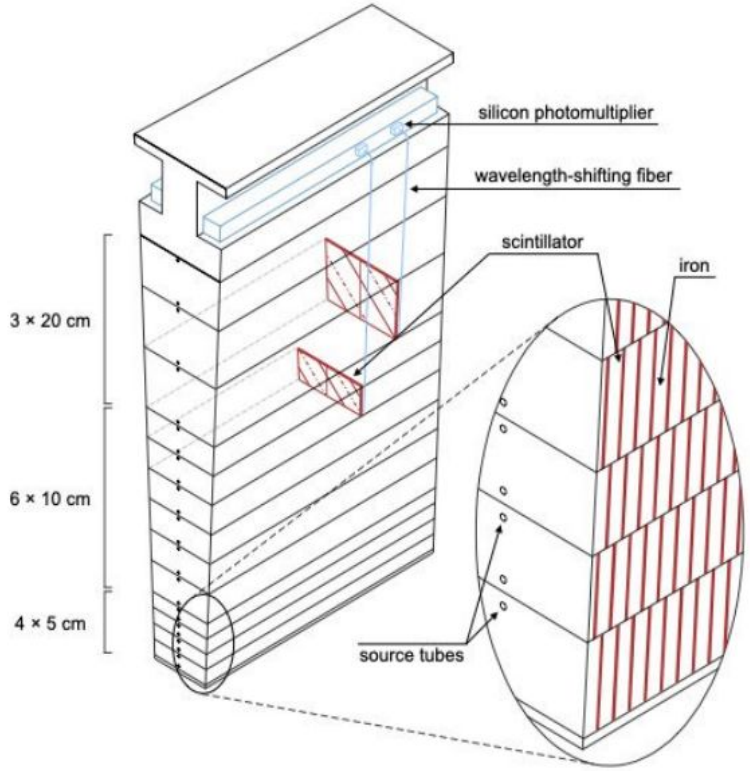
In both cases the signal rise time is larger for individual channels detecting the main part of the signal relative to the sum of the neighbouring channels.

ALLEGRO HCAL

- A possible application of this device is the ALLEGRO HCAL barrel, which involves a readout system based on **tile + fiber + SiPM**.
- Design based on alternating steel and scintillator layers (5 mm absorbers, 3 mm scintillators)

  Barrel:13 radial layers
  Endcap: 6 / 9 / 22 radial layers

- 128 modules in ϕ, 2 tiles per module
  $\Delta\phi$ = 0.025
  $\Delta\eta$= 0.022 (grouping 3-4 tiles)
- **Performance studies ongoing**
- Potential application in any calorimeter with SiPMs, which are expected to be widely used in future calorimeters.

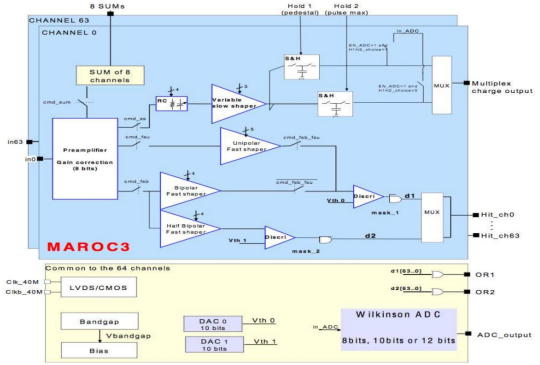


Readout systems on the market

- The device we want to design offers broader functionality than similar existing readout systems.

- **Multi-AnodeReadOut Chip (MAROC3)**

  64-channels readout, AMS SiGe 0.35 μm technology. Maximum amplification up to a factor 4.
  More info: https://www.weeroc.com/~documents/route%3A/download/132/



- **CLARO8**

  8-channels readout, 0.35 μm CMOS technology. CLARO8 provides mainly digital output signals, has only 4 gain settings and does not allow to sum the channel signals.
  More info: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7891728