RICHIESTE 2026
stato 2025

Attilio Andreazza Università di Milano and INFN

UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

Attività in corso

- Dimostratore con serial powering
  - attività in DRD7, project 7.1b,
    - solo commitment in manpower: uso di catene con rivelatori di ATLAS e RD_FCC
  - incluso in un Progetto CCF di DRD3
    - integrazione con Al PCB, ora in valutazione
    - comprende una conclusione su fondi già promessi
    - continuazione per altri due anni:
      - nuovi rivelatori + thin flexes con FBK

Dettaglio nella prossima slide

- Sviluppo rivelatori
  - richieste: test(beam) di MD3 ARCADIA con 50 um di spessore
  - interessi, ma forse prematuro per delle richieste:
    - *in DRD3 support al Progetto COFFEE in 55 nm (vertice cinese)*
    - *interesse agli sviluppi in LF 110 nm come da EOI*
    - *da valutare contributo in DRD8, microchannel cooling (manpower)*

4 kE missioni (recupero da 2025?)

Progetto DRD7

Procurements		Cost (CHF)
Al Serial Power Bus for ATLASPIX 3.1 (CERN)	**2025: 10k sj CSN1 + 10k DRD(?)**	15,000
Cu Multi Chip Module Flex LF sensors (design verification)	Coperto da IHEP	5,000
Al Multi Chip Module Flex LF sensors (FBK)	Fondi DRD3 (?) + **2026: 27.5k in conv.**	15,000
Al Serial Power Bus for LF sensors (CERN)	Fondi DRD3	15,000
DAQ Upgrades (FPGA, chip carriers and readout boards)	**2026: 4k (2 FPGA + carriers)**	15,000
Chip-to-Module assembly jigs	**2027: 5k**	2,000
Stave loading and test equipment	**2026+7: Richieste da Pisa?**	10,000
CMOS Wafers production and processing (thinning and dicing)	Fondi DRD3 *+ contributi KIT/UK*	20,000
Total project cost:		**107,000**

Nuovi sensori, richieste 2026 sj a sottomissione

Total project cost: 107,000 CHF

- DRD3 CCF contribution (13 institutes × 2650 CHF) 34,450 CHF
- RD50 CCF contribution (6 institutes × 2650 CHF) 15,900 CHF
- Funding from participating institutions 56,650 CHF

BACKUP

INFN MILANO
UNIVERSITÀ DEGLI STUDI DI MILANO
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Institutes and Contact Persons

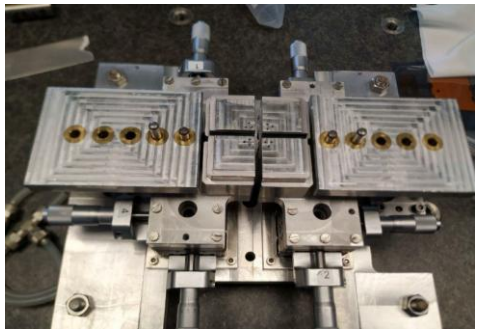
Institute	DRD3	RD50	Project contact
University of Birmingham	x	x	James Glover
University of Bristol	x		Jaap Velthuis
University of Edinburgh	x		Yanyan Gao
University of Heidelberg	x		Heiko Augustin
Hochschule RheinMain	x		Daniel Muenstermann
IHEP	x	x	Yiming Li
INFN and University of Milano	x		Attilio Andreazza
KIT	x		Ivan Peric
University of Lancaster	x	x	Harald Fox
INFN Pisa	x	x	Fabrizio Palla
FBK Trento	x	x	David Novel
TIFPA and University of Trento	x		Roberto Iuppa
INFN Torino	x	x	Stefania Beolé
Participating institutes	**13**	**6**	

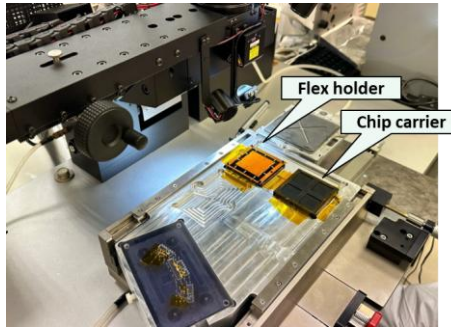
Deliverables and timelines

Deliverable	Timeline
Multi-chip module construction and readout (ATLASPix3.1)	06/2025
Al-flex production for ATLASPix3.1 power bus	09/2025
ATLASPix-based SP chain prototype construction and characterisation	03/2026
Submission and production of new CMOS sensors (LF)	07/2025-03/2026
Multi-chip readout flex submission for the LF CMOS sensors	12/2026
Multi-chip LF module construction and readout	03/2027
Al-flex production for the LF CMOS sensors	09/2027
LF sensors based SP chain prototype construction	01/2028
LF sensors based SP chain prototype evaluation	03/2028

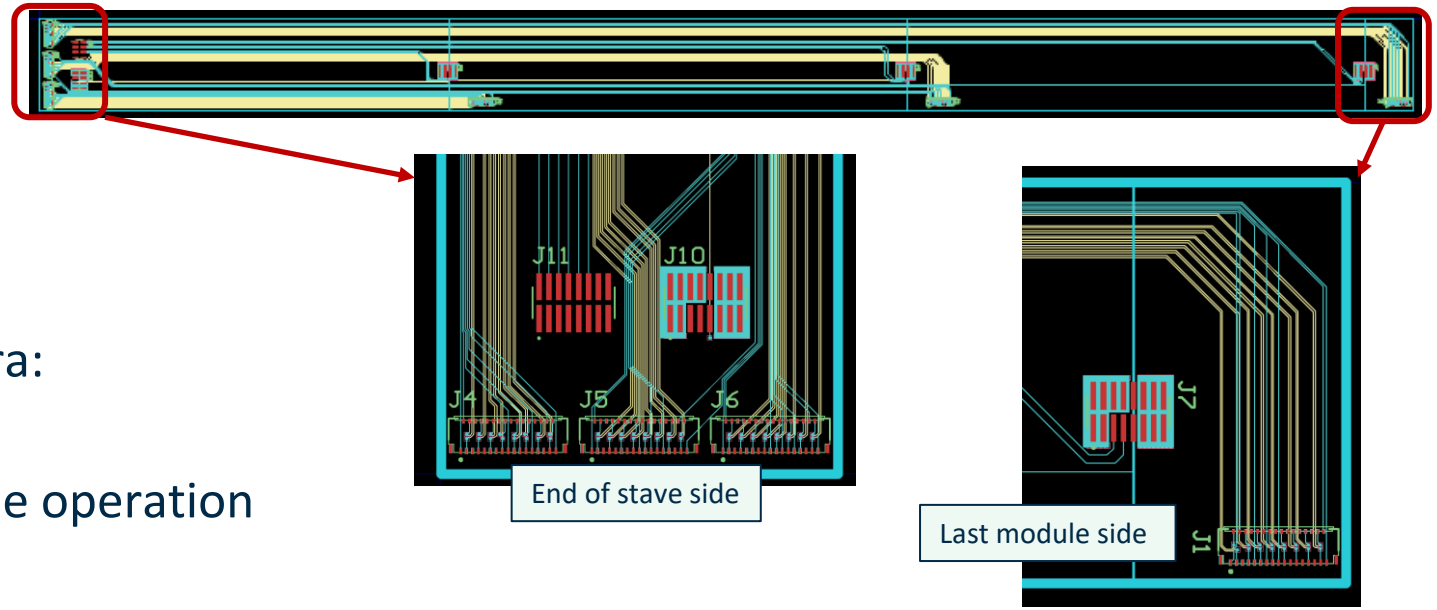
Stage 1 Completion

- Assembly modules with remaining ATLASPIX3.1 chips
  - ~6 modules with 150 μm sensors probed by Milano/Edinburgh
  - 50 μm sensors available from Heidelberg
  - Either pick-and-place or dedicated jig





- Designed a power bus to test a multi-module serial power chain
  - Aluminium conductor to reduce thickness in radiation lengths
  - Connecting to modules by pigtails
  - 4 cm × 60 cm size to match CERN Microfabrication Lab capability
  - Received quotation from Rui De Oliveira: 14,200 CHF for a panel (5-8 pieces)
  - Ready to start production, since module operation issues are solved



- Loading of cold plate (half stave with 3 modules + heaters)
  - Need tooling for loading and instrumentation for assessing thermal performance

Stage 2 planning

1. **Submission and production of LF generic R&D chips**
2. **Thinning of sensors to samples of 150 and 50 μm thickness**
3. **Design and production of multi-chip module PCB for LF sensors:**

   Requires sequential steps in understanding and verification of chip behaviour:

   1. Test of chips on single-chip-carriers, to define the operating point, minimal amount of signal, wire bonding and register configuration
   2. Copper based version, standard wire bonding, to verify the schematics and operation of the multi-chip modules
   3. Low-mass Aluminum based using FBK technology, implementing tab bonding
4. **Assembly and operation of SP chain with multi-chip modules**
   - Daisy chaining of modules through adapter cards
   - Interface to DAQ system
5. **Realization of an integrated power bus and multi-chip module PCB**
   - Major step with respect to the separate structure with power bus and module PCB as separate pieces, connected by pigtails
   - **May test some of the chip-to-flex attach technologies being developed in WG7**

Conclusions

- Future experiments will need to develop large tracking systems with **low-mass services** (both electrical and thermal) and **efficient power distribution and data handling**
- In particular there is an increase in interest in the deployment of **Aluminum conductor flexible PCB**
- This *Common Project* aims to gather groups already addressing this topic in different experiments
  - timescale for some experiments is not far away
  - prototyping solutions for system issues in parallel to sensor development
  - share information about Al flexible PCB vendors
  - stimulate the development of IP implementing features for system level integration also in the developing projects within DRD3-WP1
  - cost benefit from synergies with already running projects