

DRD3 Common Project Proposal

Date: 26/05/2025

Title of project: HV-CMOS Pixel Detector Demonstrator with Serial Powering and Innovative Interconnections

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Request to RD50: 25,000 CHF

Request to DRD3: 25,000 CHF

Total project cost: 107,000 CHF

Abstract:

This proposal (June 2025-June 2028) aims to develop a large area HV-CMOS pixel detector demonstrator for large-scale production in future Higgs factory experiments, based on multi-chip modules with data aggregation and serial powering. These multi-chip modules, including low-mass multilayer flexible PCBs, will then be integrated in staves, where modules will be powered in serial mode utilising the on-chip Shunt Low Drop Out (SDLO) regulators. Together with data aggregation, this will substantially reduce the number of stave data and power connections. Low-mass aluminium flex productions, innovative connection methods (e.g. single-point Tape Automated Bonding), low-mass mechanical support, and efficient cooling technologies will be explored for overall system optimization in power and material budget. The expertise gained by the participating institutes will be beneficial for the integration of future large scale devices that will be developed by the strategic DRD3 projects in the next few years.

Project description

Main motivation

Monolithic CMOS technology has also been widely considered in many tracking detector designs for future Higgs factory experiments (e.g. FCC-ee and CEPC) and Electron-Proton/Ion Collider (ePIC) with an active area of $O(100\text{m}^2)$. It is also chosen as the baseline for a number of middle-term tracker upgrade

projects such as ALICE ITS3, ALICE3, LHCb Upgrade II, Belle2 vertex upgrade, and mu3e phase-2 upgrade. Future Higgs factory experiments foresee an order of magnitude increase in the active area either for a full silicon tracker or for silicon wrappers around the central gas tracking chamber, compared to the current CMOS trackers. This requires a step change in the overall system design in parallel to sensor R&D, especially in power, data transmission, material budget, and integration.

Project description

This proposal will focus on efficient powering, low-mass electronics and services, as well as mechanical support and cooling for future large area monolithic pixel trackers. SP has been demonstrated successfully by the ATLAS and CMS tracker HL-LHC upgrades in hybrid pixel technologies, but has not yet been established for CMOS sensors. This project aims to provide a system level electrical and mechanical prototyping experience using full or large reticle size HV-CMOS chips equipped with on-chip SLDO voltage regulators, and explore multi-module serial powering (SP) and innovation integration techniques.

Off-chip electronics components, such as module flex PCB and data/power buses, contribute significantly to CMOS pixel detector material budget, often outweighing the contribution of active silicon elements. Copper (radiation length of 1.4 cm) is usually used in standard PCBs manufacturing. With a factor of 6 its value, Aluminum has been proposed - and used in the ALICE and mu3e experiment - as an efficient alternative to reduce material budget. However, Al-flex production processes are not yet widely available in industry, especially for those with long traces above 50 cm, or with thin lines for tab-bonding to the front-end. This proposal represents a significant step towards realizing this in large quantities required for large area application. We have identified CERN Micro Pattern Technologies Laboratory and FBK as partners in the project. The CERN Micro Pattern Technologies Laboratory has already fabricated Al flexes for ALICE, ATLAS-IBL and ILC. It also has capacity for large PCBs, up to 50 cm size. FBK has developed an in-house process for production of flexible and low-mass packaging [2]. It is limited in size of individual 15 cm wafers, but allows for tab-bonding for interconnections to ASICs and other PCBs. We also greatly benefit from the expertise and experience of other participating institutes, in particular Heidelberg and Birmingham, in related mu3e and ePIC R&D activities.

In this project we aim to produce two stages of prototypes. The initial stage is based on the available full reticle size (4 cm²) ATLASPIX3.1 (or P2Pix) sensors produced in the TSI/AMS 180 nm technology node. The second stage will use new large size sensors (2-4 cm²), to be produced by an engineering run in the LFoundry(LF) 150 nm technology node implementing a porting of the SLDO from the TSI 180 nm and potentially new features such as chip-to-chip data transfer and aggregation for large area tracking detector.

The first stage will demonstrate the operation of a CMOS based multi-chip module SP chain, verifying the chip SLDO performance in multi-chip/module setups, establishing multi-module SP chain DAQ systems, assessing the feasibility of power bus based on Aluminum conductor, and producing low mass cooling and mechanical supports. Many components for this stage are either existing or in advanced R&D stage from previous projects, such as ATLASPix3.1 based quad-chip modules with 150μm thickness being assembled by Edinburgh and Milano, a long mechanic support stage FCCee R&D from Pisa, 50μm thick ATLASPIX3.1 sensors in Heidelberg. Many participating institutes will gain valuable assembly experience in particular in handling very thin (50μm thickness) devices.

The second stage will exploit the new sensors to be submitted around September- December 2025 (led by KIT) and explore high density aluminum flex PCB production and innovative interconnections. The project benefits from nearly full in-kind contributions from participating institutes in the chip submission. DAQ systems of the participant institutes will also be upgraded accordingly.

Critical tasks and milestones

Stage 1:

1. Production on an Aluminium based power bus for SP
2. Thermal characterization of a long stave support
3. Loading and operation of a serial power chain of multi-chip modules (150 μ m thick sensors) with sensor on the long stave
4. Assembly of multi-chip modules with 50 μ m thick sensors

Stage 2:

1. Submission and production of LF generic R&D chips
2. Thinning of sensors to samples of 150 and 50 μ m thickness
3. Design and production of multi-chip module PCB for LF sensors:
 - a. Copper based version to verify the schematics and operation of the chip
 - b. Low-mass Aluminium based using FBK technology, implementing tab bonding
4. Assembly and operation of SP chain with multi-chip modules with the above mentioned PCB
5. Realization of an integrated power bus and multi-chip module PCB

Timescale:

Multi-chip module construction readout (ATLASPix3.1): June 2025

Al-flex production for ATLASPix3.1 power bus: September 2025

ATLASPix-based SP chain prototype construction and characterisation: March 2026

Submission and production of new CMOS sensors: July 2025 - March 2026

Multi-chip readout flex submission for the new CMOS sensor: December 2026

Multi-chip module construction and readout: March 2027

Second Al-flex production for the new CMOS sensors: September 2027

LF sensors based SP chain prototype construction: January 2028

LF sensors based SP chain prototype evaluation: March 2028

Project costs, contributions from participating institutes and request to the DRD3 common fund:

Project Costs:

We request funding, with substantial in-kind contributions from participating institutes, in productions of Aluminum flex PCBs for multi-chip module assembly and SP operation, procurement of wafers (including thinning and dicing) for new sensors with SLDO, DAQ systems updates (e.g. FPGAs, chip carrier PCB productions), and productions of low-mass supporting and cooling structure productions

PCB productions (total 50k CHF)

AI Serial Power Bus for ATLASPIX 3.1 (CERN)	1 production (~5 boards)	15000 CHF
AI Multi Chip Module Flex LF sensors (FBK)	1 production	15000 CHF
Cu Multi Chip Module Flex LF sensors (design verification)	1 productions	5000 CHF
Serial Power Bus for LF sensors (CERN)	1 production (~5 boards)	15000 CHF

DAQ upgrades (total 15k CHF)

FPGAs, chip carrier and readout boards	5-10 sets	15000 CHF
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Mechanics (total 22k CHF)

Chip-to-flex assembly jigs	~5 sets	2000 CHF
CF-based mechanic support	2 sets	20000 CHF

Wafer production and post-processing (20k CHF)

CMOS wafer productions and processing	~5 wafers	20000 CHF
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Total	107,000 CHF
Request to DRD3/CFF contribution:	50,000 CHF
Contributions from participating institutes:	57,000 CHF

In summary, this project focuses primarily at the system level prototyping for future Higgs factory tracking detectors based on HV-CMOS sensors. The technologies explored have a strong synergy with on-going R&D in a number of middle-term upgrades projects in the timescale of the 2030s. This proposal provides a common framework that enables groups with common interests and backgrounds in various experiments to share their experiences and resources within the DRD3 Collaboration. It also serves as a basis for the thesis work of a number of post-graduate students (master, PhD) and publications.

References

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2. D. Novel, A. Lega, T. Facchinelli, R. Iuppa, S. Beol , P. Bellutti, “Evolution of flexible PCBs in particle detection: From ALICE ITS1 to future frontiers in microfabrication for ALPIDE chip integration”, <https://doi.org/10.1016/j.nima.2024.169840>