HV-CMOS Pixel Detector Demonstrator with Serial Powering and Innovative Interconnections

3rd DRD3 Week on Solid State Detectors R&D
Amsterdam, 2-6 June 2025

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CCF Project Proposal by

Birmingham, Bristol, Edinburgh, FBK, Heidelberg, Hochschule RheinMain, IHEP, KIT, Lancaster, Milano, Pisa, Torino, Trento

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Project proposal

- This proposal aims to develop a **large area HV-CMOS pixel detector demonstrator** for large-scale production in **future Higgs factory** experiments, based on **multi-chip modules** with **data aggregation** and **serial powering**.
- These multi-chip modules, including **low-mass multilayer flexible PCBs**, will then be integrated in staves, where modules will be powered in serial mode utilising the on-chip Shunt Low Drop Out (SDLO) regulators. Together with data aggregation, this will substantially **reduce the number of stave data and power connections**.
- **Low-mass aluminium flex productions**, innovative connection methods (e.g. single-point Tape Automated Bonding), **low-mass mechanical support**, and **efficient cooling technologies** will be explored for overall system optimization in power and material budget.
- *The expertise gained by the participating institutes will be beneficial for the integration of future full-size devices that will be developed by the strategic DRD3 projects in the next few years*

Available for comment in DRD3 CDS Repository: CERN-DRD3-PROJECT-2025-014

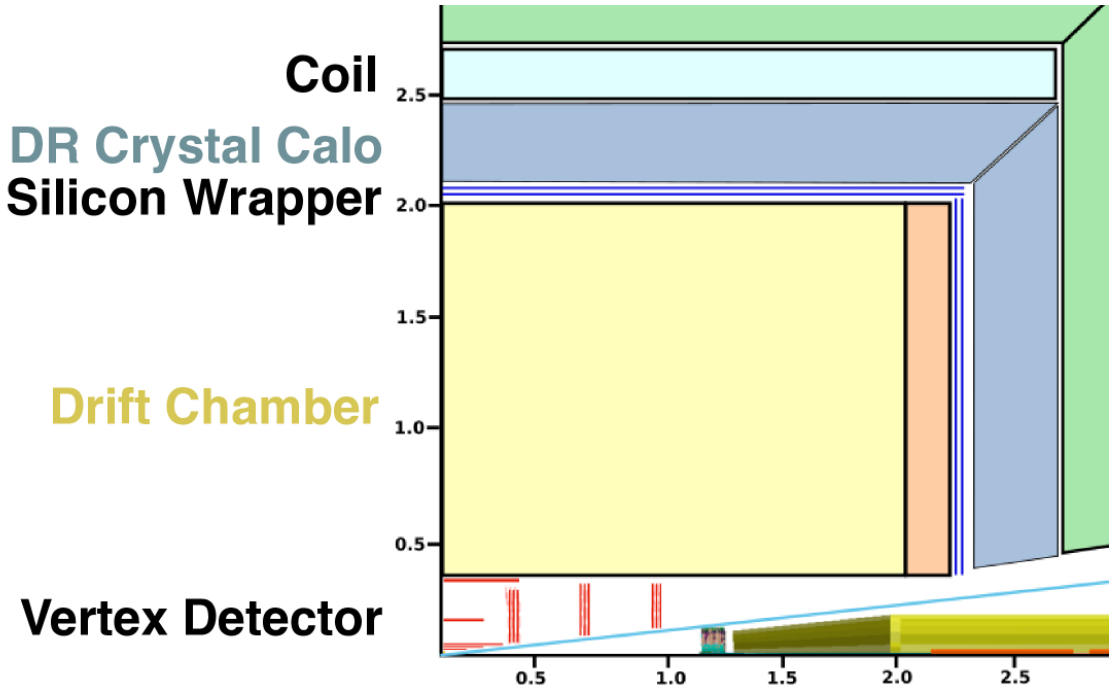
Institutes and Contact Persons

Institute	DRD3	RD50	Project contact
University of Birmingham	x	x	James Glover
University of Bristol	x		Jaap Velthuis
University of Edinburgh	x		Yanyan Gao
University of Heidelberg	x		Heiko Augustin
Hochschule RheinMain	x		Daniel Muenstermann
IHEP	x	x	Yiming Li
INFN and University of Milano	x		Attilio Andreazza
KIT	x		Ivan Peric
University of Lancaster	x	x	Harald Fox
INFN Pisa	x	x	Fabrizio Palla
FBK Trento	x	x	David Novel
TIFPA and University of Trento	x		Roberto Iuppa
INFN Torino	x	x	Stefania Beolé
Participating institutes	**13**	**6**	

Project Proposal

- The project idea was already presented at:
  - 1st DRD3 week:
    Large area low-power Monolithic CMOS Tracking Detectors for future particle physics experiments
  - 28/10/2024 WG1 meeting:
    HV-CMOS Multi-chip integration for large area silicon tracker
- Given the amount of resources involved and the very specific topics, moved from a strategic *work package project* to a *common fund project*
- Since October:
  - enlarged the collaboration with other groups already involved in the development of low-mass flexible PCB
  - new results from the preliminary stage of the process
  - defined scope and roadmap
- Project proposal submitted to WG1 Conveners and the Spokesperson

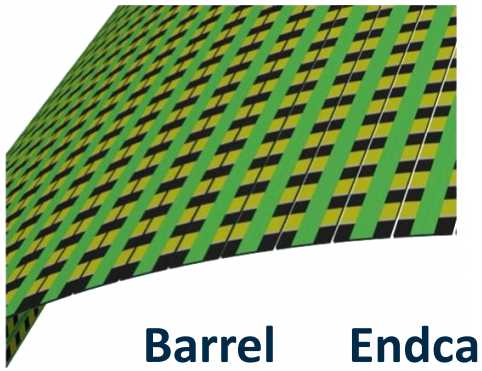
Project motivation: Higgs Factories



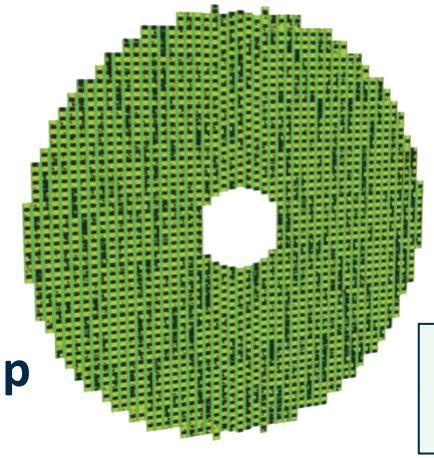
Silicon tracking in different regions

(IDEA concept shown here, but general considerations are valid for all layouts)

- **inner vertex detector (R=1.4-3.3 cm)**
  - **3-5 μm resolution, O(200 MHz/cm^2), very low material**
- **outer vertex detector (R=13-31 cm)**
  - **~7 μm resolution, 27 ns timestamp, O(40 kHz/cm^2)**
  - **material is a concern**
- **silicon wrapper/TOF (R/z = 200 cm)**
  - **~7 μm resolution, 27 ns timestamp**
  - **100 m^2 (2 layers): ~2.5 10^5 chips, ~100 kW power**

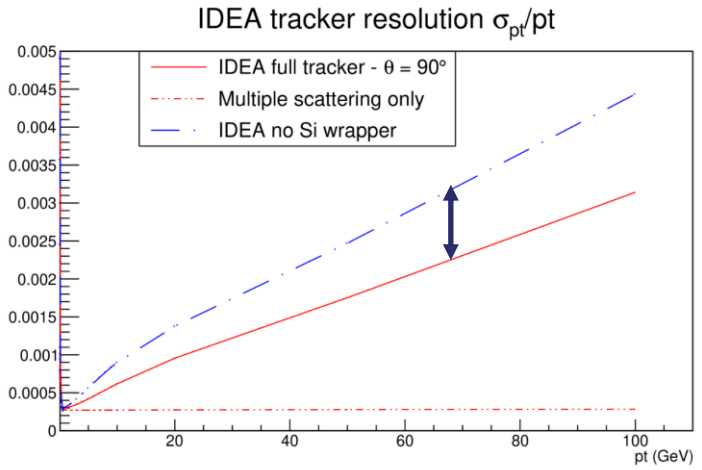


Barrel



Endcap

The IDEA detector concept for FCC-ee arXiv:2502.21223



Project motivation: service integration

Distribution of power and data signals along the local supports

- **serial powering** to reduce dissipation on the distribution lines
- **minimize** the number of connections

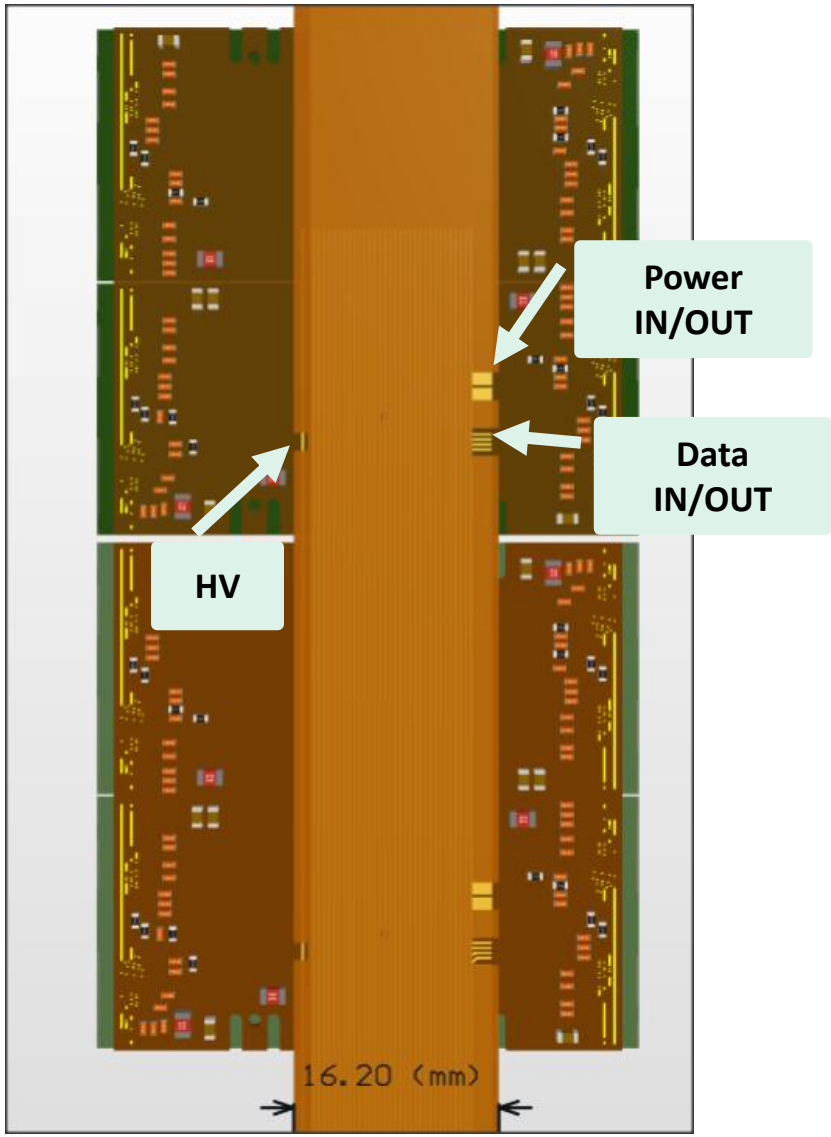
Read-out units are:

- **multi-chip modules** (example 2x2 quad modules)
- (or large stitched detectors)

Minimal I/O connection on chip requires:

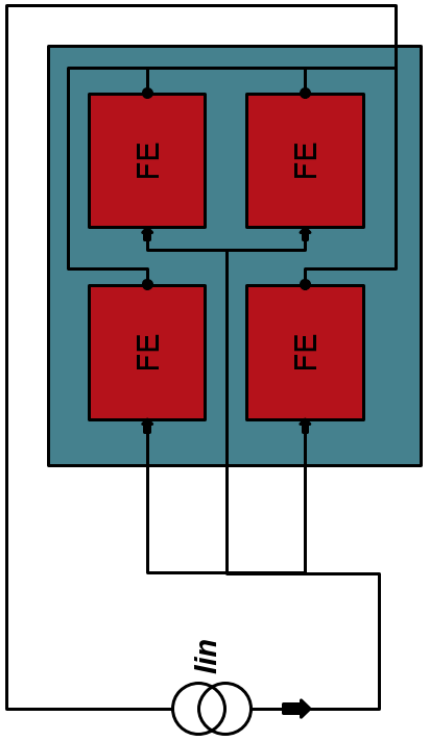
- Serial powering chain: all biases generated internally by shunt-LDO regulators
  - 1 LV and 1 HV line per "stave"
- chip-to-chip data transmissions: local data aggregation on module
  - 1 data-out per "module"
- LVDS module configuration with clock data recovery
  - 1 data-in per module
- **No current detector providing all these features**

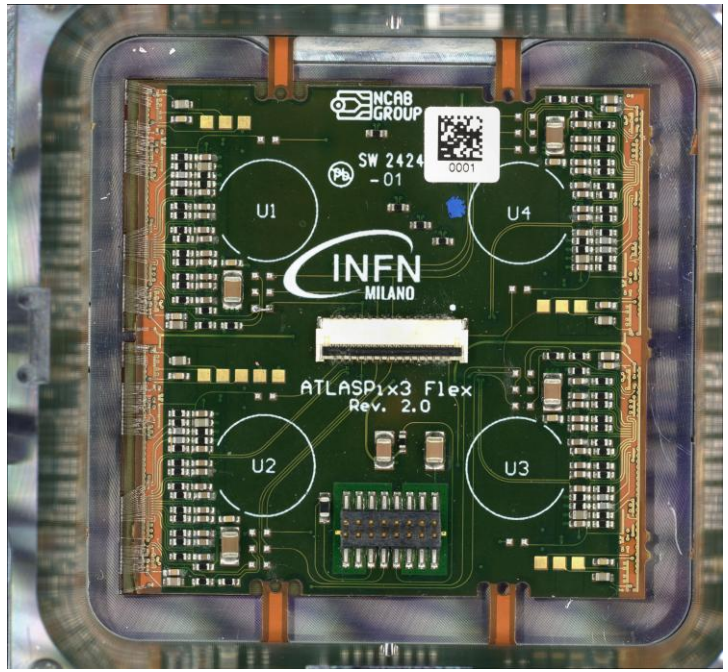
Reducing material by developing PCB with Al as conductor

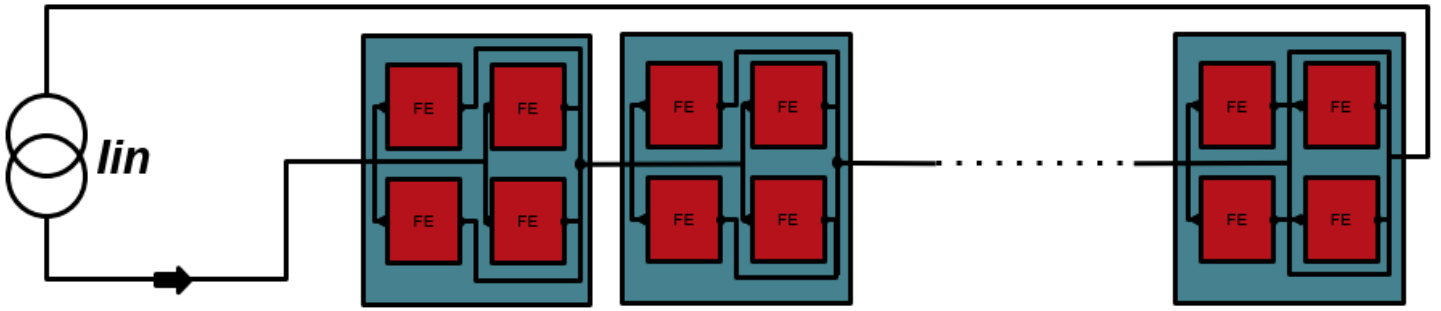


CMOS modules (1)

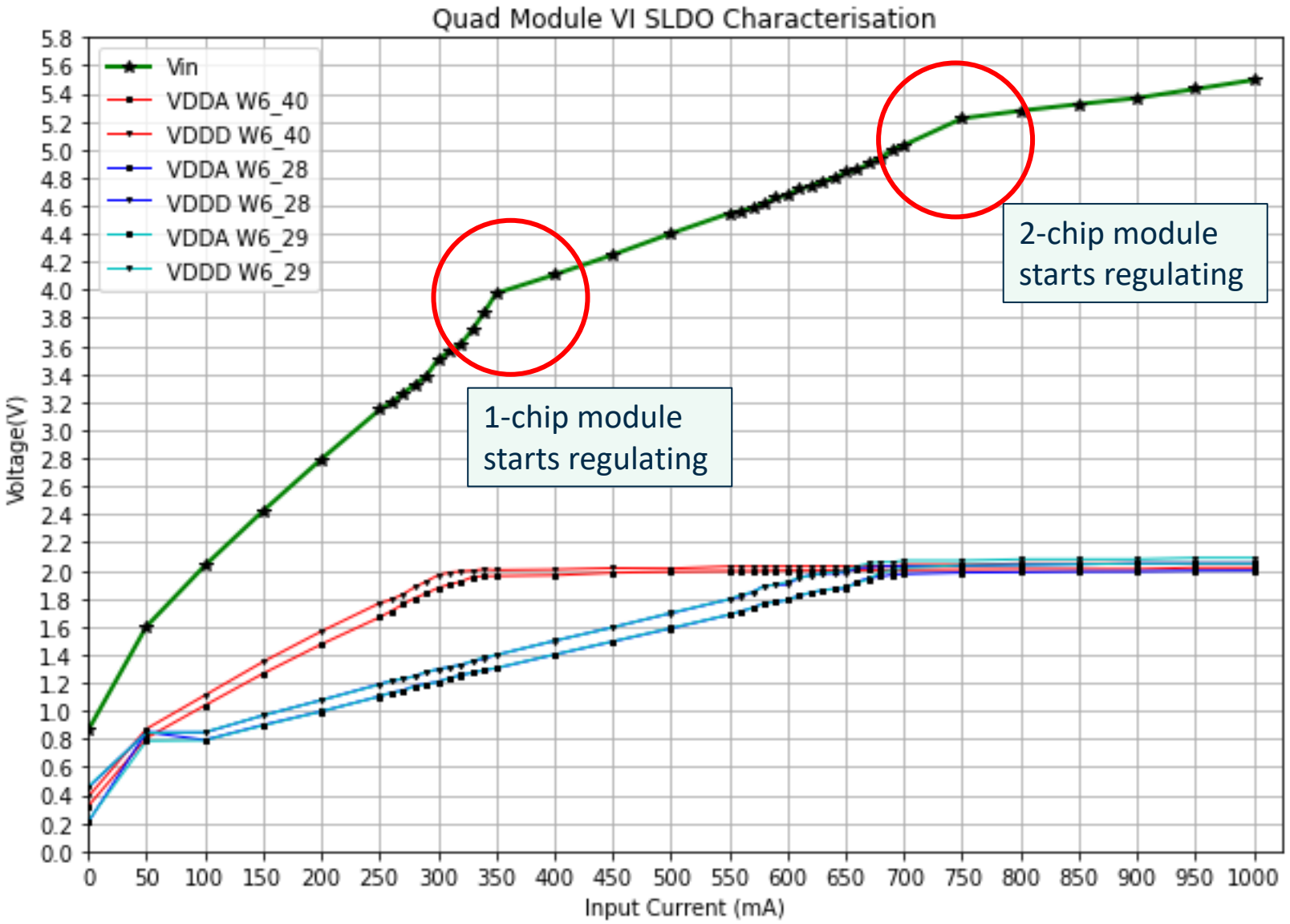
- Prototyping with ATLASPIX3.1 sensors
  - TSI 180 nm CMOS process
  - Almost full-reticle size 2 × 2 cm^2
  - 150 mW/cm^2
- Multi-chip modules
  - Single LV and HV bias line
  - Common data-in LVDS lines: command, clock, synch, trigger
  - Individual modules data-out LVDS lines
  - AC coupling to DAQ
- Possible to build a serial powering chain
- Probing of SLDO operation before assembling

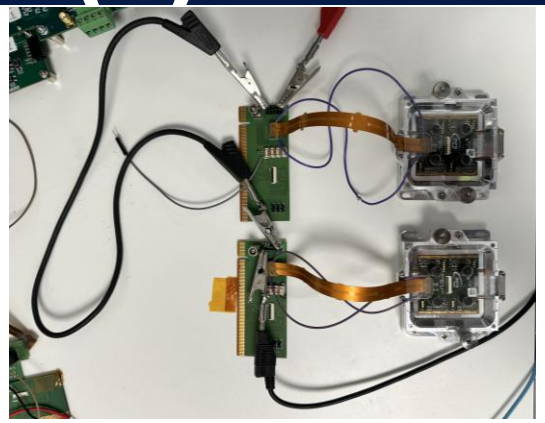






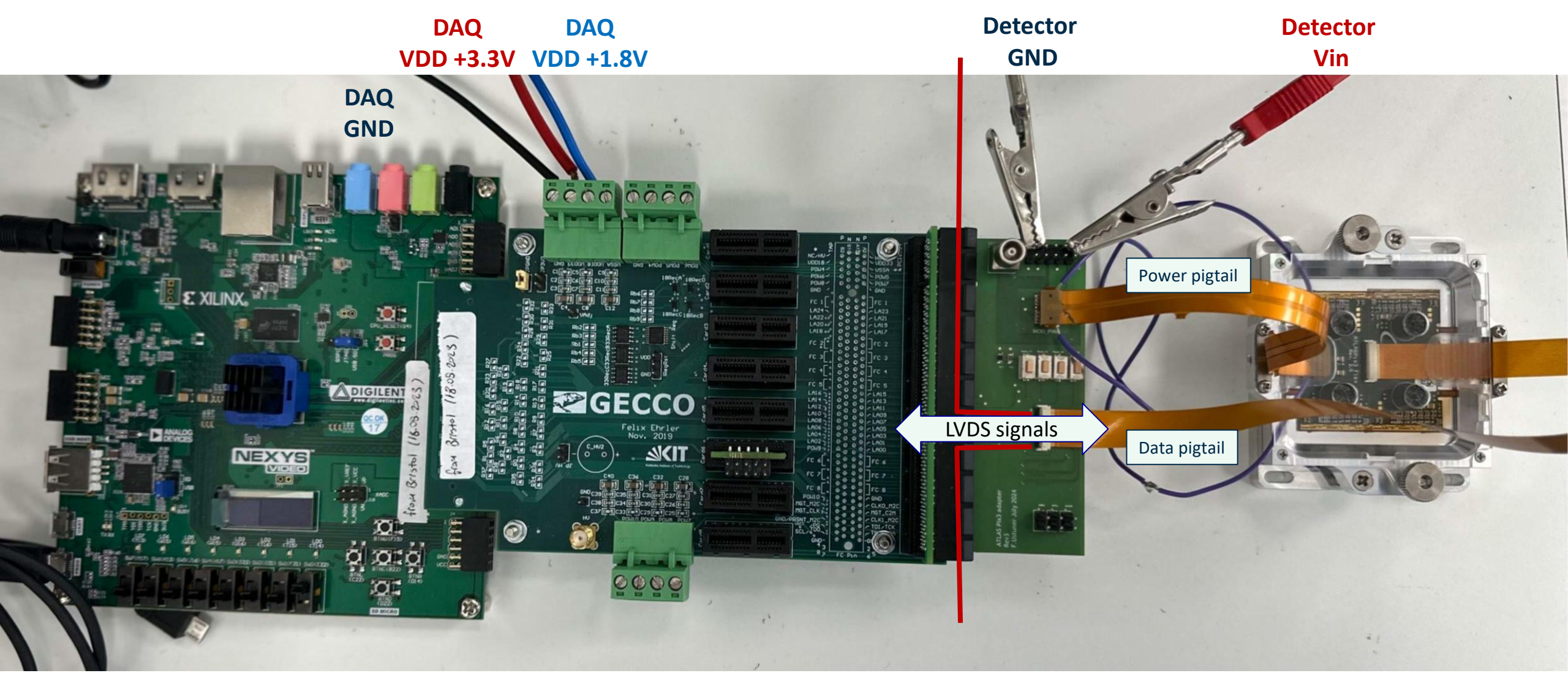
CMOS modules (2)





- The serial powering chain for two modules
  - "test modules" with 1 and 2 chips respectively
- Each module has an individual regulation process
  - **1-chip module**
    - VDDD/A = 1.99/1.97 V
    - @ 350 mA
  - **2-chip module**
    - VDDD/A = 2.04/2.00 V
    - @ 700 mA

Module testing setup



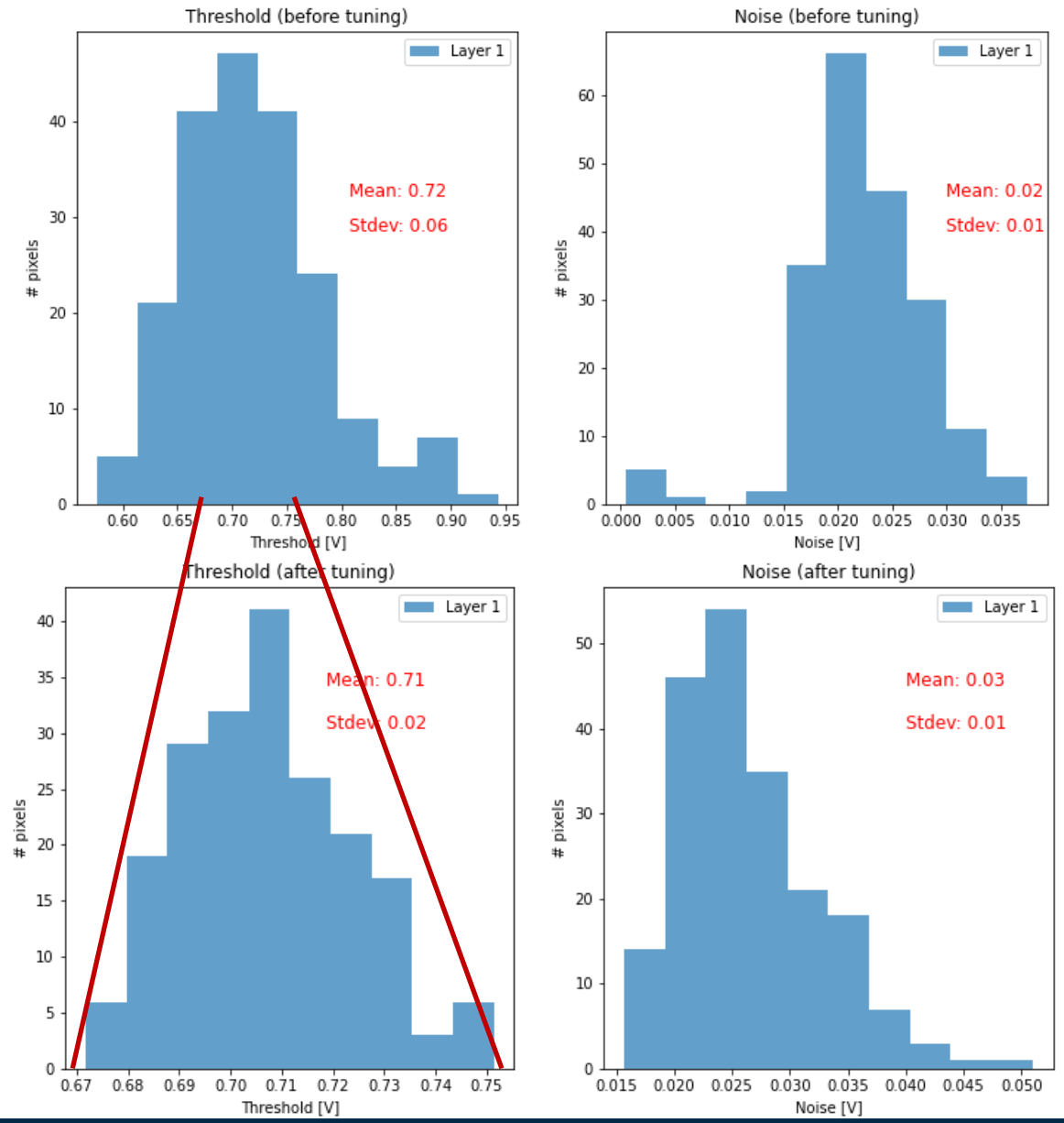
- GECCO, flexible readout system developed by KIT
- Firmware and sofware adapted to module operation
- Adapter card splitting the two power domains
- LVDS signals decoupling on the flex PCB

Threshold Tuning

- Quad module – 3: single wire bonded chip
- Fixed wire bonding diagram to have proper setting of configuration pins
- Configuration and operation shows the decoupling scheme implemented on the hybrid has good performance

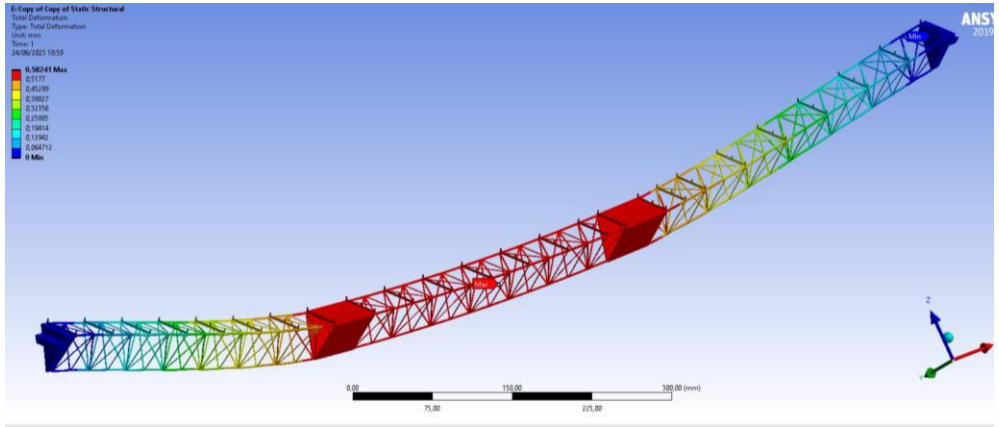
- Threshold and noise measurement using s-curve method
- Threshold tuning by a 3-bit trimming DAC

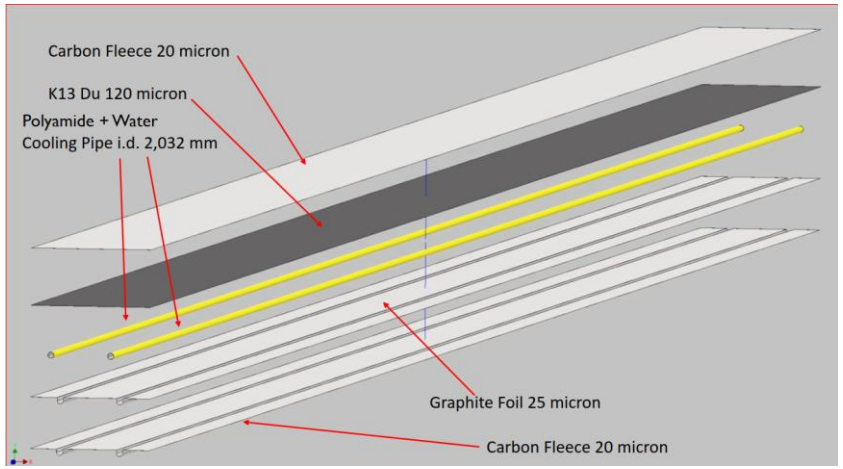
- Performance (on a sample matrix) comparable with operation on a carrier board

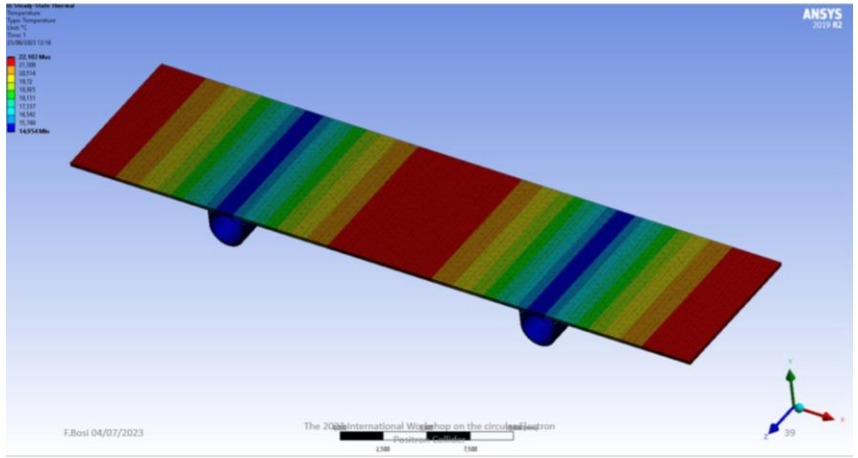


Low mass mechanical support

- Low mass stave prototype
  - long barrel layout (1332 mm length)
- Light support structures
  - water jet truss cutting and structure assemblying
  - design checked by FEA
  - support constructed and tested in Pisa
- Low-mass cooling interface
  - carbon cold plate
  - 2 mm diameter Kapton cooling pipes for water cooling





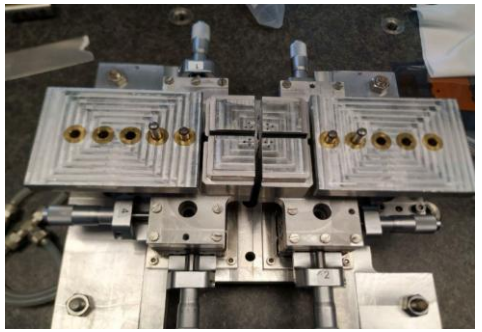


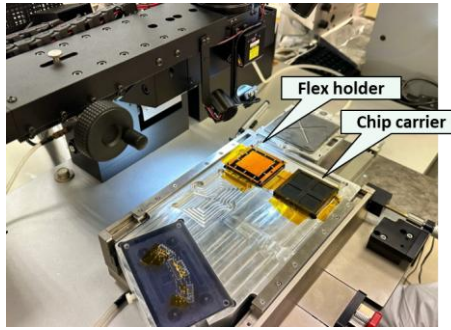
Project goals

1. **Demonstrate the operation of a CMOS based multi-chip module SP chain in realistic environment**
   - verifying the chip SLDO performance in multi-chip/module setups, establishing multi-module SP chain DAQ systems
   - assessing the feasibility of power bus based on Aluminum conductor
   - producing low mass cooling and mechanical supports.
   - *Many components for this stage are either existing or in advanced R&D stage from previous projects*, such as ATLASPix3.1 based quad-chip modules with 150μm thickness being assembled by Edinburgh and Milano, a long mechanical support stave from FCC-ee R&D from Pisa, 50μm thick ATLASPIX3.1 sensors in Heidelberg.
2. **Increase the level of integration above the ATLASPix3.1: Explore high density aluminum flex PCB production and innovative interconnections**
   - This stage will exploit new sensors to be submitted in LF 150 nm technology around September- December 2025 (led by KIT)
   - DAQ systems of the participant institutes will also be upgraded accordingly.

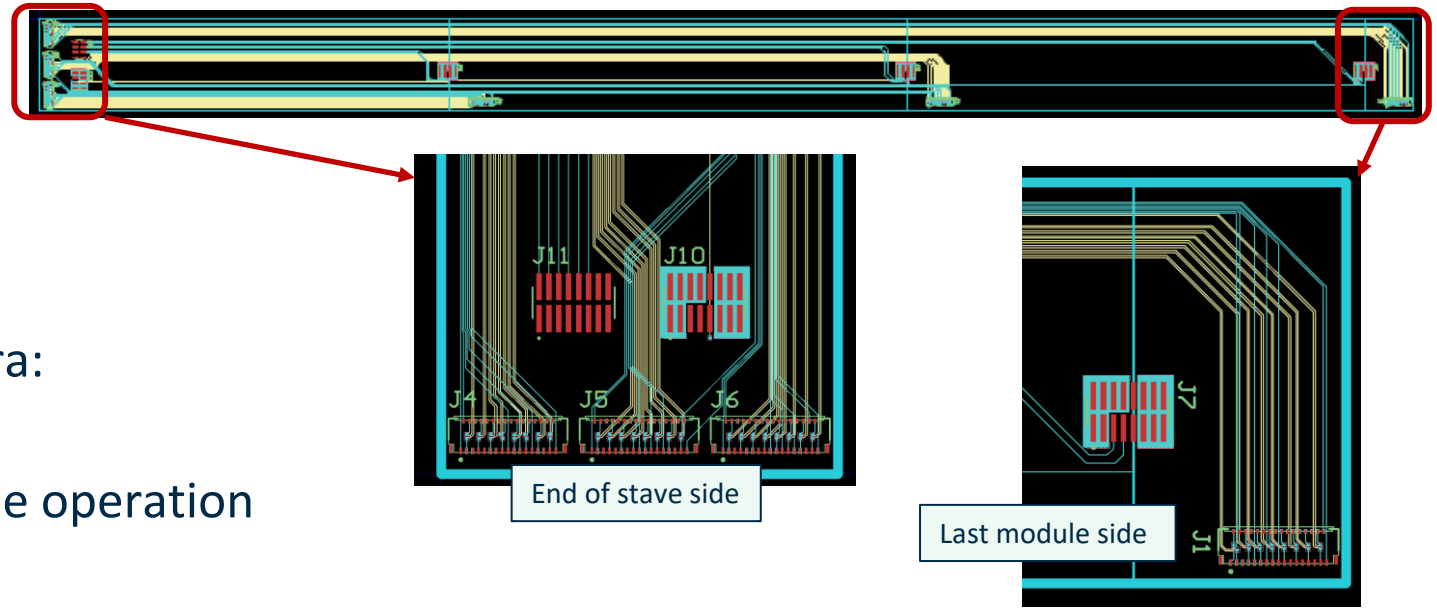
Stage 1 Completion

- Assembly modules with remaining ATLASPIX3.1 chips
  - ~6 modules with 150 μm sensors probed by Milano/Edinburgh
  - 50 μm sensors available from Heidelberg
  - Either pick-and-place or dedicated jig





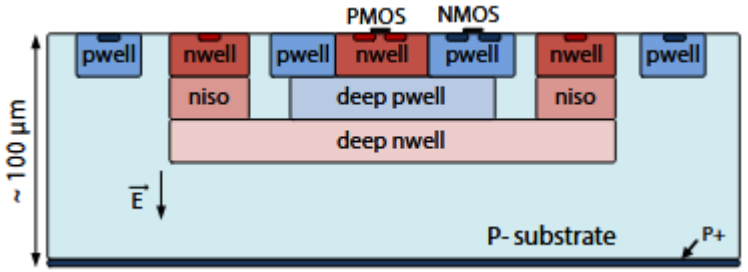
- Designed a power bus to test a multi-module serial power chain
  - Aluminium conductor to reduce thickness in radiation lengths
  - Connecting to modules by pigtails
  - 4 cm × 60 cm size to match CERN Microfabrication Lab capability
  - Received quotation from Rui De Oliveira: 14,200 CHF for a panel (5-8 pieces)
  - Ready to start production, since module operation issues are solved



- Loading of cold plate (half stave with 3 modules + heaters)
  - Need tooling for loading and instrumentation for assessing thermal performance

Stage 2 sensors

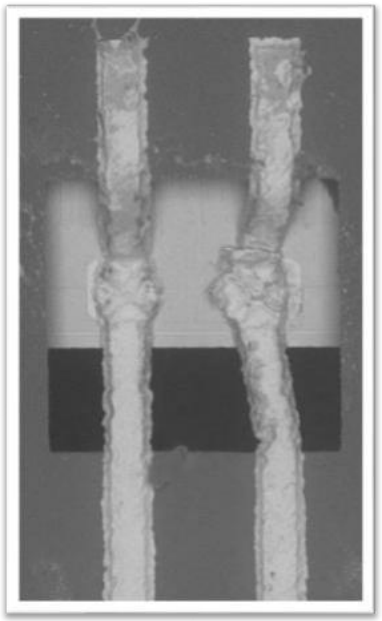
- Need new sensor since ATLASPIX3.1 chip are out of stock
- Testing multi-chip integration does not require a **chip** but a **CHIP**
  - ≥1 cm^2 to simplify handling and providing a significant load
- Specific features for system level integration, not usually implemented during early sensors R&D
  - **SLDO for serial powering** } **already tested on ATLASPIX3.1**
  - command decoder **with clock data recovery** } **not tested on ATLASPIX3.1**
  - **chip-to-chip data transfer** } **not available on ATLASPIX3.1**

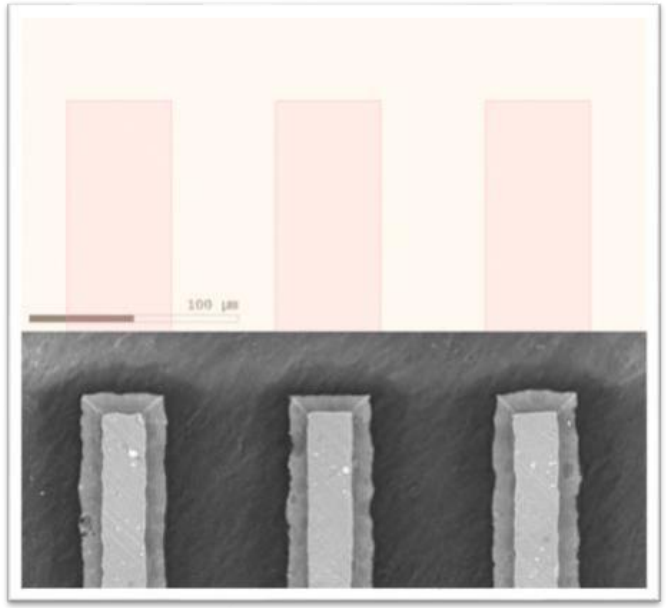


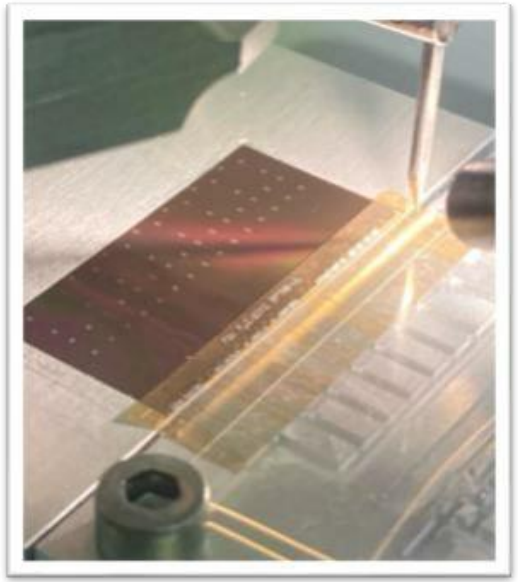
- **KIT** is planning a submission in **LFoundry 150 nm** process later this year
  - Migration into this technology of KIT TSI/AMS 180 nm designs
  - Large die, either half (2 cm^2) or full reticle size (4 cm^2)
  - SLDO from the TSI/AMS design implemented in LF 150
  - If contribution from this CCF project, daisy chain of chip data could be implemented
    - IP already developed for an ATLASPIX4 prototype run in TSI
  - Wish to book some wafers to be dedicated to integrations studies

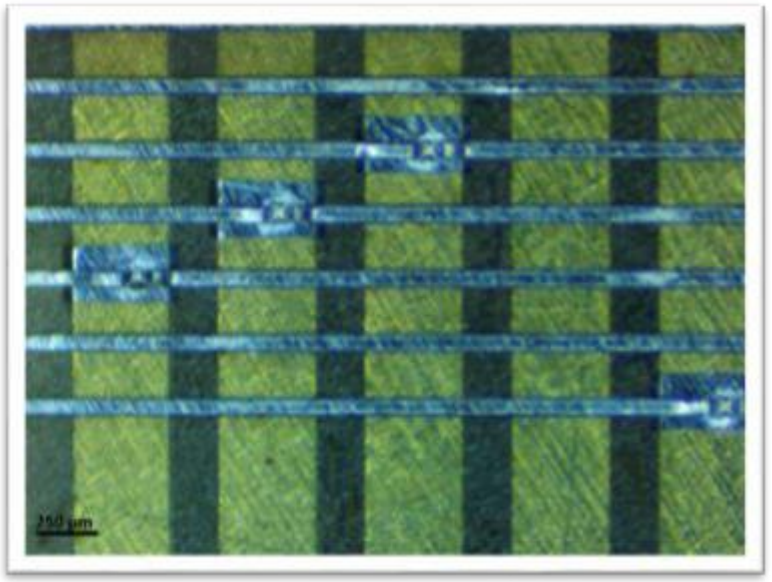
Stage 2: FBK technology

- Fabrication process inspired from the state-of-art LTU-Kharkiv [DOI: 10.15407/fm24.01.143]
- Processing inside FBK cleanrooms
- Kapton-Al PCBs
  - 20 μm Al thickness
  - 25 Kapton thickness
  - **Wafer level manufacturing (6" wafers)**
- Feature size
  - minimal size is 2 × Al thickness = 40 μm
  - very high line density (90 μm pitch)
- Interconnection
  - spTAB 75 × 75 μm tool tip
  - flex-to-chip TAB
  - flex-to-flex TAB:
    - use TAB as vias to reduce overall material
    - connection to additional flexible PCB









Stage 2 planning

1. **Submission and production of LF generic R&D chips**
2. **Thinning of sensors to samples of 150 and 50 μm thickness**
3. **Design and production of multi-chip module PCB for LF sensors:**

   Requires sequential steps in understanding and verification of chip behaviour:

   1. Test of chips on single-chip-carriers, to define the operating point, minimal amount of signal, wire bonding and register configuration
   2. Copper based version, standard wire bonding, to verify the schematics and operation of the multi-chip modules
   3. Low-mass Aluminum based using FBK technology, implementing tab bonding
4. **Assembly and operation of SP chain with multi-chip modules**
   - Daisy chaining of modules through adapter cards
   - Interface to DAQ system
5. **Realization of an integrated power bus and multi-chip module PCB**
   - Major step with respect to the separate structure with power bus and module PCB as separate pieces, connected by pigtails
   - **May test some of the chip-to-flex attach technologies being developed in WG7**

Deliverables and timelines

Deliverable	Timeline
Multi-chip module construction and readout (ATLASPix3.1)	06/2025
Al-flex production for ATLASPix3.1 power bus	09/2025
ATLASPix-based SP chain prototype construction and characterisation	03/2026
Submission and production of new CMOS sensors (LF)	07/2025-03/2026
Multi-chip readout flex submission for the LF CMOS sensors	12/2026
Multi-chip LF module construction and readout	03/2027
Al-flex production for the LF CMOS sensors	09/2027
LF sensors based SP chain prototype construction	01/2028
LF sensors based SP chain prototype evaluation	03/2028

Cost estimation

Procurements	Cost (CHF)
Al Serial Power Bus for ATLASPIX 3.1 (CERN)	15,000
Cu Multi Chip Module Flex LF sensors (design verification)	5,000
Al Multi Chip Module Flex LF sensors (FBK)	15,000
Al Serial Power Bus for LF sensors (CERN)	15,000
DAQ Upgrades (FPGA, chip carriers and readout boards)	15,000
Chip-to-Module assembly jigs	2,000
Stave loading and test equipment	10,000
CMOS Wafers production and processing (thinning and dicing)	20,000
Total project cost:	**107,000**

- **Total project cost:** **107,000 CHF**
  - DRD3 CCF contribution (13 institutes × 2650 CHF) 34,450 CHF
  - RD50 CCF contribution (6 institutes × 2650 CHF) 15,900 CHF
  - Funding from participating institutions 56,650 CHF

Conclusions

- Future experiments will need to develop large tracking systems with **low-mass services** (both electrical and thermal) and **efficient power distribution and data handling**
- In particular there is an increase in interest in the deployment of **Aluminum conductor flexible PCB**
- This *Common Project* aims to gather groups already addressing this topic in different experiments
  - timescale for some experiments is not far away
  - prototyping solutions for system issues in parallel to sensor development
  - share information about Al flexible PCB vendors
  - stimulate the development of IP implementing features for system level integration also in the developing projects within DRD3-WP1
  - cost benefit from synergies with already running projects

BACKUP

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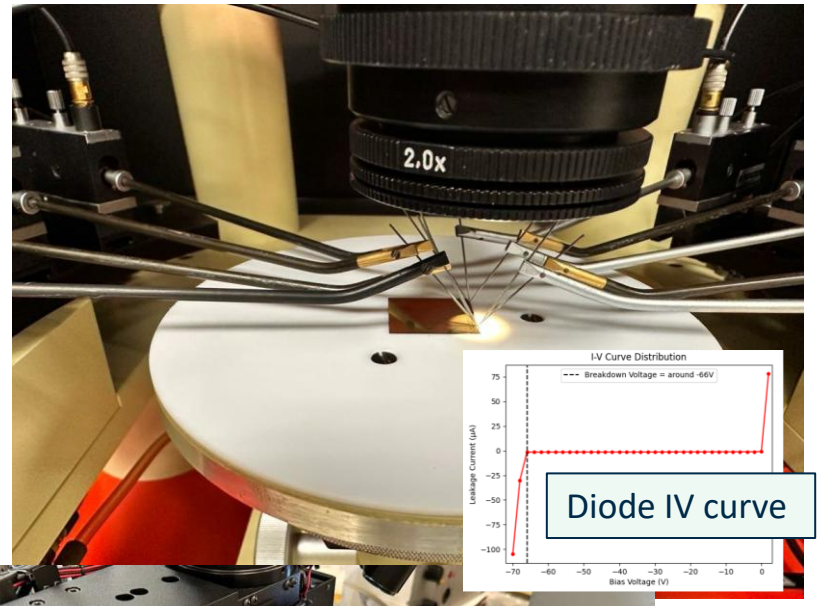
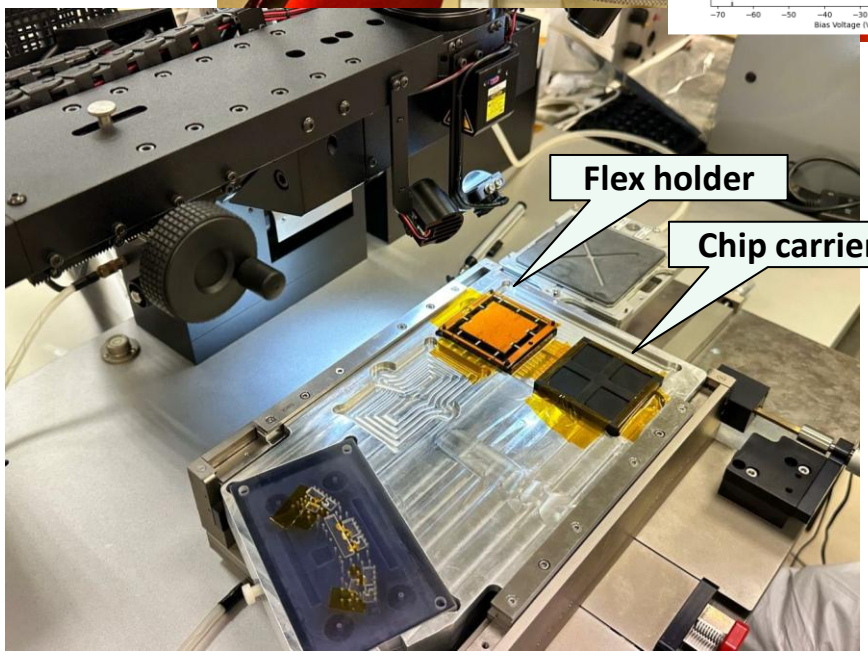
Module assembly

- I-V test for HV functionality under probe station before assembly
  - failure mode observed during the production of quad modules with direct powering
  - a short on one chip may jeopardize the operation of the other chips in the module
- Finetech pico die bonder
  - used also for the assembly of ATLAS ITk 3D modules
  - manual optical alignment between chips and flex-hybrid
- Araldite 2011 deposited by stamps method on flex backside



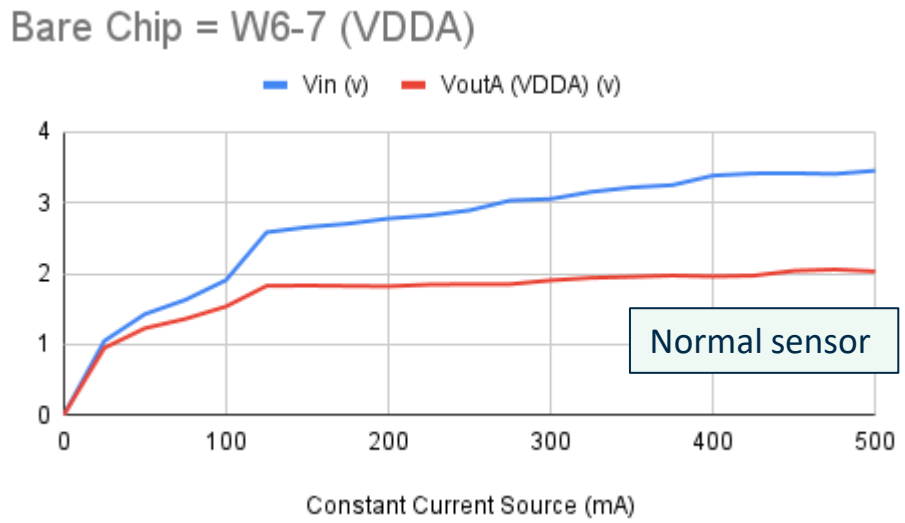


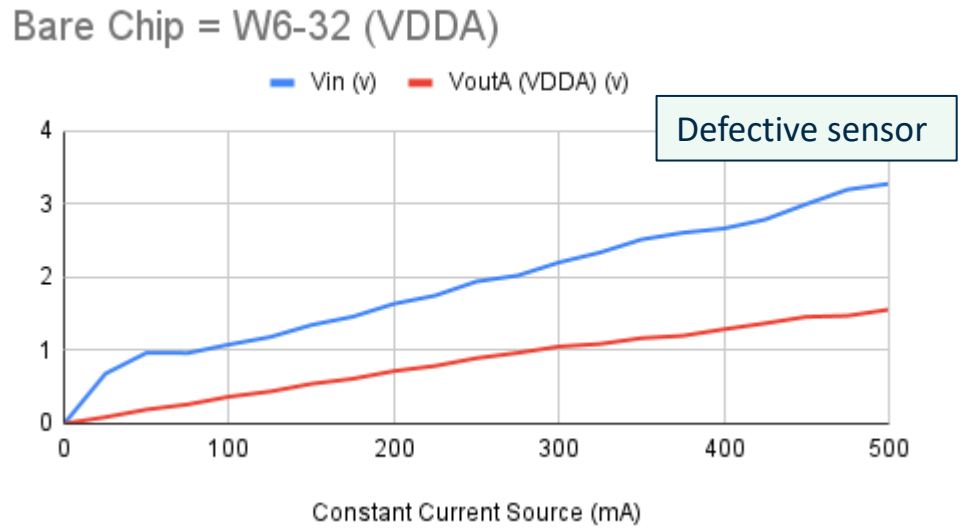
ATLASPIX3.1 Wafer 6 Probing

- Initial probing setup was not testing correctly the VDDD regulator: needle configuration changed in March

- The **VDDA** is regulated at 2.1 V after ~250 mA input current
- The **VDDD** is regulated at 2.1 V after ~150mA input current
- Large voltage drop is an issue of the testing setup (long cable and needle contact resistance)

- Tested all chips from wafer #6
  - 11/48 show anomalous behaviour
  - Large sensor power consumption
  - Does not turn on even at rather high bias currents
  - Chip selection critical since module yield is chip yield to the 4th power

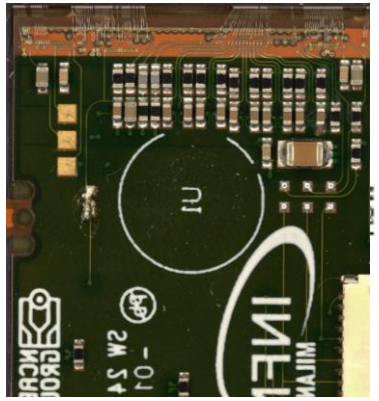


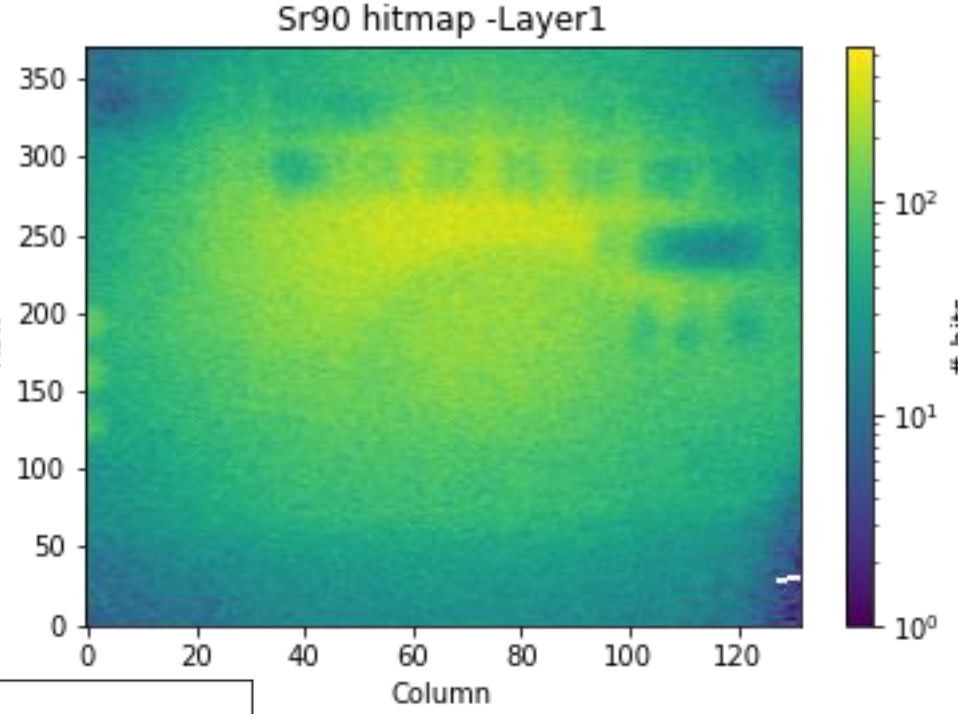


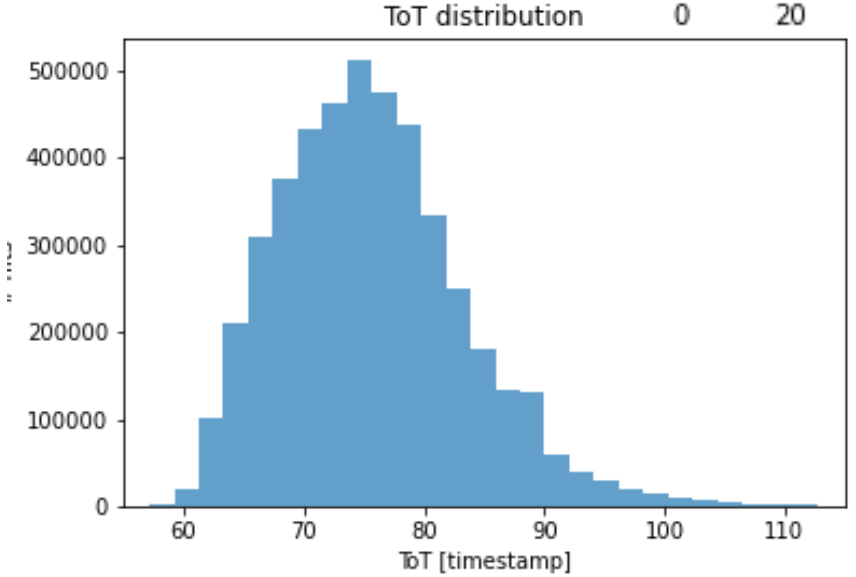
Source Scan

- Quad module – 3: single wire bonded chip
- Fixed wire bonding diagram to have proper setting of configuration pins
- Configuration and operation shows the decoupling scheme implemented on the hybrid has good performance

- Measurement with ^{90}Sr beta source
- Full 132x372 pixel matrix
- Pulse height measurement with ToT

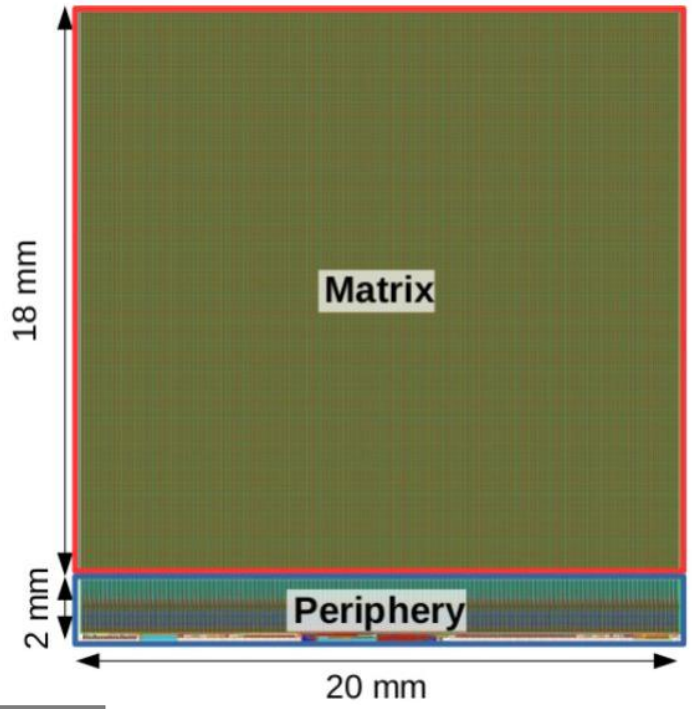


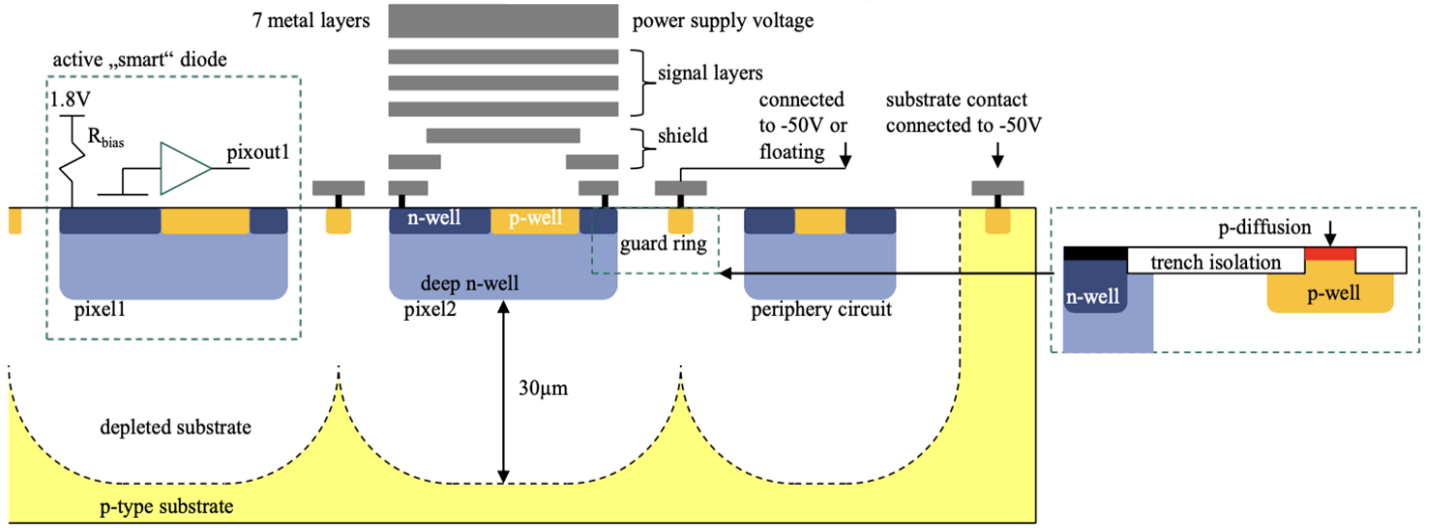




ATLASPIX3

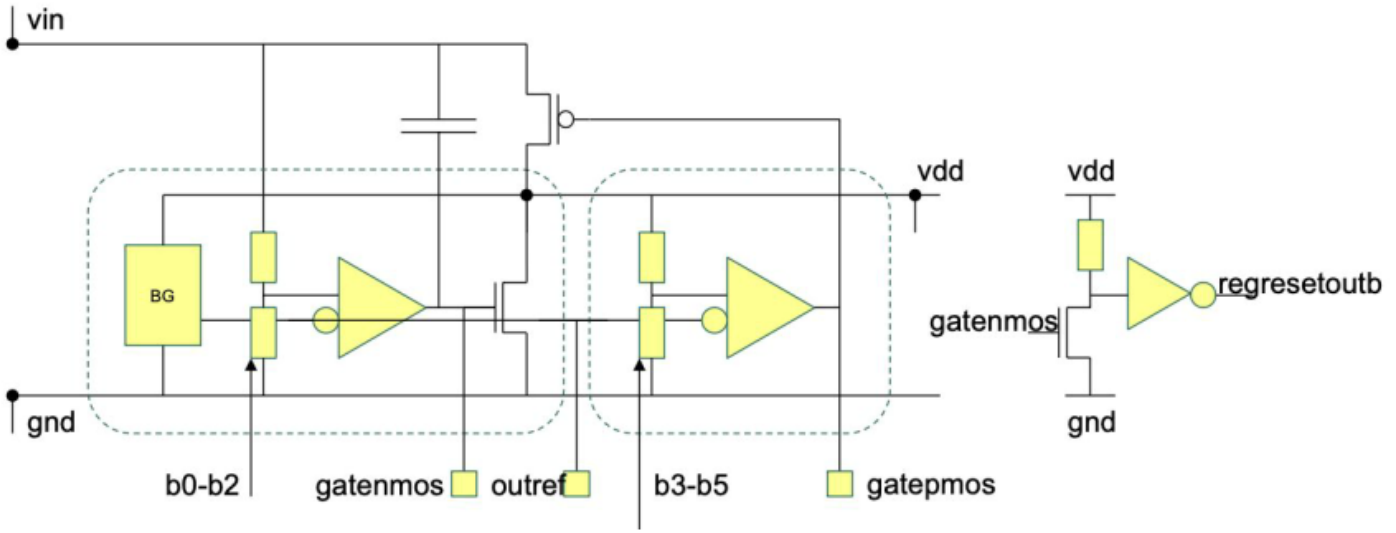
- **ATLASPIX3 general features**
  - **TSI 180 nm HVCMOS** technology
  - full-reticle size **20×21 mm²** monolithic pixel sensor
  - 200 Ωcm substrate (other substrates up to 2 kΩcm also possible)
  - **132 columns of 372 pixels**
  - **pixel size 50×150 µm²** (25×150 µm² on recent prototypes)
  - **breakdown voltage ∼-60 V**
  - up to **1.28 Gbps downlink**
  - **25 ns timestamping**
  - analog pixel matrix, digital processing in periphery
- Both **triggerless** and **triggered** readout modes:
  - two End of Column buffers
  - 372 hit buffers for triggerless readout
  - 80 trigger buffers for triggered readout

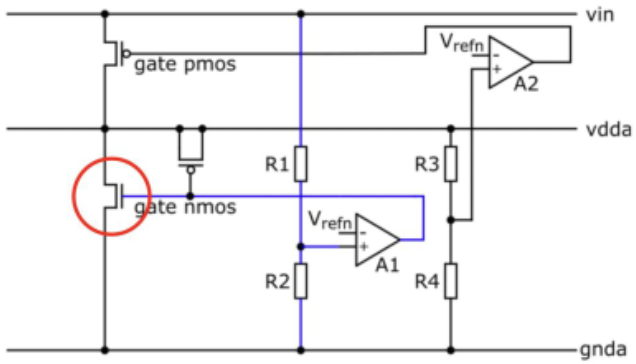




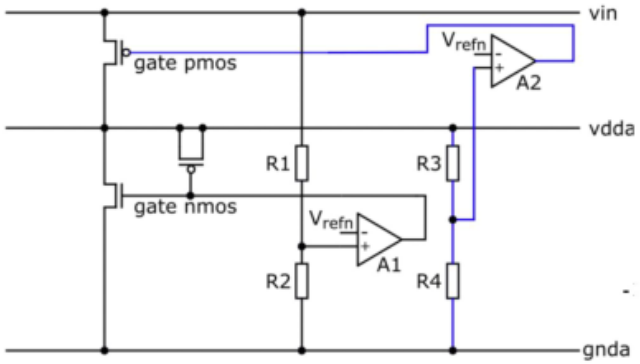
ATLASPIX3 Serial Powering

- Version **ATLASPix3.1** has possibility for **serial powering** through **two shunt/low dropout regulators**
  - **digital** and **analog** (VDDD/A)
  - **3 bits** to tune threshold of shunt regulator
  - **3 bits** to tune VDD
  - gatenmos, outref, gatepmos are for monitoring
  - regresetoutb can be used as power on reset
- Possibility to use a **single power supply for all the 6 alimentation needed to operate the chips**





- First loop defines **shunt regulators**



- Second loop **regulates VDDD/As**

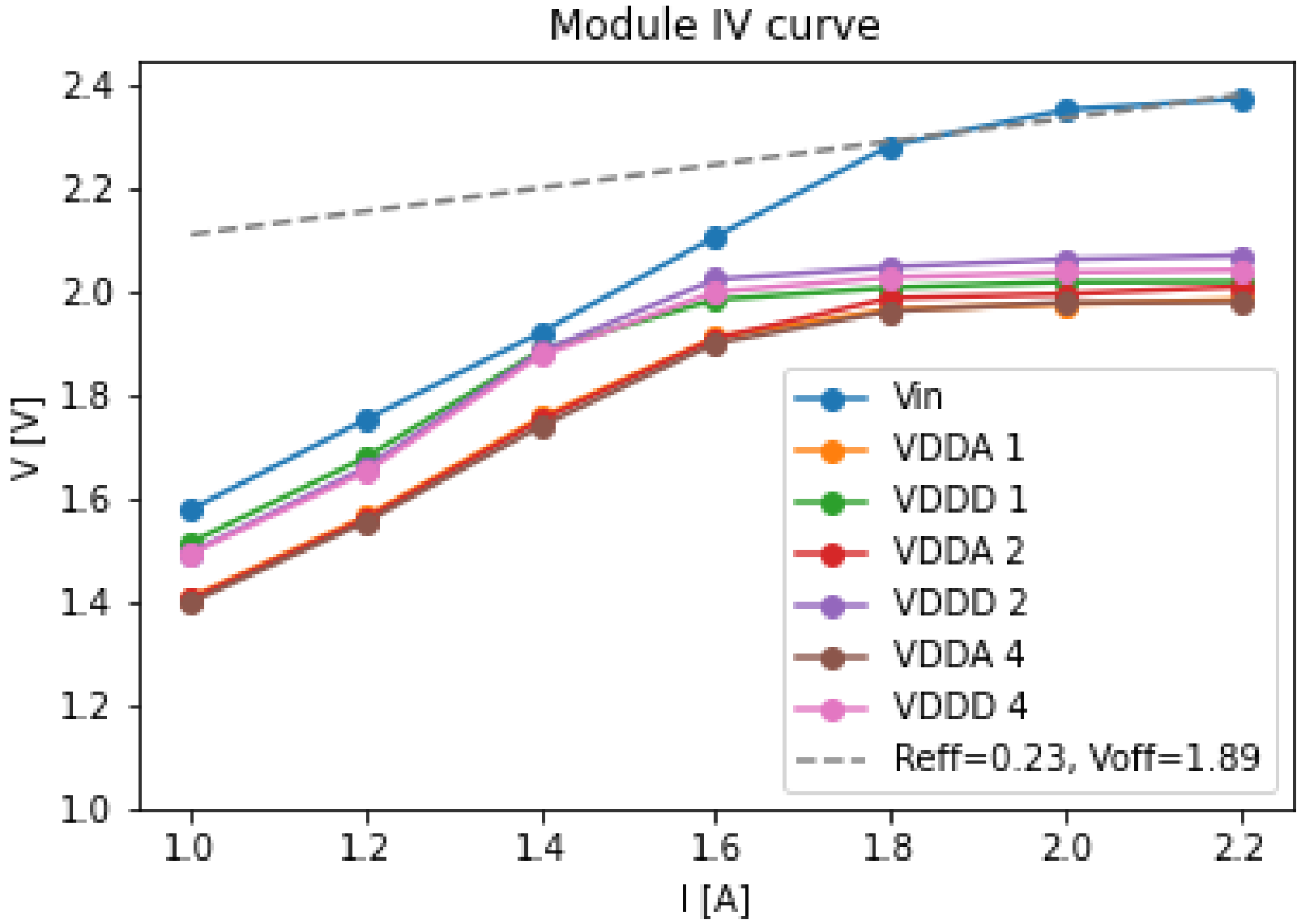
Risk assessment (What if...?)

- **LF submission will not provide suitable chips**
  - hold some ATLASPIX3.1 chips till result of submission is known
  - perform stage 2 with P2Pix sensors
  - "digital modules" using RD53 pixel chips for HL-LHC (no physical signal, electrical only test – too high power consumption)

- **Do not get INFN funding for FBK flexible PCB production**
  - build module flex with standard wire bonding technique
  - explore another vendor

Si tracker: system considerations

- **Complete system consists of 900'000 cm² area / 4 cm² chip = 225k chips (56k quad-modules)**
  - aggregation of several modules for data and services distribution is essential
  - inner tracker will be 5--10% of this
- **Data rate** constrained by the inner tracker
  - average rate 10^{-4} - 10^{-3} particles cm^{-2} $event^{-1}$ at Z peak
  - assuming 2 hits/particle, 96 bits/hit for ATLASPIX3
  - **640 Mbps link/quad-module** (assuming local module aggregation) provides ample operational margin
  - 16 modules can be arranged into **10 Gbps fast links**: **3.5k links**
    - can also assume 100 Gbps links will be available: 350 links
- **DAQ architecture**
  - **triggerless readout** will fit the data transmission budget but requires off-chip re-ordering of data
  - **triggered readout** will be **simpler** and would also reduce the bandwidth occupancy
- **Power consumption**
  - ATLASPIX3 power consumption **150 mW/cm²**
  - 600 mW/chip → 2.4 W/module → **total FE power 130 kW**
  - additional power for on detector aggregation and de-randomizations **~2W/link**


Module IV curve
V [V]
I [A]
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
1.0
1.2
1.4
1.6
1.8
2.0
2.2
Vin
VDDA 1
VDDD 1
VDDA 2
VDDD 2
VDDA 4
VDDD 4
Reff=0.23, Voff=1.89