

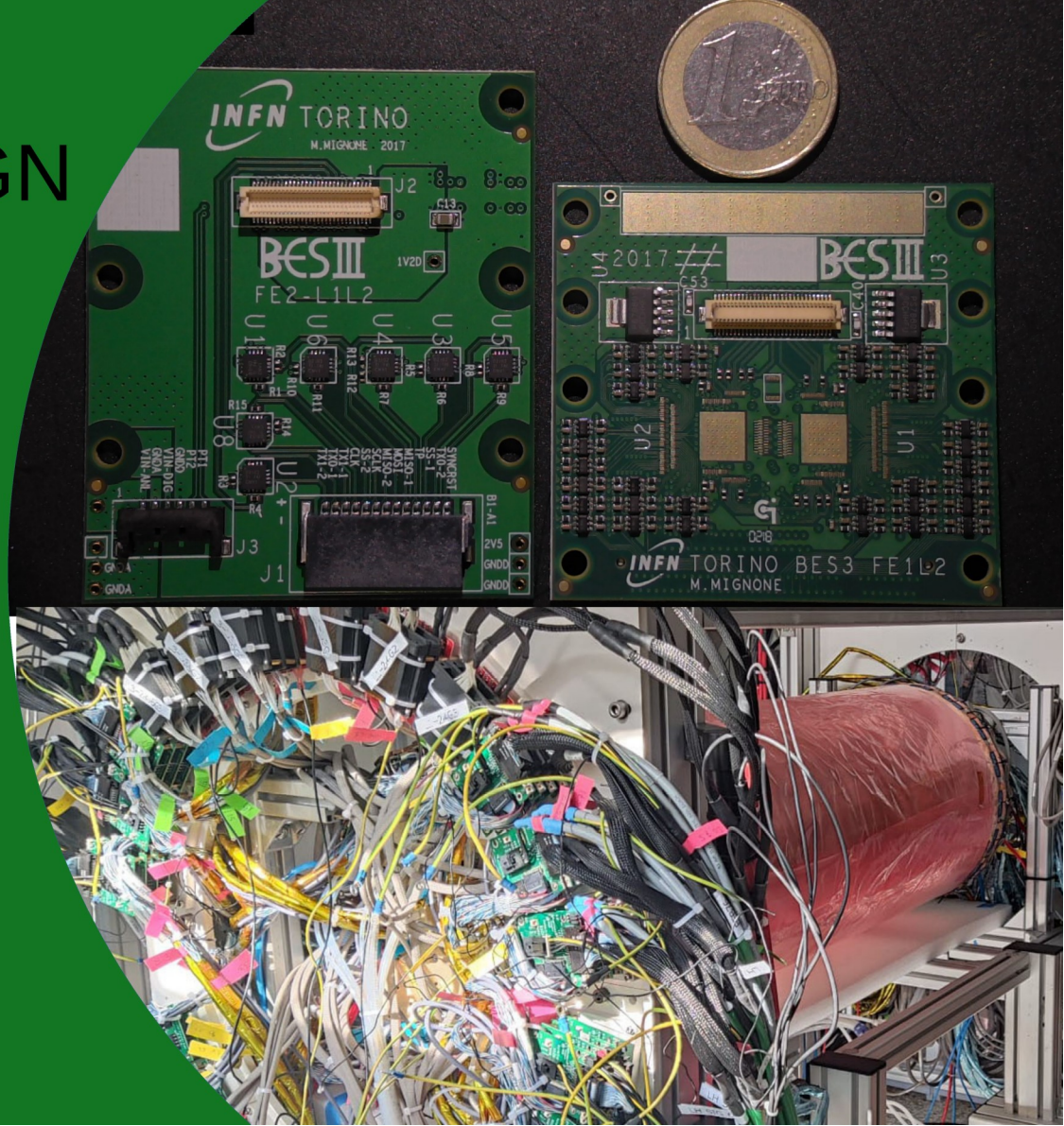
TIGER FRONT END BOARDS - NEW DESIGN

Federico Matias Melendi
INFN Ferrara, University of Ferrara
mlnfrfc@unife.it

FCC collaboration meeting -Ferrara - 27/05/2025



Università
degli Studi
di Ferrara





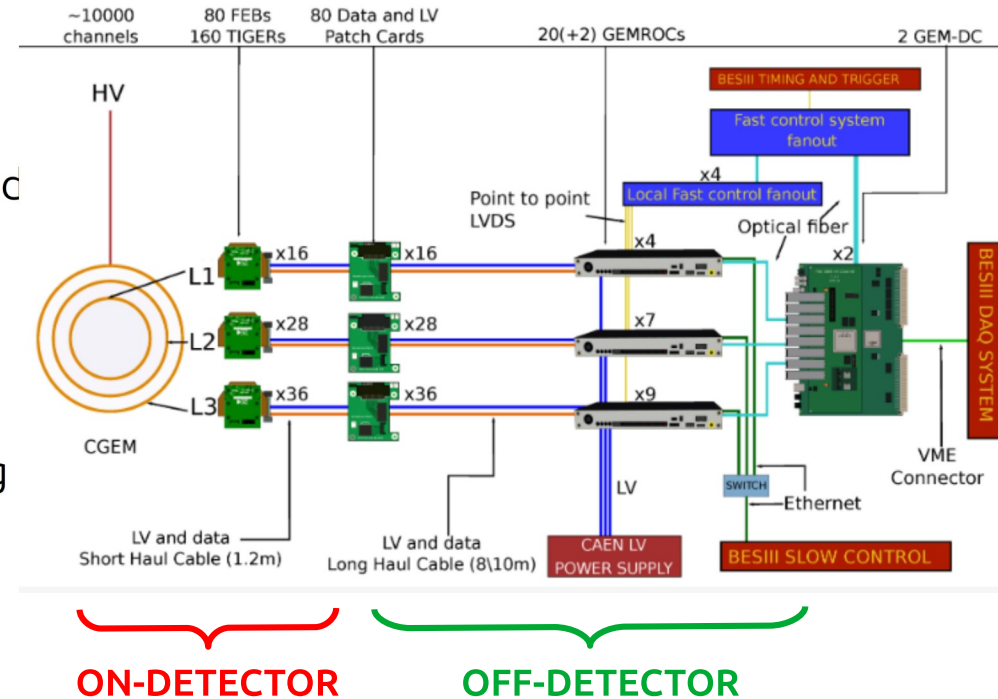
OUTLINE:

- TIGER-GEMROC read out
- TIGER integration in BESIII
- FEBs improvement
- Conclusions & outlook



TIGER-GEMROC read out

- The readout chain consists of **ON-detector** and **OFF-Detector** electronics
- The OFF-detector electronics is based on GEM Read Out Cards (GEMROC) and Data Low Voltage Patch Cards (DLVPC)
- GEMROC is an FPGA based backend module for configuring the ON-detector electronics, powering and managing data flow during acquisition



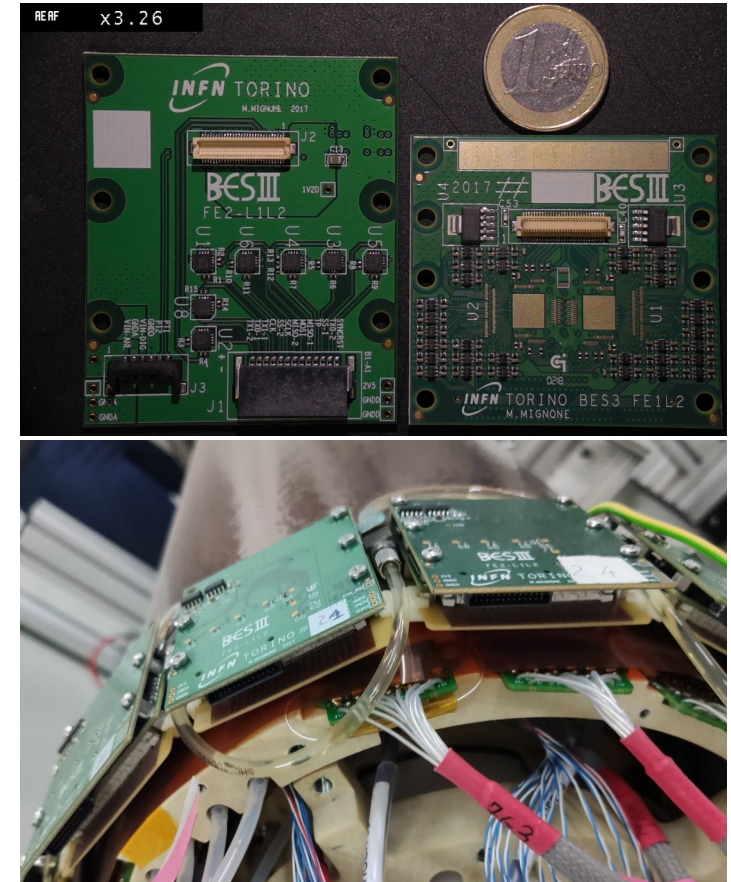
For more details: [The CGEM-IT readout chain - A. Amoroso et al 2021 JINST 16 P08065](#)

TIGER-GEMROC read out

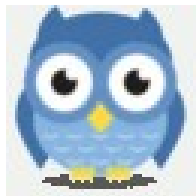
- The **ON-Detector** electronics is composed by Front-End-Boards (FEBs). Each FEB host two TIGER ASIC chip
- TIGER (Torino Integrated GEM Electronics for Readout) is a 64-channel mixed signal ASIC capable of performing simultaneous **charge and time measurements**
- Each FEB was calibrated and tested by INFN Turin
- before being installed
- A **cooling system** ensures a constant operating temperature

For more details: [The CGEM-IT readout chain - A. Amoroso et al 2021 JINST 16 P08065](#)
[A mixed-signal ASIC for time and charge measurements with GEM detectors](#)

Photo by M. Mignone



TIGER-GEMROC software



GUF – **G**raphical **U**ser **F**rontend **I**nterface → python based software

- Interface with GEMROCs and TIGERs
- Manages the data acquisition
- Measures noise rate and other performance
- User-friendly interface (user mode/expert mode)



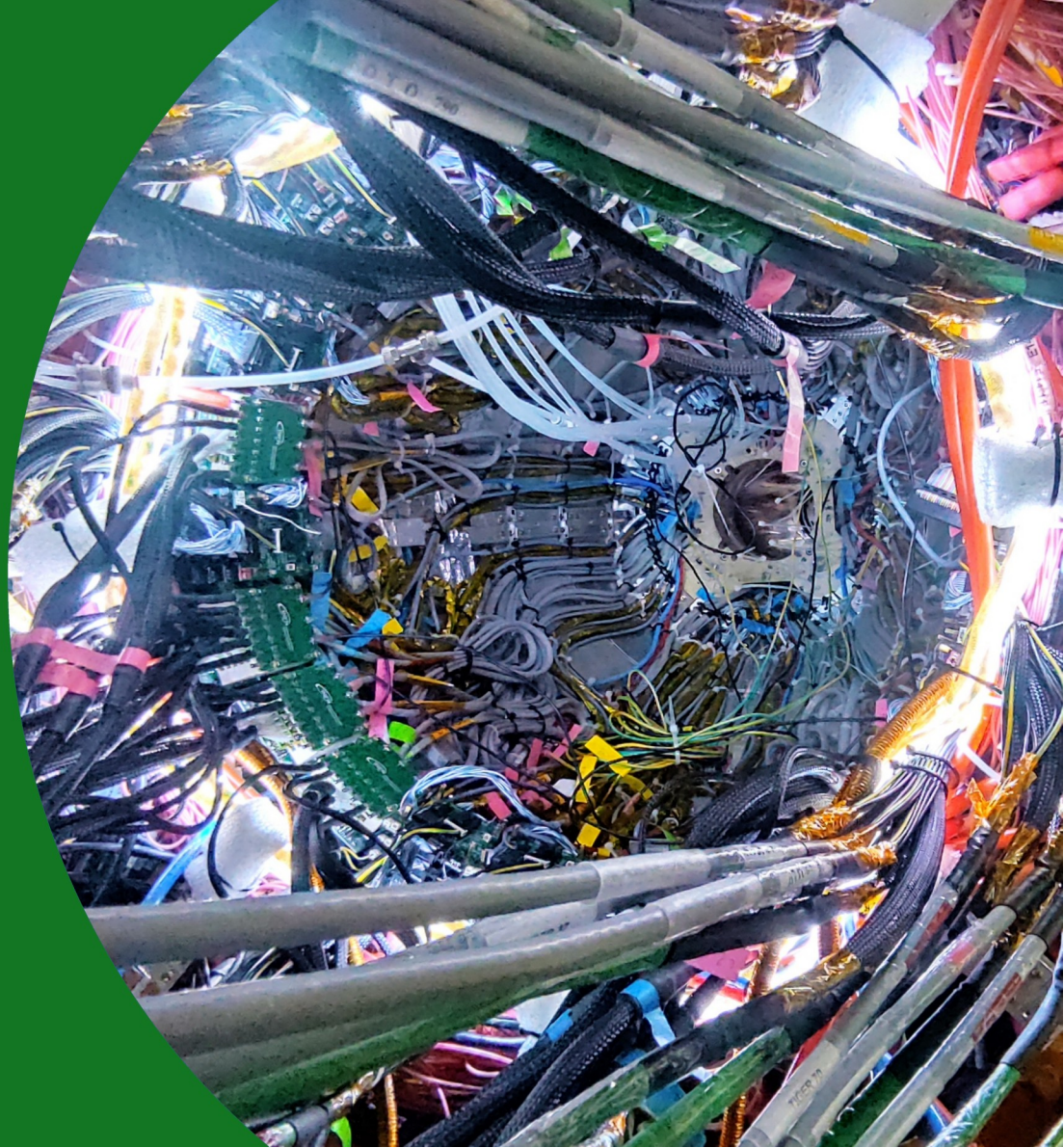
CIVETTA (**C**omplete **I**nteractive **V**ersatile **T**est **T**ool **A**alysis)

- Data sampling
- Decode
- Calibration and mapping
- OFF-LINE analysis

For more details: [Deployment of the readout electronics for the BESIII Cylindrical GEM Inner Tracker A. Bortone - 16/11/2021](#)



TIGER integration & Identified areas for improvement

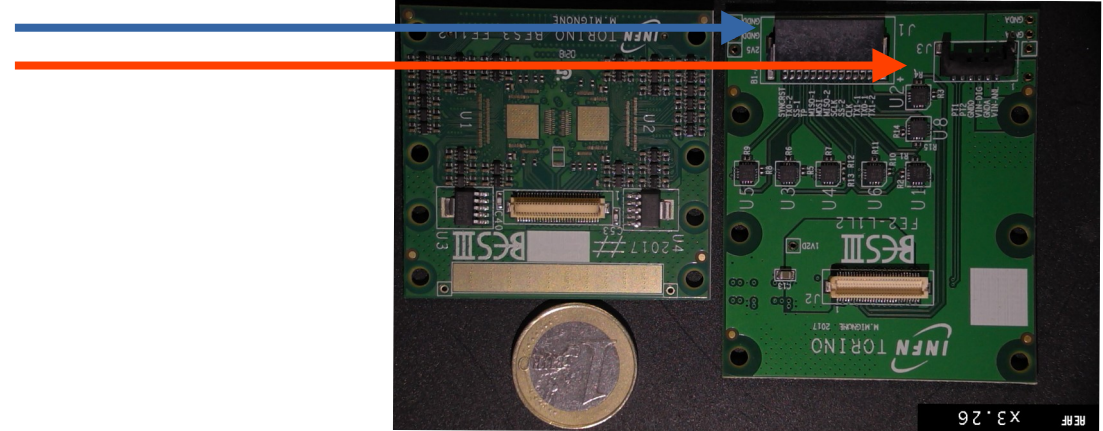


- In December 2024 the integration of the TIGER electronics was completed
- During operations, several system peculiarities were highlighted
- Extensive research has been conducted to enhance system stability and performance
→ This help us to identify several improvement for our system!



Identified areas for improvement

- **Low voltage** and **data** connectors



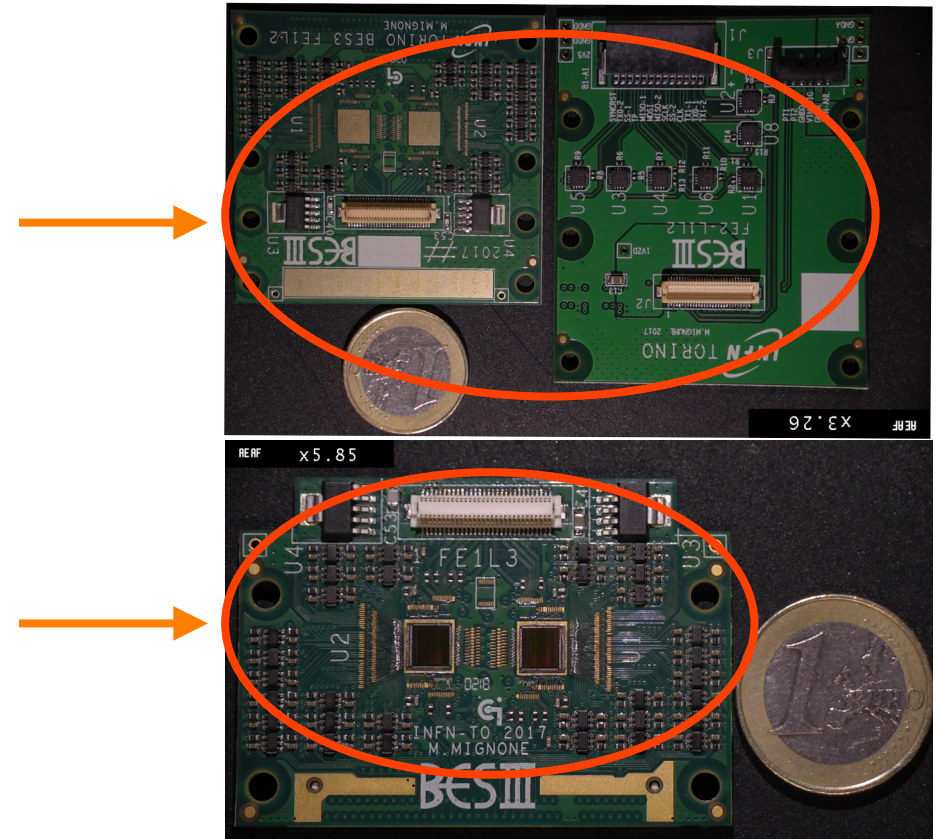
Identified areas for improvement

- **Low voltage** and **data** connectors
- Sub-optimal cable shielding and reliability



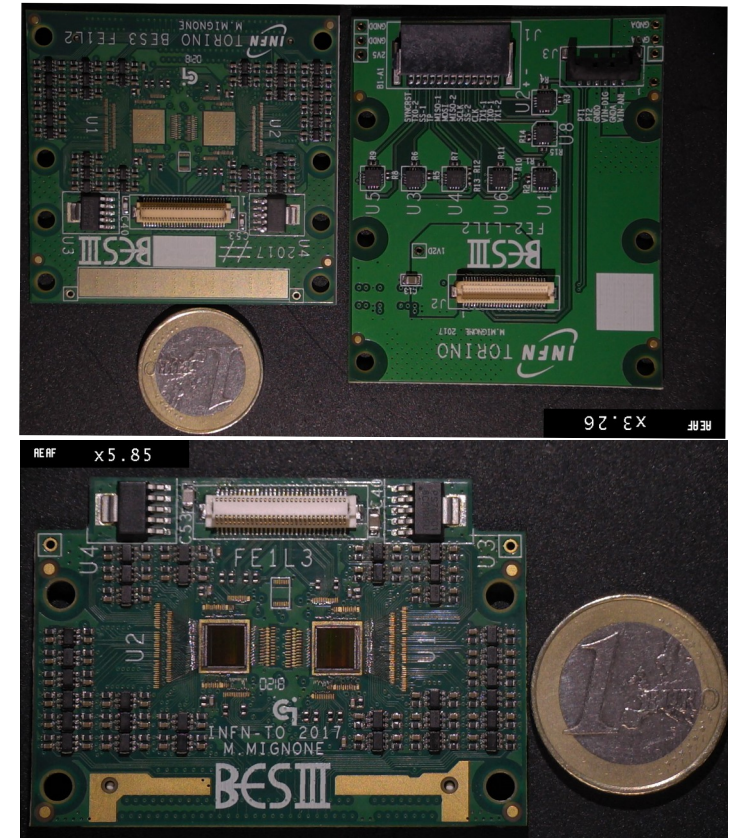
Identified areas for improvement

- **Low voltage** and **data** connectors
- Sub-optimal cable shielding and reliability
- High density of components
(due to BESIII mechanical constraints and requirements)

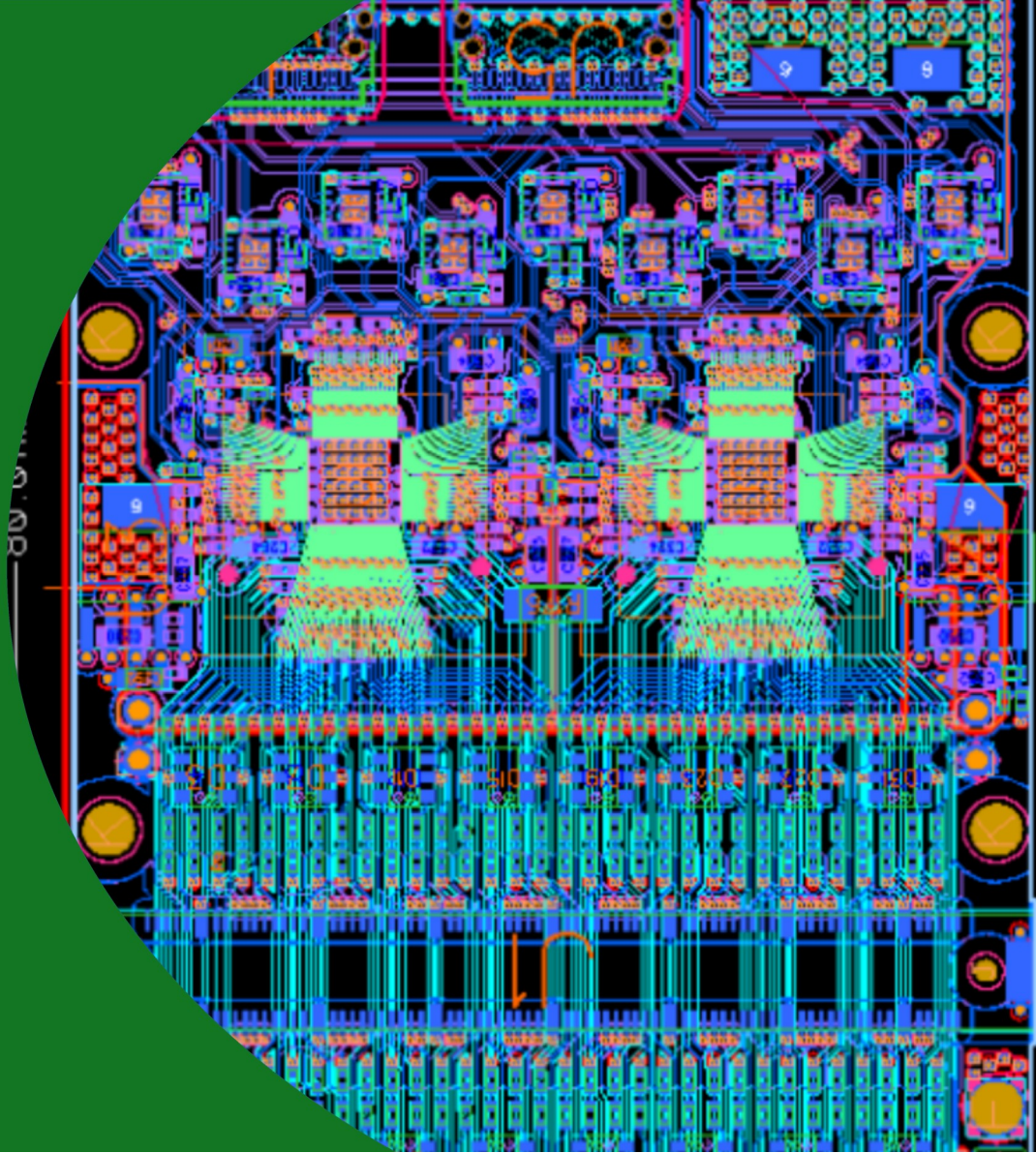


Identified areas for improvement

- **Low voltage** and **data** connectors
- Sub-optimal cable shielding and reliability
- High density of components
(due to BESIII mechanical constraints and requirements)
- DLVPCs not ideal shield
- Some channels at the connector's edges are noisier than others

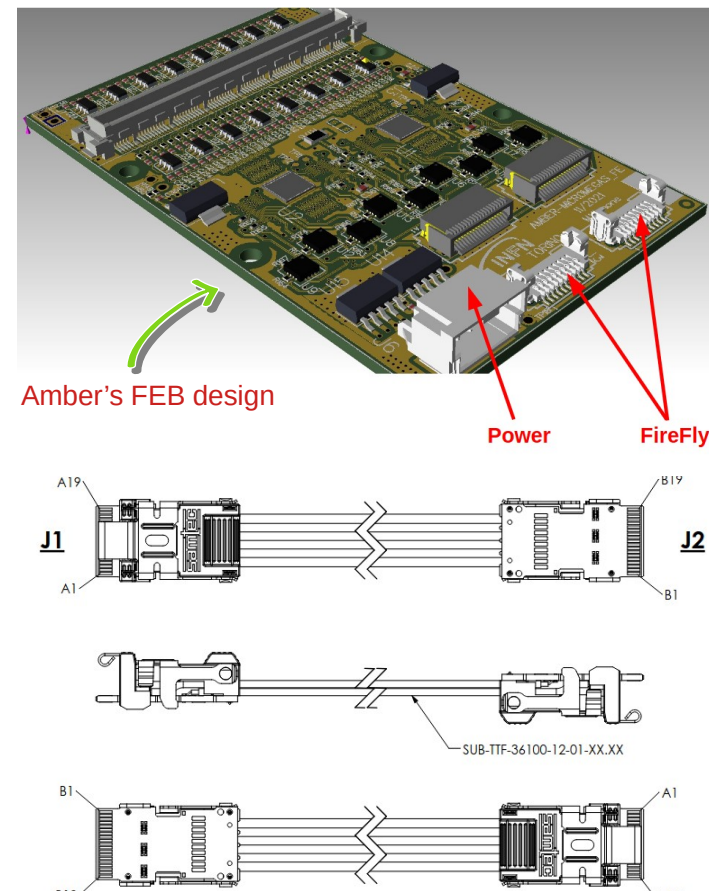


Improvements for the readout chain



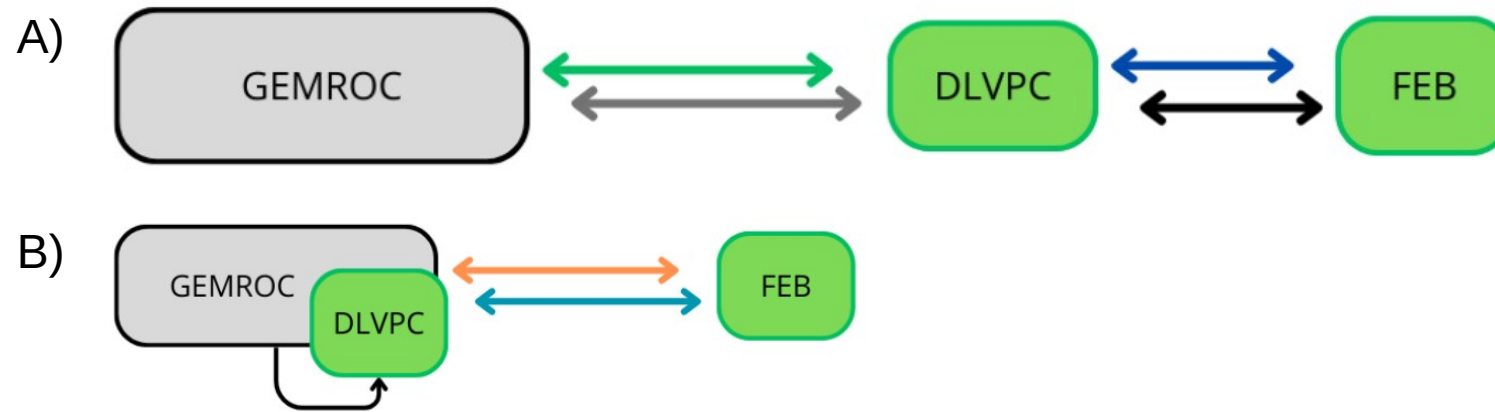
Improvements for the readout chain

- New connector for both low voltage and data
→ FireFly connector has been proposed (strong & reliable)
- New FEBs design: from 2PCBs → 1PCB
- New configuration of the protection circuit of TIGER channels (design and definition still ongoing)
- Larger ground connection on the FEBs (APV style)



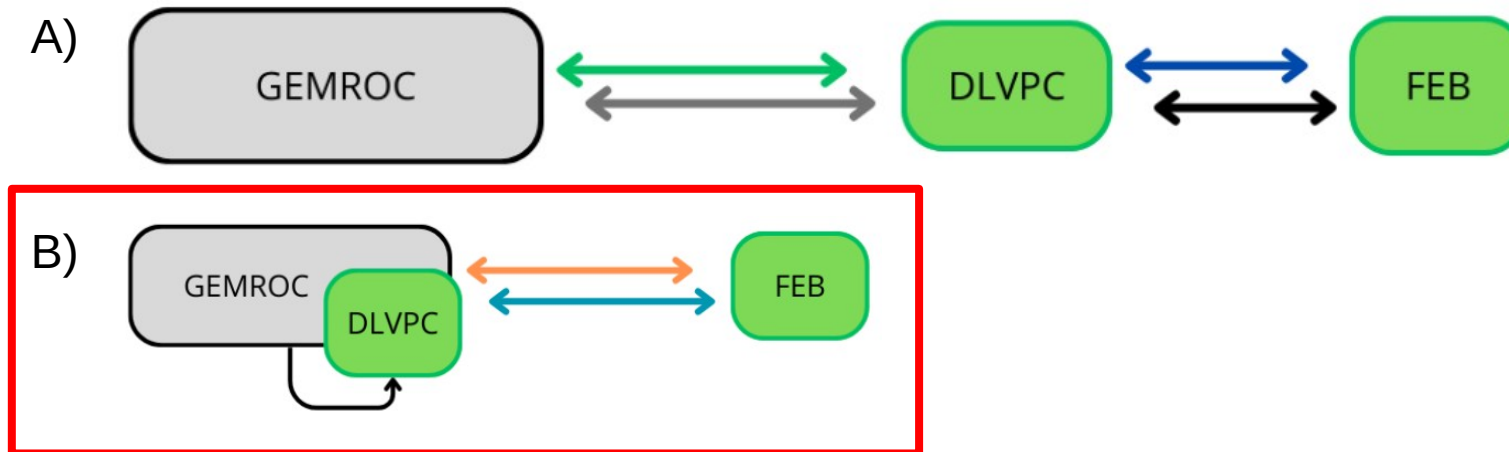
Improvements for the readout chain

New design of DLVPCs, elimination of Long haul cables, DLVPCs directly connected to GEMROCs → it simplifies the system, allowing for increased **robustness** and **straightforward operation**



Improvements for the readout chain

New design of DLVPCs, elimination of Long haul cables, DLVPCs directly connected to GEMROCs → it simplifies the system, allowing for increased **robustness** and **straightforward operation**





Conclusion & outlook



- The innovative FEB design is developed to **maximize the potential of the TIGER chip**, unconstrained by the previous mechanical limitations of BESIII
- The new DLVPCs configuration make the system simpler to implement and compact (i.e. elimination of long haul, better ground, etc...)
- The design is still ongoing:
 - FEBs desing, M. Da Rocha Rolo, M. Greco and M. Mignone INFN Torino
 - DLVPCs design, A. Cotta Ramusino INFN Ferrara

- To test the new FEBs coupled with μ -RWELL a test beam is being planed (November 2025)
 - DUT: 1-D μ -RWELL, TRKs: GEMs, Read out: TIGER/GEMROC

- To test the new FEBs coupled with μ -RWELL a test beam is being planed (November 2025)
 - DUT: 1-D μ -RWELL, TRKs: GEMs, Read out: TIGER/GEMROC
- For the test beam a dedicated GEM support and HV distribution system is being designed

- To test the new FEBs coupled with μ -RWELL a test beam is being planed (November 2025)
 - DUT: 1-D μ -RWELL, TRKs: GEMs, Read out: TIGER/GEMROC
- For the test beam a dedicated GEM support and HV distribution system is being designed
- Introduction of dedicated shielding for both HV end electronics

- To test the new FEBs coupled with μ -RWELL a test beam is being planed (November 2025)
 - DUT: 1-D μ -RWELL, TRKs: GEMs, Read out: TIGER/GEMROC
- For the test beam a dedicated GEM support and HV distribution system is being designed
- Introduction of dedicated shielding for both HV end electronics
- New Mechanics to host the distribution system
 - Activity ongoing, R. Malaguti and FCC team INFN Ferrara

- To test the new FEBs coupled with μ -RWELL a test beam is being planed (November 2025)
 - DUT: 1-D μ -RWELL, TRKs: GEMs, Read out: TIGER/GEMROC
- For the test beam a dedicated GEM support and HV distribution system is being designed
- Introduction of dedicated shielding for both HV end electronics
- New Mechanics to host the distribution system
 - Activity ongoing, R. Malaguti and FCC team INFN Ferrara
 - we will give you update regarding the operation schedule as soon as possible!

THANK YOU FOR YOUR ATTENTION!

FEDERICO MATIAS MELENDI

mlnfr@unife.it fmelendi@fe.infn.it



Funded by the
European Union
NextGenerationEU



Horizon 2020
European Union funding
for Research & Innovation

European
Commission

BESIIICGEM
RISE
FEST



Università
degli Studi
di Ferrara