

### R&D for vertex tracker

○ FCC

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INFN Pisa

IDEA Study group 17June 2025

# Summary

- Inner vertex air-cooling test
- Vertex services integration and assembly test
- Development of a stave for the Silicon Wrapper with serial power and low mass mechanics

#### Expression of interests submitted to European Strategy Update

Expression of Interest for a lightweight vertex detector for FCC-ee

Involved Laboratories: Italy: INFN - Genova, Frascati, Milano, Padova, Perugia, Pisa, Torino, Trieste-Udine Switzerland: ETH Zurich, Paul Scherrer Institute, University of Zurich United States of America: Brown University, BNL, FNAL, LBNL, MIT, SLAC, Stony Brook University Expression of Interest for the development of modules for Vertex detector and Silicon Wrapper with combined tracking and timing capability in LFoundry 110nm technology

> Involved Laboratories: Italy: INFN - Bologna, Milano, Padova, Pavia, Perugia, Pisa, Torino, TIFPA United States: FNAL

- Depleted Monolithic Active Pixel Detectors (DMAPS)
- Very thin sensors and curved geometries
- Layout optimization
- Low power architectures: air cooling
- **o** Integration with the machine

Report on ARCADIA tests and perspectives by M. Mandurrino at the 6th IDEA meeting

https://agenda.infn.it/event/46076/contributions/263027/attachments/134772/201700/2025Mandurrino\_RDFCC.pdf

### Services integration is instrumental also for the mockup of the interaction region being carried out at INFN-LNF

#### See M. Boscolo presentation at 2nd IDEA meeting

https://agenda.infn.it/event/43761/contributions/247869/attachments/128381/190149/241119\_MDI\_Mboscolo\_IDEA%20MEETING.pdf

- Central vacuum chamber with cooling system
- Conical vacuum chamber with cooling system
- Bellows
- Inner vertex detector with air cooling system
- Outer tracker
- Support tube
- Luminosity calorimeter



### **Current vertex layout**

Outer vertex tracker: ATLASPix3 based

Modules of 50  $\times$  150  $\mu$ m<sup>2</sup>pixel size

- Intermediate barrel at 13 cm radius
- Outer barrel at 31.5 cm radius
- 3 discs per side

Inner Vertex detector: ARCADIA based

Modules of 25  $\times$  25  $\mu$ m<sup>2</sup>pixel size

3 barrel layers at - 13.7, 23.7 and 34/35.6 mm radius







### Study of the services

- Inner vertex
- Air cooled

- **Outer vertex and disks**
- Water cooled



- Layer 3 ducts
- Layer 2 ducts
- Layer 1 ducts

<u>6 sectors of 60° for each of the three</u> <u>indipendently powered layers</u> Diffusers included in the 3D printed support with hose connection Need to be optimized in terms of length and pitch angle to allow for easy cables routing

Rear view



Pipe system that wraps around the innermost disk:

- Minimize the effect on the others
- Necessity of an adequate assembly procedure

# **External Support Tube**

2800

Di=710

**Reinforced Rib** 





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# Study of the air cooling

Goal of the study

- **Reproduce simulation result**
- See
- <u>https://indico.cern.ch/event/1439509/contributions/6289579/attachments/299</u>
  <u>5130/5276700/Baldinelli.pdf</u>
- Test turbulence, mechanical stress/vibrations
- Test interference with cables and beam-pipe services



of air cooling





Compressed air system to define:

- Flow rate needed to cool the detectors
- **Pressure drop** in the central region •
- **Temperature increase** between inlet and outlet



First test on a 60° circular sector of layer 3 including five staves

Next test on the same circular sector with all three layers

In progress







#### Fabrizio Palla – INFN Pisa– IDEA vertex R&D – IDEA Study Meeting 17 June 2025



#### Designed to:

- Be adaptable
- Be controlled
- Allow CFD result verification

**Bonding tool** 



Lower

Stave dimensions (mm)			
	н	W	
Design	10.25	1.4	
Real	10.5	2.6*	

\* increase in thickness of Rohacell







#### With stave



With the **integrated design** solution:

#### **ADVANTAGES:**

- 1. Layer 1 stiffeners are eliminated
- 2. Layer 1 air ducts are eliminated
- 3. Small additional heat load (12 W compatible with the paraffin system performance)
- 4. Layer 1 is  $\sim$ 2 mm closer to the interaction point
- 5. Easier integration of cooling systems

Contact between the detectors and the outer jacket mediated by a layer of electrical insulator:

- Kapton
- Ceramics



Need for a rigid support for the sensors:

- Bonding
- Centering
- Assembly

• Design under study

#### HV-CMOS demonstrator with serial powering Birmingham, Bristol, Edinburgh, EBK, Heidelberg, Hoch

Birmingham, Bristol, Edinburgh, FBK, Heidelberg, Hochschule RheinMain, IHEP, KIT, Lancaster, Milano, Pisa, Torino, Trento

- P.I. Attilio Andreazza (Milan), Yanyan Gao (Edinburgh)
- See presentation by A. Andreazza at the DRD3 week in Amsterdam https://indico.cern.ch/event/1507215/contributions/6540418/
- Project goals

FCC

- Demonstrate the operation of a CMOS based multi-chip module SP chain in realistic environment
- Explore high density low mass aluminium flex PCB production and innovative interconnections, to reduce
- Case study: long staves for the Silicon Wrapper

#### Distribution of power and data signals along the local supports

- serial powering to reduce dissipation on the distribution lines
- minimize the number of connections

#### Read-out units are:

- multi-chip modules (example 2x2 quad modules)
- (or large stitched detectors)

#### Minimal I/O connection on chip requires:

- Serial powering chain: all biases generated internally by shunt-LDO regulators
  - 1 LV and 1 HV line per "stave"
- chip-to-chip data transmissions: local data aggregation on module
  - 1 data-out per "module"
- LVDS module configuration with clock data recovery
  - 1 data-in per module
- No current detector providing all these features Reducing material by developing PCB with Al as conductor



### Steps

- Assemble 3 modules with ATLASPix3.1 on a bus to test serial powering
- Mount and power modules on a long (1330 mm) stave fabricated in Pisa
- Produce a second larger (2 or 4 cm2) in Lfoundry 150 nm with suitable components not available or not tested on ATLASPix
- clock data recovery , chip-to-chip data handling
- Develop low-mas Aluminium (20 μm)-Kapton(25 μm)
  PCBs
- Mount and power modules on a long stave





# Time line

Deliverable	Timeline
Multi-chip module construction and readout (ATLASPix3.1)	06/2025
Al-flex production for ATLASPix3.1 power bus	09/2025
ATLASPix-based SP chain prototype construction and characterisation	03/2026
Submission and production of new CMOS sensors (LF)	07/2025- 03/2026
Multi-chip readout flex submission for the LF CMOS sensors	12/2026
Multi-chip LF module construction and readout	03/2027
Al-flex production for the LF CMOS sensors	09/2027
LF sensors based SP chain prototype construction	01/2028
LF sensors based SP chain prototype evaluation	03/2028

### **Conclusions and perspectives**

- Vertex design activities ongoing
- First study of the services
- **R&D** launched for a serial powering and flex demonstrator