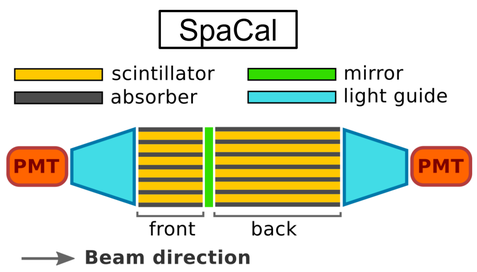
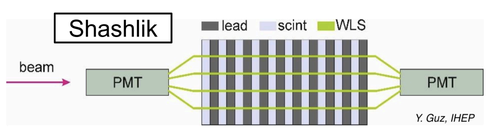
The ICECAL65: an Energy Measurement ASIC for the Upgrade II in the LHCb Calorimeter Detector

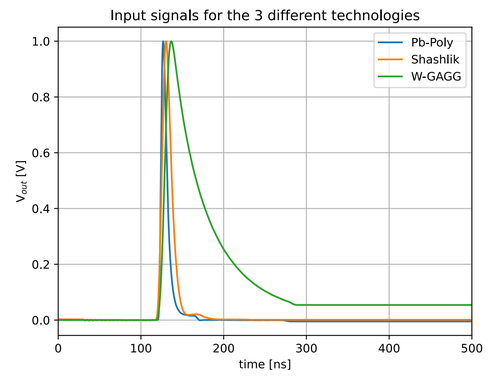
A. López, D. Marín, J. Serrano, E. Barajas, X. Aragonés, D. Peña, J. Altet, S. Gómez, E.Picatoste

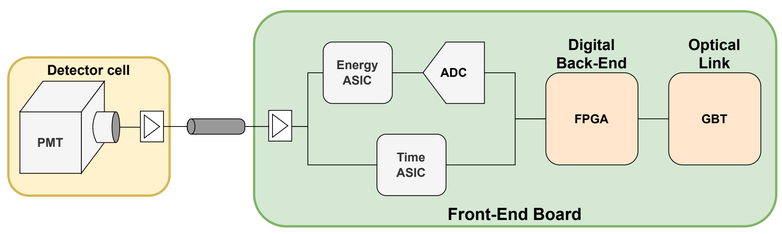
Institut de Ciències del Cosmos de la Universitat de Barcelona (ICCUB) and Universitat Politècnica de Catalunya (UPC)

LHCb Calorimeter Detector Upgrade II





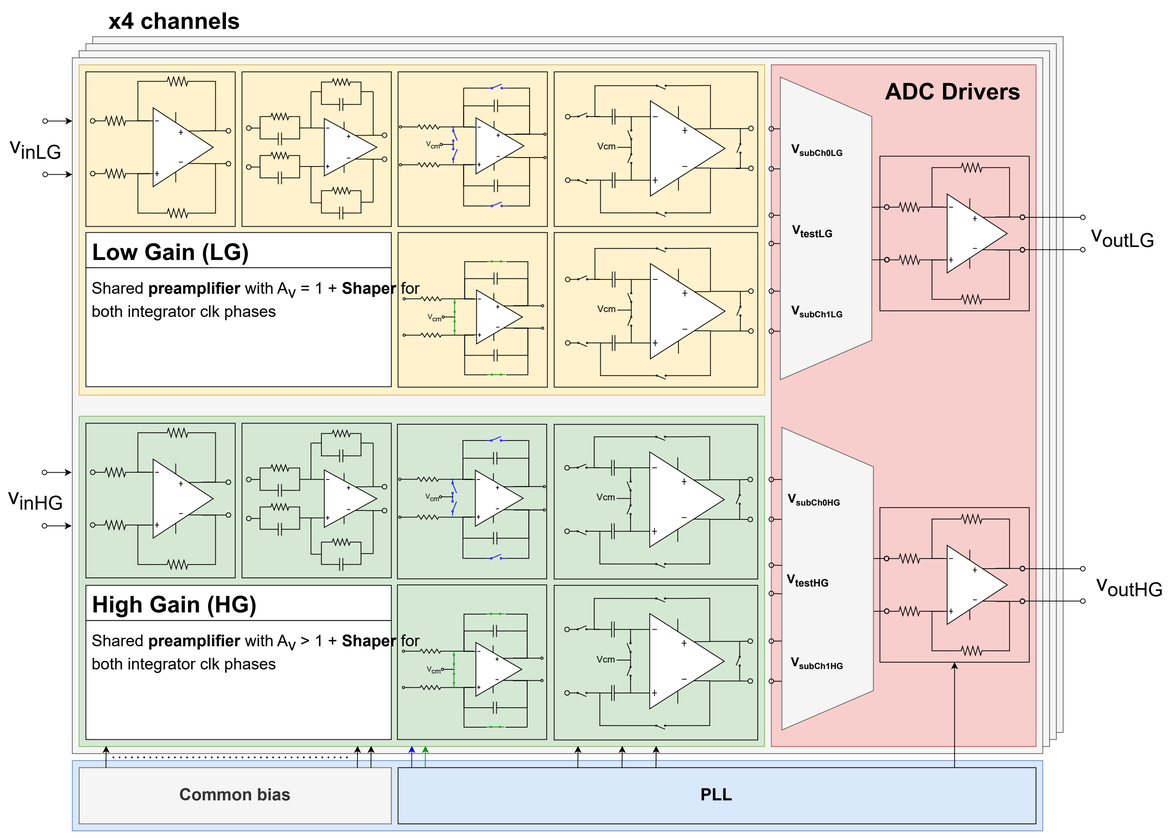




Detector technology	SpaCal	SpaCal	Shaslik
Absorber	Tungsten (W)	Lead (Pb)	Lead (Pb)
Scintillator/fibres	GAGG	Polystyrene	Scintillator/YS4 fibres
Cell size	1.5 x 1.5 cm^2	3 x 3 cm^2	4 x 4 cm^2

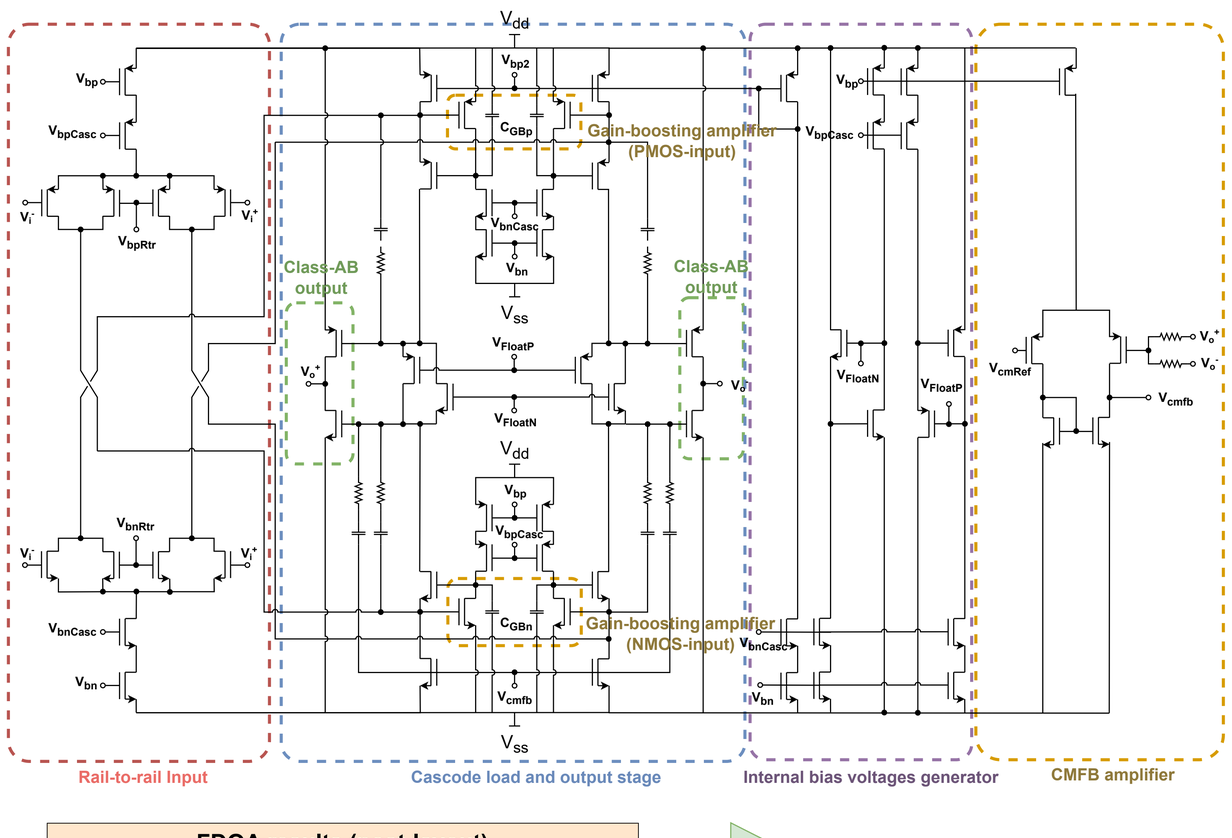
- **ECAL** intended to measure the energy (**ICECAL65**) and time of arrival (**SPIDER**) of photoelectrons.
- Photoelectroncs generated with **3 different scintillator detectors** (W-Poly, Shashlik and W-GAGG).
- Photodetection performed using Photomultipliers (**PMTs**).

Channel Architecture

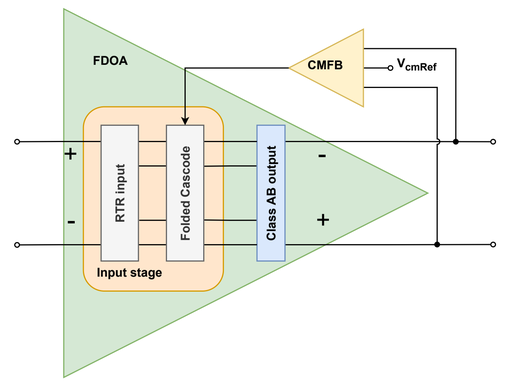


- TSMC 65 nm **4-channel** ASIC.
- **Two-gain** system to achieve the required **12-bit** resolution.
  - 11-bit resolution per gain path. Dynamic range 1 V and **noise/LSB ~ 500 µV.**
- Time-interleaved double channel for **continuous readout at 40 MHz** transmission.
- **Fully-differential** to improve noise rejection.
- Clks individually generated per channel using a PLL.
  - 20 MHz clks for channel blocks and 40 MHz clks for external ADCs.
- Output buffer drive capability up to **10 pF**.
- Power consumption **~ 50 mW/channel**.

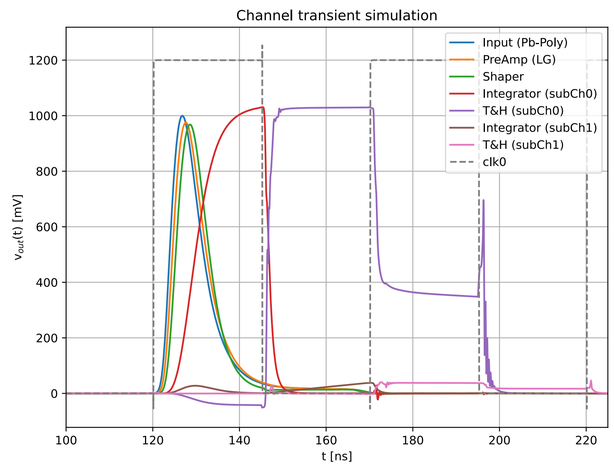
Fully-Differential Operational Amplifier (FDOA)



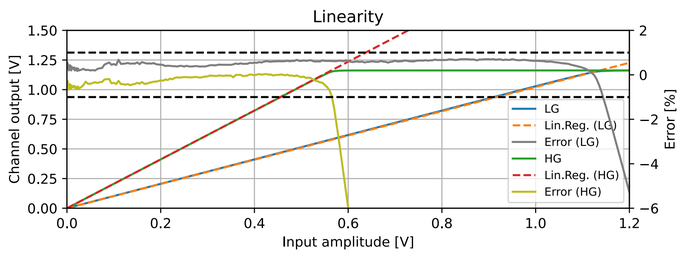
FDOA results (post-layout)		
Specification	**Channel FDOA**	**Driver FDOA**
A_{v0} (dB)	85.59	81
GBW (MHz)	524.9	293.2
Phase margin (º)	70.4	65.67
Slew-rate (V/µs)	641.4	366.1
Noise @ 1Mhz - 1 GHz [μV_{rms}]	317.1	250.2
PSRR @ mismatch [dB]	67.34	66.08
Power (mW)	3.576	10.07

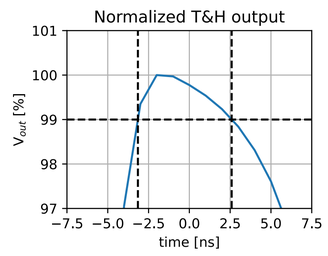


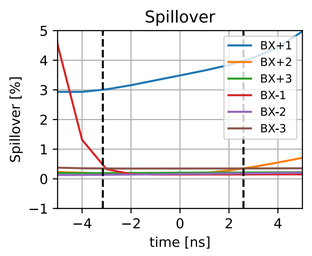
Channel Transient simulation and performance



- Pole-zero shaper with adjustable RCs to cope with:
  - **Channel technology** (SpaCal, W+Crystal, Pb-Poly, and Shaslik).
  - **PMT variations**.
- Integrator with variable C for gain adjustment.
- Track & Hold with **high slew-rate** to ensure the correct ADC performance.

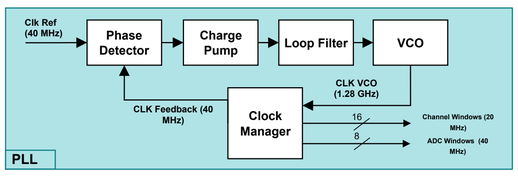






- Linearity error **< 1 %**
- Plateau > **+- 2ns**
- Maximum spillover **~ 3%**
- Transient noise at T&H output **σ ~ 500 uV.**
  - Maximum for 11-bit resolution.

PLL



- Channel clks **individually** generated with a PLL.
- Window resolution of **781 ps**.
- **Triple voting PFD** for robustness against radiation.

Additional features

- System includes a **Power on Reset** (PoR) to guarantee the correct start-up
- **Pulse injector** for testing porpuses.
- Monitoring and debugging outputs.
- Slow control using an **I2C** protocol.

Conclusions and next steps

- PCB test + **verification** of a 4-channel version of the ASIC expected in **February** after recent tape-out submission (October 2025).
- Expected to be extended to **8 channels** in the next version of the ASIC.
- **On-chip ADC** is being considered to be included for the ICECAL65 v2.

References

[1] LHCb collaboration, Framework TDR for the LHCb Upgrade II: Opportunities in flavour physics, and beyond, in the HL-LHC era, Tech. Rep. CERN-LHCC-2021-012, LHCB-TDR-023, CERN, Geneva (2021).
[2] R. Hogervorst, J.P. Tero, R.G.H. Eschauzier, and J.H. Huijsing. A compact power-efficient 3V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries IEEE Journal of Solid-State Circuits, 29(12):1505–1513, 1994.
[3] C. D. Matthus, S. Buhr, M. Kreißig and F. Ellinger, "High Gain and High Bandwidth Fully Differential Difference Amplifier as Current Sense Amplifier," in IEEE Transactions on Instrumentation and Measurement, vol. 70, pp. 1-11, 2021, Art no. 2000911

Acknowledgements:Grant M2RN002806 MIN/ PID2022-139842NB-C21 funded by MICIU/AEI/ 10.13039/501100011033, as appropriate, by the "European Union NextGenerationEU/PRTR" and by Generalitat de Catalunya.

International Workshop on New Photon-Detectors PD2025

Contact: alopezguillen@ub.edu