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Enabling photon detection: the role of ASICs

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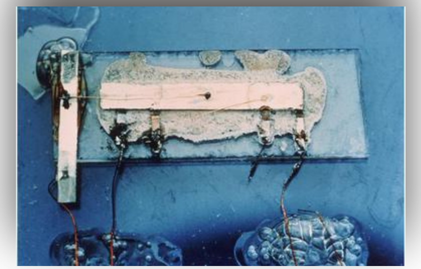
Introduction

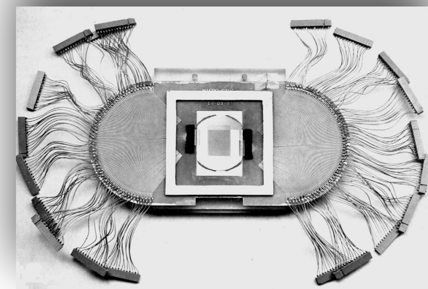
- Focus on ASICs for hybrid single photon detectors
- A look at where we are
- A guess on possible next steps

Toward ASICs for single photon detectors

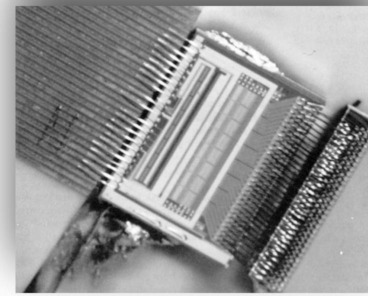
First IC (1958)



NA11 micro-vertex (1983)



First IC for vertex detectors (1984)



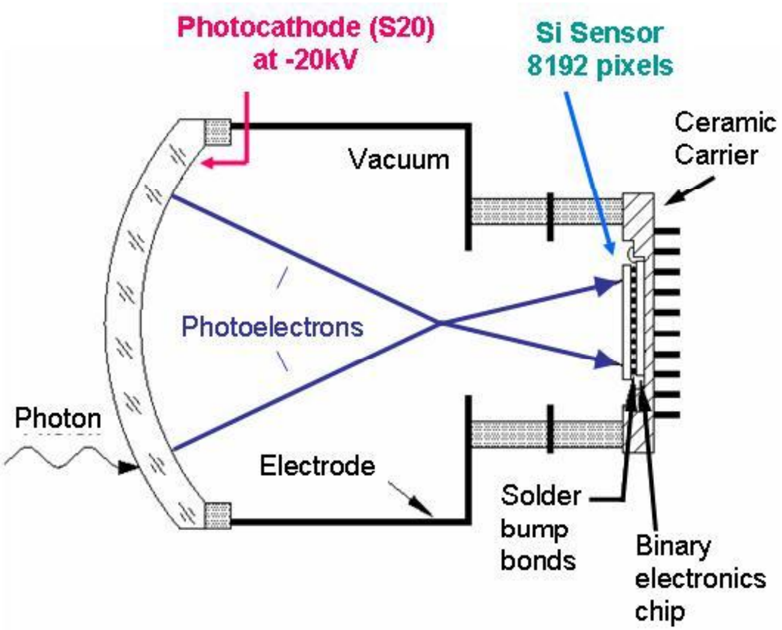
Earliest paper found on IEEExplore looking for “ASICs” + “PMT”

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 38, NO. 2, APRIL 1991 135

Readout Electronics of Multi-Anode Photomultiplier Tubes for Scintillation Fiber Calorimeter

Hirokazu IKEDA, Mitsuo IKEDA, Susumu INABA,
Fumihiko TAKASAKI, and Manobu TANAKA
National Laboratory for High Energy Physics
1-1 Oho, Tsukuba, 305 Japan

An early example of high density read-out



Single HPD. Ruler is 10cm long

- **The advent of SiPM attracted a lot of attention (and design resources…)**

Ten years of ASICs used with SiPMs

ASIC	# ch	CMOS node	On-chip TDC (LSB)	On-chip ADC / Energy meas.	Power / ch (approx.)
TOFPET2	64	110 nm	30 ps	QDC + ToT	~8.2 mW/ch
PETIROC 2A	32	350 nm	40 ps	10-bit ADC	~6 mW/ch
TEMPOROC 2	64	130 nm	20 ps rms	Dual ADC per channel	~5 mW/ch
ALCOR	32–64	110 nm	25–50 ps	ToT / slew-rate	~10–12 mW/ch
FastIC+	8	65 nm	24.4 ps	ToT-based energy, digital modes	1.8–12.5 mW/ch
BETA	16–64	130 nm	Comparator only (~400 ps)	12-bit Wilkinson ADC (HG/LG)	~1–1.4 mW/ch
PETA5	36	180 nm	50 ps	Amplitude integration + ADC	30 mW/ch
PETAT	32	180 nm	Yes (time-stamping)	Amplitude measurement on chip	13 mW/ch
MIZAR	64	65 nm	No (waveform sampling)	12-bit Wilkinson ADC per cell	~5 mW/ch
CASTOR	1	110 nm	No	Cryogenic AFE	20 mW/ch

Ten years of ASICs used with MCP

ASIC	Type	Channels/Pixels	Sampling / Timing
Timepix4	Hybrid pixel (ToA/ToT)	512×448 pixels	195 ps bins (~5.1 GHz equiv.)
MIRA	Pixelated MCP readout	32×32 = 1024	133/280 ns shaping
GRAPH	Waveform sampler	16	Up to 125 MHz, 12-bit, 2048 samples
PSEC−4	Waveform sampler	6	4–15 GSa/s
DRS4	Waveform sampler	8 (+1)	0.7–5 GSa/s
SAMPIC	Waveform + TDC	16	0.8–8.5 GSa/s

Ten years of ASICs used with PMTs

ASIC	Channels	Application Focus	Key Features
MAROC3A	64	Multi-anode PMTs	Gain equalization, fast discriminator, Wilkinson ADC
CATIROC	16	Large PMTs (Neutrino/ Cherenkov)	Self-trigger, 10-bit ADC, time+charge readout
PARISROC	16	PMT arrays (Neutrino)	Variable gain, charge ADC, coarse+fine timing
HKROC	~16–32	Hyper-Kamiokande PMTs	Low-noise FE, SAR ADC, integrated TDC
SIPHRA (IDE3380)	16 + sum	PMTs/SiPMs (Space, Lab)	Spectroscopy + timing, programmable shaping
APOCAT (IDE3381)	16	High-rate photon counting	ADC + counters, rad-hard
LHAASO PMT FE ASIC	1 per PMT	Cherenkov Water Detector Array	Wide dynamic range, analog shaping
PROMiS (KM3NeT)	1 per PMT	Deep-sea neutrino telescope	Low-noise FE, LVDS timing outputs
QTC ASIC (Super-K)	1	Water Cherenkov PMTs	Charge-to-time conversion

Disclaimer: the lists in slide 5-7 are meant to be representative, but not exhaustive!
If your ASIC is not there blame AI…

Key inputs from the tables

- Two broad family of ASICs
  - On board direct extractor of key features
  - Waveform samplers
- Key onboard IPs: ADCs, TDCs, PLLs, Serializers
- Moderate channel number (< 64)
- Good timing resolution required in most cases

Key inputs from the tables

- Technology node O(130 nm) turned out to be a "sweet spot"
  - Fair digital gate density
  - Good analogue performance and design flexibility
  - Manageable cost

ASICs

9 leading ASIC manufacturing foundries with technologies ranging from 0.35 µm to 7 nm

The role of ASICs in photon detection

- Rather than enabling photon-detection per se, ASICs are fundamental to enable practical, large photon detection systems
- Sometimes even single channel integration can make a difference
- High number of channels imply less power/channel, possibly limiting performance w.r.t. off-the-shelf components
- Targeting the same performance of off-the shelf components can be misleading

Typical questions

- When can we have a fully digital waveform sampler? (Optimal would be 12 bits, 1-10 GS/s …)
- Can we have better TDC resolution?
- Why don’t we move to more aggressively scaled nodes?
- Where can we improve our chips/systems?

When can we have a fully digital waveform sampler?

- **Reality check: 12 bits, 1 GS/s, 64 channels: 768 Gb/s: 0.15 W/channel only to send - out data … forget about!**

PRESS RELEASES

MaxLinear announces 5nm CMOS PAM4 DSP with integrated VCSEL drivers for 800G and 400G Multimode short-reach optical modules and Active Optical Cables (AOC)

☐ September 28, 2023

- Providing cost-optimized, best-in-class power consumption of <10W for 800G short reach links in datacenters and AI/ML cluster applications.
- The active optical cable market is projected to be $19 billion by 2030.

Marvell Announces Industry's First 5nm Transmit-Only 800G PAM4 Optical DSP for AI and Cloud Interconnects

Spica Gen2-T adds to the Marvell industry-leading portfolio of 800 Gbps DSPs, the most widely deployed optical DSPs in cloud data centers and AI clusters.

When can we have a fully digital waveform sampler?

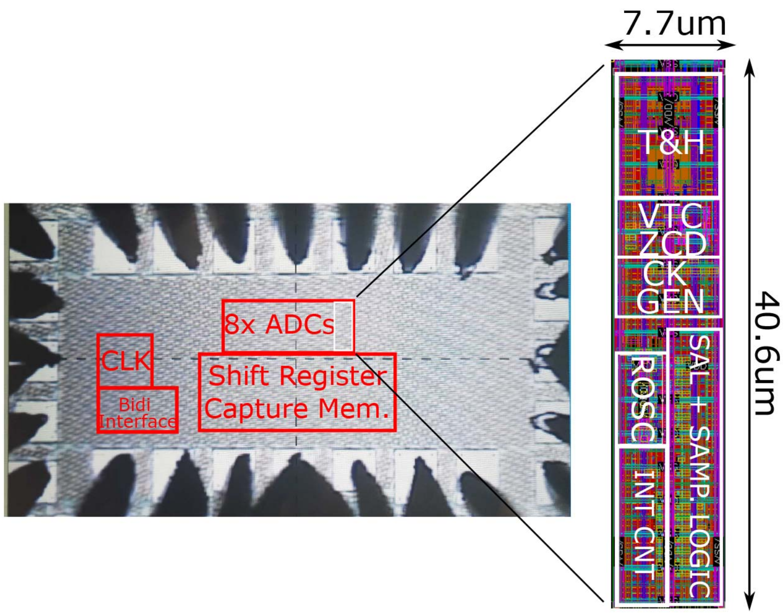
- On chip data decimation always necessary. But doing it in digital can be a very good idea:
  - UDSM technologies optimize digital performance and power consumption/function
  - 130 millions transistors/mm2 in 5 nm…
  - Software defined signal processing
- The critical block here is the ADC

A look at state of the art ADC

IEEE SOLID-STATE CIRCUITS LETTERS, VOL. 6, 2023 193

An 8b 1.0-to-1.25 GS/s Time-Based ADC With Bipolar VTC and Sense Amplifier Latch Interpolated Gated Ring Oscillator TDC

A. Serdar Yonar, *Graduate Student Member, IEEE*, Pier Andrea Francese, *Senior Member, IEEE*, Matthias Brändli, *Member, IEEE*, Marcel Kossel, *Senior Member, IEEE*, Mridula Prathapan, *Member, IEEE*, Thomas Morf, *Senior Member, IEEE*, Andrea Ruffino, *Member, IEEE*, Gain Kim, *Member, IEEE*, and Taekwang Jang, *Senior Member, IEEE*



5-nm CMOS
8 bit
1.18 mW@1Gb/s
1.9 mW@1.25 Gb/s

State of the art ADC with better performance

A 12-bit 10GS/s Time-Interleaved SAR ADC with Even/Odd Channel-Correlated Absolute Error-Based Over-Nyquist Timing-Skew Calibration in 5nm FinFET

Junsang Park, Jinwoo Park, Jaemin Hong, Sunjae Park, Dongsuk Lee, Sungno Lee, Hyochul Shin, Kyunghoon Lee, Byeongwoo Koo, Youngjae Cho, Michael Choi, and Jongshin Shin
Samsung Electronics, Hwaseong-City, Gyeonggi-Do, South Korea, Email: junsg.park @samsung.com

TABLE I
PERFORMANCE SUMMARY AND COMPARISION

		This Work		ISSCC 2023 [1]	ISSCC 2020 [2]	ISSCC 2017 [3]	VLSI 2022 [4]
Technology		5nm FinFET		7nm FinFET	16nm FinFET	28nm FDSOI	5nm FinFET
Architecture		TI-SAR		TI-SAR	TI-Pipeline	TI-Pipeline	TI-Pipeline
Resolution		12		12	12	12	12
Fs [GS/s]		10		24	18	10	10
Fin [GHz]		5	9	7.24	8	4	5
SNDR at Fin [dB]		50.2	46.2	46.5	48	55	48
SFDR at Fin [dB]		61.2	60.0	76	54	64	61
Input	2nd Nyquist	O		-	O	-	-
	TDD	O		-	-	-	-
Power [W]		0.386		0.75	1.3	2.9	0.625
Area [mm^2]		0.71		0.9	2.6	7.4	2.1
FoM_{walden} (1) [fJ/step]		146.0		181	351.9	631.2	305
$FoM_{Schreier}$ (2) [dB]		151.3		148.5	146.4	147	147

Older ADC performance

322 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 55, NO. 2, FEBRUARY 2020

A Temperature-Stabilized Single-Channel 1-GS/s 60-dB SNDR SAR-Assisted Pipelined ADC With Dynamic Gm-R-Based Amplifier

Wenning Jiang, *Student Member, IEEE*, Yan Zhu, *Member, IEEE*, Minglei Zhang, *Member, IEEE*, Chi-Hang Chan, *Member, IEEE*, and Rui Paulo Martins, *Fellow, IEEE*

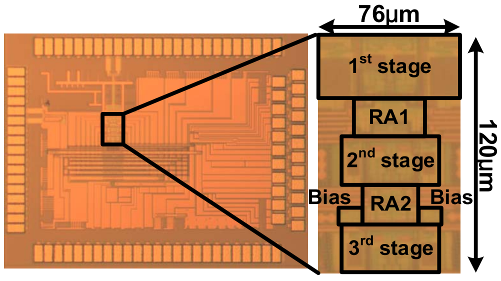


TABLE II
ADC PERFORMANCE SUMMARY AND COMPARISON

	This work	VLSI 2017[16] K.-J. Moon	JSSC 2018[3] R. Sehgal	ISSCC 2017[9] L. Kull	ISSCC 2017[17] H. Huang	ISSCC 2019[25] B. Hershberg	JSSC 2019[4] J. Lagos
Architecture	Pipelined SAR	Pipelined SAR	Pipeline	Pipelined SAR	Pipelined SAR	Pipeline	Pipeline
Residue Amplifier	Open-loop Gm-R	gm-cell	Open-loop Integrator	CML Amplifier	Dynamic Amplifier	Ring Amplifier	Ring Amplifier
Technology	28nm	28nm	28nm	14nm	65nm	16nm	28nm
Resolution [bits]	12	10	12	10	12	11	12
Sample Rate [MS/s]	1000	500	280	1500	330	600	1000
Supply Voltage [V]	1	1	1	0.95	1.3	0.85	0.9
SFDR @Nyq. [dB]	74.56	69.2	77	58.39	75.8	78.3	73.1
SNDR @Nyq. [dB]	60.02	56.6	64	50.1	63.5	60.2	56.6
Power [mW]	7.6	6	13	6.92*	6.2	6.0	24.8
FoM_{Walden} @Nyq. [fJ/conv-step]	9.28	21.7	35.8	17.7*	15.4	12	45
$FoM_{Schreier}$ @Nyq. [dB]	168.2	162.8	164.3	160.5*	167.8	167.2	159.6
Area [mm^2]	0.0091	0.015	0.22	0.0016	0.08	0.037	0.54

* including the reference buffer

When can we have a fully digital waveform sampler?

- **With pure data-push architecture: not in the foreseeable future**
- **With sampling rate < 1 Gs/s and resolution < 10 bits: possible already in 28 nm. More aggressively scaled technologies will improve mainly on digital**
- **For higher resolution and/or sampling speed…stay with old fashion analogue memories…**

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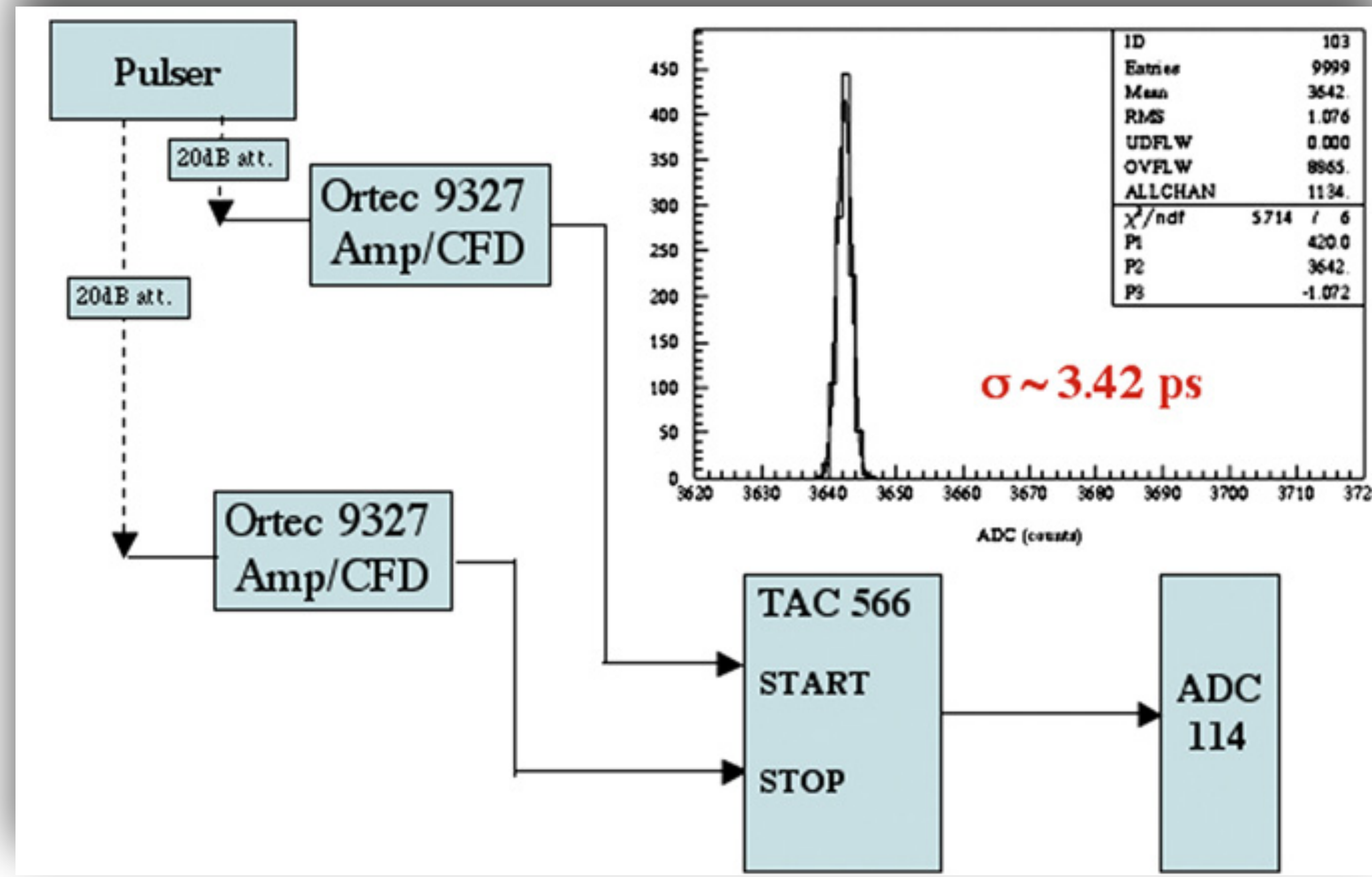
Can we have better TDC performance?

Year	Technology	Architecture	Measured Resolution	Notes
2025	130 nm CMOS	Dual-phase oscillator analog sampling	0.79–0.9 ps RMS	Scalable, low power (~4.1 mW/ch)
2015	65 nm CMOS	Charge pump + SAR ADC (time-to-charge)	0.80–0.84 ps RMS	Two prototype chips validated
2012	0.18 µm CMOS	Differential pulse-shrinking buffer ring	580 fs LSB	9-bit range; measured silicon
2008	0.13 µm CMOS	Flash TDC with multi-comparator front-end	0.6 ps resolution	Measured maximum resolution
2016	45 nm FPGA	Multiedge coding in independent lines	902 fs equivalent	FPGA-based but experimentally verified

- **Timing resolution defined by the interplay between the sensor and the front-end**

Timing with 60 years old technology



Why we don't move to finer technologies (and what would we gain?)

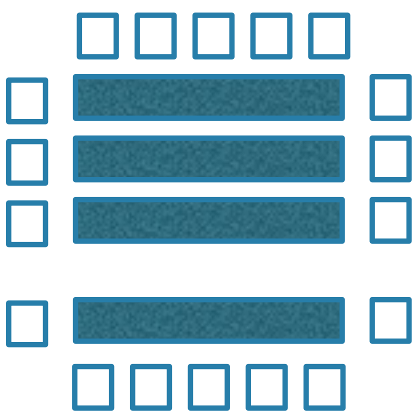
- Costs
- Design time
- Design complexity
- Clear gain on digital
- Smaller area
- No major gain in analogue performance
- 28 nm is a legacy technology as well…

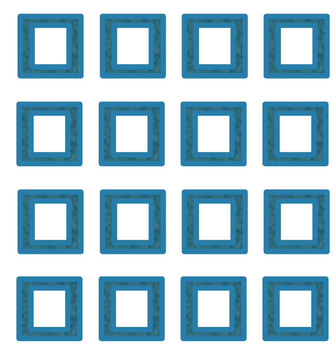
Where can we improve?

- ASICs performance often are not limited by the fundamental noise floor
  - Bugs in data path/control logic
  - Cross-talk due to shared bias lines
  - Overlooked parasitic capacitance/resistance
  - IR drops
  - Wire-bond inductance

Where can we improve?

- ASICs performance often are not limited by the fundamental noise floor
  - Better verification frameworks
  - On chip improved power management
  - Estensive Package/board level simulations
  - Better channel arrangement + use of CSP and WLCSP packaging





Concluding remarks

- ASICs are indispensable tools to provide practical, medium-to-large scale photon detection systems
- They performance is often limited by implementation pitfall that can be prevented with adequate simulations
- Avoid too many prototyping cycles
- More scaled technologies offer room for improvements, in particular in digital power reduction and circuit density, but do not expect miracles
- Cryogenic electronics is adding additional complexity