A1

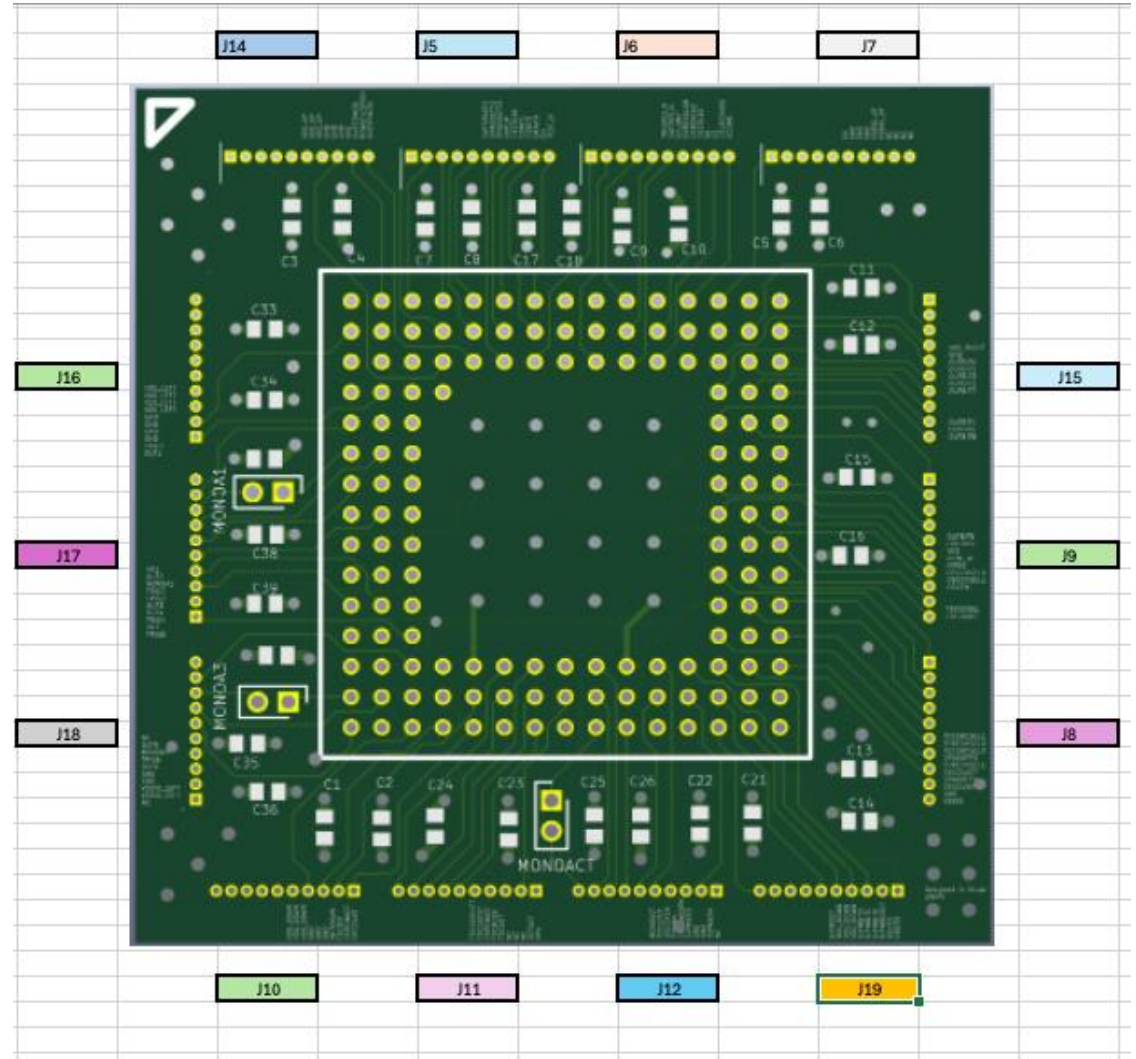
NAME	CONN	N_PIN	N_CONN
TDCRESET_N	J10	51	13
VDD_DOWN	J10		
TDCOUT	J11		
TDCCKSHIFT	J11		
TDCCKEXT	J11		
VDD_UP	J14		
TDCIN4	J12		
TDCLOCK	J12		
VDD_LEFT	J16		
TRIG1	J16		
OUT1	J16		
GND	J16		
VDD_RIGHT	J15		
TRIG2	J17		
OUT2	J17		
TRIG3	J17		
OUT3	J17		
TRIG4	J17		
OUT4	J17		
MONOA1	J17		
VK1	J17		
VDDIO_LEFT	J18		
VDD33	J19		
GND33	J19		
EN	J5		
TEST_N	J5		
DATATX	J5		
CONF0	J5		
CONF1	J5		
CKCOLA1	J5		
VCCLAMP	J6		
VB	J6		
S1	J6		
VCONN	J6		
CELLRESMOD	J6		
ENRESGLOB_N	J6		
TRIGRES_N	J6		
OUTRES_N	J6		
INITUP	J6		
CKROWA1A2	J6		
VDDIO_UP	J7		
S0	J7		
TDCSRCSEL0	J8		
TDCSRCSEL1	J8		
TDCCKSEL	J8		
TDC20BIT	J8		
TDCMODE	J8		
OSCEN	J8		
OSCCKSEL1	J8		
OSCCKSEL0	J8		
VDDIO	J8		

A2

NAME	CONN	N_PIN	N_CONN
VDD_DOWN	J10	38	11
VDD_UP	J14		
OUTBIT0	J15		
OUTBIT1	J15		
OUTBIT2	J15		
OUTBIT3	J15		
OUTBIT4	J15		
OUTBIT6	J15		
OUTBIT7	J15		
OUTBIT8	J15		
VDD_RIGHT	J15		
GND	J15		
VDD_LEFT	J16		
VDDIO_LEFT	J18		
VDD33	J19		
GND33	J19		
EN	J5		
TEST_N	J5		
DATATX	J5		
CONF0	J5		
CONF1	J5		
VCLAMP	J6		
VB	J6		
S1	J6		
VCONN	J6		
CELLRESMOD	J6		
ENRESGLOB_N	J6		
CKROWA1A2	J6		
CKCOLA2	J6		
INITUP	J6		
S0	J7		
VDDIO_UP	J7		
VDDIO	J8		
VK2	J9		
INTEG	J9		
RCNT_N	J9		
OUTBIT5	J9		
OUTBIT9	J9		

A3

NAME	CONN	N_PIN	N_CONN
INITDOWN	J10	44	12
CKCOLA3	J10		
TDCRESET_N	J10		
VDD_DOWN	J10		
CKROWA3	J11		
TDCOUT	J11		
TDCCKSHIFT	J11		
TDCCKEXT	J11		
TDCIN4	J12		
TDCLOCK	J12		
VDD_UP	J14		
VDD_RIGHT	J15		
GND	J15		
VDD_LEFT	J15		
TRIG5	J17		
VK3	J17		
OUT5	J18		
TRIG6	J18		
OUT6	J18		
MONOA3	J18		
VDDIO_LEFT	J18		
VDD33	J19		
GND33	J19		
EN	J5		
TEST_N	J5		
DATATX	J5		
VCLAMP	J6		
VB	J6		
VCONN	J6		
CELLRESMOD	J6		
ENRESGLOB_N	J6		
TRIGRES_N	J6		
OUTRES_N	J6		
VDDIO_UP	J7		
S0	J7		
TDCSRCSEL0	J8		
TDCSRCSEL1	J8		
TDCCKSEL	J8		
TDC20BIT	J8		
TDCMODE	J8		
OSCEN	J8		
OSCCKSEL1	J8		
OSCCKSEL0	J8		
VDDIO	J8		



A1

NAME	CONN	N_PIN	N_CONN
TDCRESET_N	J10	51	13
VDD_DOWN	J10		
TDCOUT	J11		
TDCCKSHIFT	J11		
TDCCKEXT	J11		
VDD_UP	J14		
TDCIN4	J12		
TDCLOCK	J12		
VDD_LEFT	J16		
TRIG1	J16		
OUT1	J16		
GND	J16		
VDD_RIGHT	J15		
TRIG2	J17		
OUT2	J17		
TRIG3	J17		
OUT3	J17		
TRIG4	J17		
OUT4	J17		
MONOA1	J17		
VK1	J17		
VDDIO_LEFT	J18		
VDD33	J19		
GND33	J19		
EN	J5		
TEST_N	J5		
DATATX	J5		
CONF0	J5		
CONF1	J5		
CKCOLA1	J5		
VCCLAMP	J6		
VB	J6		
S1	J6		
VCONN	J6		
CELLRESMOD	J6		
ENRESGLOB_N	J6		
TRIGRES_N	J6		
OUTRES_N	J6		
INITUP	J6		
CKROWA1A2	J6		
VDDIO_UP	J7		
S0	J7		
TDCSRCSEL0	J8		
TDCSRCSEL1	J8		
TDCCKSEL	J8		
TDC20BIT	J8		
TDCMODE	J8		
OSCEN	J8		
OSCCKSEL1	J8		
OSCCKSEL0	J8		
VDDIO	J8		

A2

NAME	CONN	N_PIN	N_CONN
VDD_DOWN	J10	38	11
VDD_UP	J14		
OUTBIT0	J15		
OUTBIT1	J15		
OUTBIT2	J15		
OUTBIT3	J15		
OUTBIT4	J15		
OUTBIT6	J15		
OUTBIT7	J15		
OUTBIT8	J15		
VDD_RIGHT	J15		
GND	J15		
VDD_LEFT	J16		
VDDIO_LEFT	J18		
VDD33	J19		
GND33	J19		
EN	J5		
TEST_N	J5		
DATATX	J5		
CONF0	J5		
CONF1	J5		
VCLAMP	J6		
VB	J6		
S1	J6		
VCONN	J6		
CELLRESMOD	J6		
ENRESGLOB_N	J6		
CKROWA1A2	J6		
CKCOLA2	J6		
INITUP	J6		
S0	J7		
VDDIO_UP	J7		
VDDIO	J8		
VK2	J9		
INTEG	J9		
RCNT_N	J9		
OUTBIT5	J9		
OUTBIT9	J9		

A3

NAME	CONN	N_PIN	N_CONN
INITDOWN	J10	44	12
CKCOLA3	J10		
TDCRESET_N	J10		
VDD_DOWN	J10		
CKROWA3	J11		
TDCOUT	J11		
TDCCKSHIFT	J11		
TDCCKEXT	J11		
TDCIN4	J12		
TDCLOCK	J12		
VDD_UP	J14		
VDD_RIGHT	J15		
GND	J15		
VDD_LEFT	J15		
TRIG5	J17		
VK3	J17		
OUT5	J18		
TRIG6	J18		
OUT6	J18		
MONOA3	J18		
VDDIO_LEFT	J18		
VDD33	J19		
GND33	J19		
EN	J5		
TEST_N	J5		
DATATX	J5		
VCLAMP	J6		
VB	J6		
VCONN	J6		
CELLRESMOD	J6		
ENRESGLOB_N	J6		
TRIGRES_N	J6		
OUTRES_N	J6		
VDDIO_UP	J7		
S0	J7		
TDCSRCSEL0	J8		
TDCSRCSEL1	J8		
TDCCKSEL	J8		
TDC20BIT	J8		
TDCMODE	J8		
OSCEN	J8		
OSCCKSEL1	J8		
OSCCKSEL0	J8		
VDDIO	J8		

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A1

NAME	CONN	N_PIN	N_CONN
TDCRESET_N	J10	51	13
VDD_DOWN	J10		
TDCOUT	J11		
TDCCKSHIFT	J11		
TDCCKEXT	J11		
VDD_UP	J14		
TDCIN4	J12		
TDCLOCK	J12		
VDD_LEFT	J16		
TRIG1	J16		
OUT1	J16		
GND	J16		
VDD_RIGHT	J15		
TRIG2	J17		
OUT2	J17		
TRIG3	J17		
OUT3	J17		
TRIG4	J17		
OUT4	J17		
MONOA1	J17		
VK1	J17		
VDDIO_LEFT	J18		
VDD33	J19		
GND33	J19		
EN	J5		
TEST_N	J5		
DATATX	J5		
CONF0	J5		
CONF1	J5		
CKCOLA1	J5		
VCCLAMP	J6		
VB	J6		
S1	J6		
VCONN	J6		
CELLRESMOD	J6		
ENRESGLOB_N	J6		
TRIGRES_N	J6		
OUTRES_N	J6		
INITUP	J6		
CKROWA1A2	J6		
VDDIO_UP	J7		
S0	J7		
TDCSRCSEL0	J8		
TDCSRCSEL1	J8		
TDCCKSEL	J8		
TDC20BIT	J8		
TDCMODE	J8		
OSCEN	J8		
OSCCKSEL1	J8		
OSCCKSEL0	J8		
VDDIO	J8		

A2

NAME	CONN	N_PIN	N_CONN
VDD_DOWN	J10	38	11
VDD_UP	J14		
OUTBIT0	J15		
OUTBIT1	J15		
OUTBIT2	J15		
OUTBIT3	J15		
OUTBIT4	J15		
OUTBIT6	J15		
OUTBIT7	J15		
OUTBIT8	J15		
VDD_RIGHT	J15		
GND	J15		
VDD_LEFT	J16		
VDDIO_LEFT	J18		
VDD33	J19		
GND33	J19		
EN	J5		
TEST_N	J5		
DATATX	J5		
CONF0	J5		
CONF1	J5		
VCLAMP	J6		
VB	J6		
S1	J6		
VCONN	J6		
CELLRESMOD	J6		
ENRESGLOB_N	J6		
CKROWA1A2	J6		
CKCOLA2	J6		
INITUP	J6		
S0	J7		
VDDIO_UP	J7		
VDDIO	J8		
VK2	J9		
INTEG	J9		
RCNT_N	J9		
OUTBIT5	J9		
OUTBIT9	J9		

A3

NAME	CONN	N_PIN	N_CONN
INITDOWN	J10	44	12
CKCOLA3	J10		
TDCRESET_N	J10		
VDD_DOWN	J10		
CKROWA3	J11		
TDCOUT	J11		
TDCCKSHIFT	J11		
TDCCKEXT	J11		
TDCIN4	J12		
TDCLOCK	J12		
VDD_UP	J14		
VDD_RIGHT	J15		
GND	J15		
VDD_LEFT	J15		
TRIG5	J17		
VK3	J17		
OUT5	J18		
TRIG6	J18		
OUT6	J18		
MONOA3	J18		
VDDIO_LEFT	J18		
VDD33	J19		
GND33	J19		
EN	J5		
TEST_N	J5		
DATATX	J5		
VCLAMP	J6		
VB	J6		
VCONN	J6		
CELLRESMOD	J6		
ENRESGLOB_N	J6		
TRIGRES_N	J6		
OUTRES_N	J6		
VDDIO_UP	J7		
S0	J7		
TDCSRCSEL0	J8		
TDCSRCSEL1	J8		
TDCCKSEL	J8		
TDC20BIT	J8		
TDCMODE	J8		
OSCEN	J8		
OSCCKSEL1	J8		
OSCCKSEL0	J8		
VDDIO	J8		

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