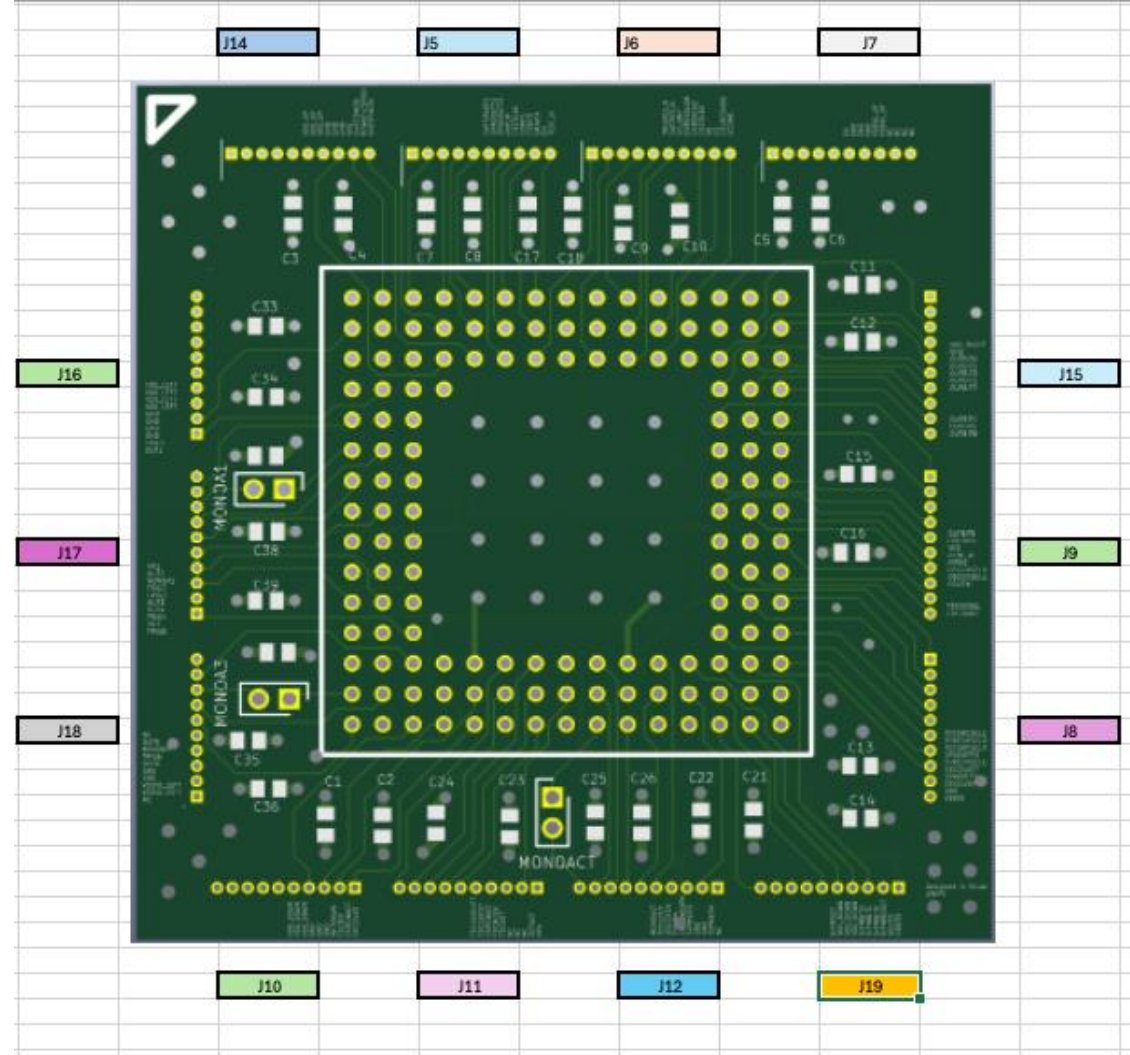


A1				A2				A3			
NAME	CONN	N_PIN	N_CONN	NAME	CONN	N_PIN	N_CONN	NAME	CONN	N_PIN	N_CONN
TDCRESET_N	J10	51	13	VDD_DOWN	J10	38	11	INITDOWN	J10	44	12
VDD_DOWN	J10			VDD_UP	J14			CKCOLA3	J10		
TDCOUT	J11			OUTBIT0	J15			TDCRESET_N	J10		
TDCKCKSHIFT	J11			OUTBIT1	J15			VDD_DOWN	J10		
TDCKCKEXT	J11			OUTBIT2	J15			CKROWA3	J11		
VDD_UP	J14			OUTBIT3	J15			TDCOUT	J11		
TDCIN4	J12			OUTBIT4	J15			TDCKCKSHIFT	J11		
TDLOCK	J12			OUTBIT6	J15			TDCKCKEXT	J11		
VDD_LEFT	J16			OUTBIT7	J15			TDCIN4	J12		
TRIG1	J16			OUTBIT8	J15			TDLOCK	J12		
OUT1	J16			VDD_RIGHT	J15			VDD_UP	J14		
GND	J16			GND	J15			VDD_RIGHT	J15		
VDD_RIGHT	J15			VDD_LEFT	J16			GND	J15		
TRIG2	J17			VDDIO_LEFT	J18			VDD_LEFT	J15		
OUT2	J17			VDD33	J19			TRIG5	J17		
TRIG3	J17			GND33	J19			VK3	J17		
OUT3	J17			EN	J5			OUT5	J18		
TRIG4	J17			TEST_N	J5			TRIG6	J18		
OUT4	J17			DATATX	J5			OUT6	J18		
MONOA1	J17			CONF0	J5			MONOA3	J18		
VK1	J17			CONF1	J5			VDDIO_LEFT	J18		
VDDIO_LEFT	J18			VCLAMP	J6			VDD33	J19		
VDD33	J19			VB	J6			GND33	J19		
GND33	J19			S1	J6			EN	J5		
EN	J5			VCONN	J6			TEST_N	J5		
TEST_N	J5			CELLRESMOD	J6			DATATX	J5		
DATATX	J5			ENRESGLOB_N	J6			VCLAMP	J6		
CONF0	J5			CKROWA1A2	J6			VB	J6		
CONF1	J5			CKCOLA2	J6			VCONN	J6		
CKCOLA1	J5			INITUP	J6			CELLRESMOD	J6		
VCCLAMP	J6			S0	J7			ENRESGLOB_N	J6		
VB	J6			VDDIO_UP	J7			TRIGRES_N	J6		
S1	J6			VDDIO	J8			OUTRES_N	J6		
VCONN	J6			VK2	J9			VDDIO_UP	J7		
CELLRESMOD	J6			INTEG	J9			S0	J7		
ENRESGLOB_N	J6			RCNT_N	J9			TDCSRCSEL0	J8		
TRIGRES_N	J6			OUTBIT5	J9			TDCSRCSEL1	J8		
OUTRES_N	J6			OUTBIT9	J9			TDCKCKSEL	J8		
INITUP	J6							TDC20BIT	J8		
CKROWA1A2	J6							TDCMODE	J8		
VDDIO_UP	J7							OSCEN	J8		
S0	J7							OSCKSEL1	J8		
TDCSRCSEL0	J8							OSCKSEL0	J8		
TDCSRCSEL1	J8							VDDIO	J8		
TDCKCKSEL	J8										
TDC20BIT	J8										
TDCMODE	J8										
OSCEN	J8										
OSCKSEL1	J8										
OSCKSEL0	J8										
VDDIO	J8										



A1				A2				A3			
NAME	CONN	N_PIN	N_CONN	NAME	CONN	N_PIN	N_CONN	NAME	CONN	N_PIN	N_CONN
TDCRESET_N	J10	51	13	VDD_DOWN	J10	38	11	INITDOWN	J10	44	12
VDD_DOWN	J10			VDD_UP	J14			CKCOLA3	J10		
TDCOUT	J11			OUTBIT0	J15			TDCRESET_N	J10		
TDCKCKSHIFT	J11			OUTBIT1	J15			VDD_DOWN	J10		
TDCKCKEXT	J11			OUTBIT2	J15			CKROWA3	J11		
VDD_UP	J14			OUTBIT3	J15			TDCOUT	J11		
TDCIN4	J12			OUTBIT4	J15			TDCKCKSHIFT	J11		
TDLOCK	J12			OUTBIT6	J15			TDCKCKEXT	J11		
VDD_LEFT	J16			OUTBIT7	J15			TDCIN4	J12		
TRIG1	J16			OUTBIT8	J15			TDLOCK	J12		
OUT1	J16			VDD_RIGHT	J15			VDD_UP	J14		
GND	J16			GND	J15			VDD_RIGHT	J15		
VDD_RIGHT	J15			VDD_LEFT	J16			GND	J15		
TRIG2	J17			VDDIO_LEFT	J18			VDD_LEFT	J15		
OUT2	J17			VDD33	J19			TRIG5	J17		
TRIG3	J17			GND33	J19			VK3	J17		
OUT3	J17			EN	J5			OUT5	J18		
TRIG4	J17			TEST_N	J5			TRIG6	J18		
OUT4	J17			DATATX	J5			OUT6	J18		
MONOA1	J17			CONF0	J5			MONOA3	J18		
VK1	J17			CONF1	J5			VDDIO_LEFT	J18		
VDDIO_LEFT	J18			VCLAMP	J6			VDD33	J19		
VDD33	J19			VB	J6			GND33	J19		
GND33	J19			S1	J6			EN	J5		
EN	J5			VCONN	J6			TEST_N	J5		
TEST_N	J5			CELLRESMOD	J6			DATATX	J5		
DATATX	J5			ENRESGLOB_N	J6			VCLAMP	J6		
CONF0	J5			CKROWA1A2	J6			VB	J6		
CONF1	J5			CKCOLA2	J6			VCONN	J6		
CKCOLA1	J5			INITUP	J6			CELLRESMOD	J6		
VCCLAMP	J6			S0	J7			ENRESGLOB_N	J6		
VB	J6			VDDIO_UP	J7			TRIGRES_N	J6		
S1	J6			VDDIO	J8			OUTRES_N	J6		
VCONN	J6			VK2	J9			VDDIO_UP	J7		
CELLRESMOD	J6			INTEG	J9			S0	J7		
ENRESGLOB_N	J6			RCNT_N	J9			TDCSRCSEL0	J8		
TRIGRES_N	J6			OUTBIT5	J9			TDCSRCSEL1	J8		
OUTRES_N	J6			OUTBIT9	J9			TDCKCKSEL	J8		
INITUP	J6							TDC20BIT	J8		
CKROWA1A2	J6							TDCMODE	J8		
VDDIO_UP	J7							OSCEN	J8		
S0	J7							OSCCKSEL1	J8		
TDCSRCSEL0	J8							OSCCKSEL0	J8		
TDCSRCSEL1	J8							VDDIO	J8		
TDCKCKSEL	J8										
TDC20BIT	J8										
TDCMODE	J8										
OSCEN	J8										
OSCCKSEL1	J8										
OSCCKSEL0	J8										
VDDIO	J8										



DB 44

A1				A2				A3			
NAME	CONN	N_PIN	N_CONN	NAME	CONN	N_PIN	N_CONN	NAME	CONN	N_PIN	N_CONN
TDCRESET_N	J10	51	13	VDD_DOWN	J10	38	11	INITDOWN	J10	44	12
VDD_DOWN	J10			VDD_UP	J14			CKCOLA3	J10		
TDCOUT	J11			OUTBIT0	J15			TDCRESET_N	J10		
TDCKCKSHIFT	J11			OUTBIT1	J15			VDD_DOWN	J10		
TDCKCKEXT	J11			OUTBIT2	J15			CKROWA3	J11		
VDD_UP	J14			OUTBIT3	J15			TDCOUT	J11		
TDCIN4	J12			OUTBIT4	J15			TDCKCKSHIFT	J11		
TDLOCK	J12			OUTBIT6	J15			TDCKCKEXT	J11		
VDD_LEFT	J16			OUTBIT7	J15			TDCIN4	J12		
TRIG1	J16			OUTBIT8	J15			TDLOCK	J12		
OUT1	J16			VDD_RIGHT	J15			VDD_UP	J14		
GND	J16			GND	J15			VDD_RIGHT	J15		
VDD_RIGHT	J15			VDD_LEFT	J16			GND	J15		
TRIG2	J17			VDDIO_LEFT	J18			VDD_LEFT	J15		
OUT2	J17			VDD33	J19			TRIG5	J17		
TRIG3	J17			GND33	J19			VK3	J17		
OUT3	J17			EN	J5			OUT5	J18		
TRIG4	J17			TEST_N	J5			TRIG6	J18		
OUT4	J17			DATATX	J5			OUT6	J18		
MONOA1	J17			CONF0	J5			MONOA3	J18		
VK1	J17			CONF1	J5			VDDIO_LEFT	J18		
VDDIO_LEFT	J18			VCLAMP	J6			VDD33	J19		
VDD33	J19			VB	J6			GND33	J19		
GND33	J19			S1	J6			EN	J5		
EN	J5			VCONN	J6			TEST_N	J5		
TEST_N	J5			CELLRESMOD	J6			DATATX	J5		
DATATX	J5			ENRESGLOB_N	J6			VCLAMP	J6		
CONF0	J5			CKROWA1A2	J6			VB	J6		
CONF1	J5			CKCOLA2	J6			VCONN	J6		
CKCOLA1	J5			INITUP	J6			CELLRESMOD	J6		
VCCLAMP	J6			S0	J7			ENRESGLOB_N	J6		
VB	J6			VDDIO_UP	J7			TRIGRES_N	J6		
S1	J6			VDDIO	J8			OUTRES_N	J6		
VCONN	J6			VK2	J9			VDDIO_UP	J7		
CELLRESMOD	J6			INTEG	J9			S0	J7		
ENRESGLOB_N	J6			RCNT_N	J9			TDCSRCSEL0	J8		
TRIGRES_N	J6			OUTBIT5	J9			TDCSRCSEL1	J8		
OUTRES_N	J6			OUTBIT9	J9			TDCKCKSEL	J8		
INITUP	J6							TDC20BIT	J8		
CKROWA1A2	J6							TDCMODE	J8		
VDDIO_UP	J7							OSCEN	J8		
S0	J7							OSCCKSEL1	J8		
TDCSRCSEL0	J8							OSCCKSEL0	J8		
TDCSRCSEL1	J8							VDDIO	J8		
TDCKCKSEL	J8										
TDC20BIT	J8										
TDCMODE	J8										
OSCEN	J8										
OSCCKSEL1	J8										
OSCCKSEL0	J8										
VDDIO	J8										



DB 44