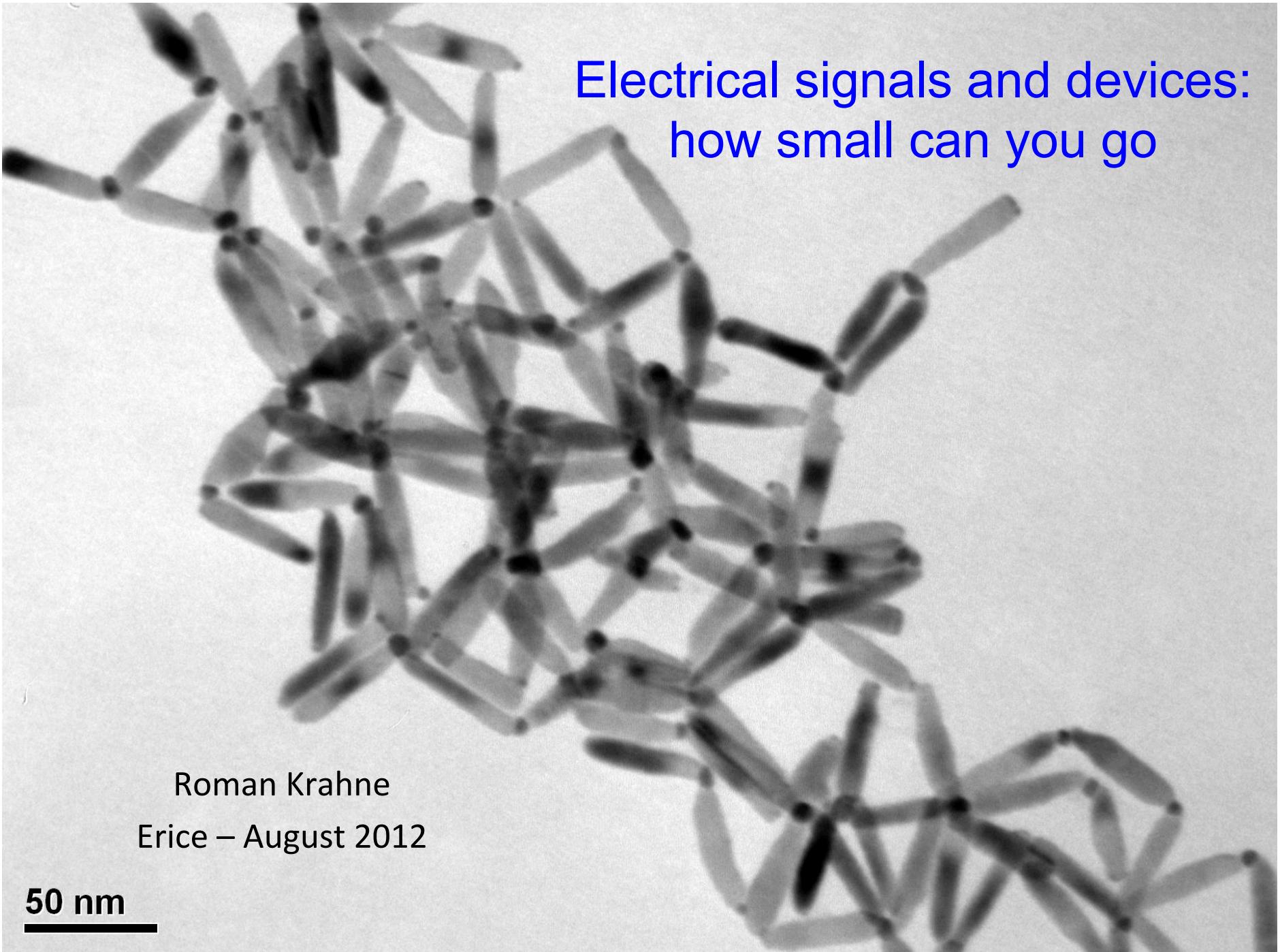


Electrical signals and devices: how small can you go



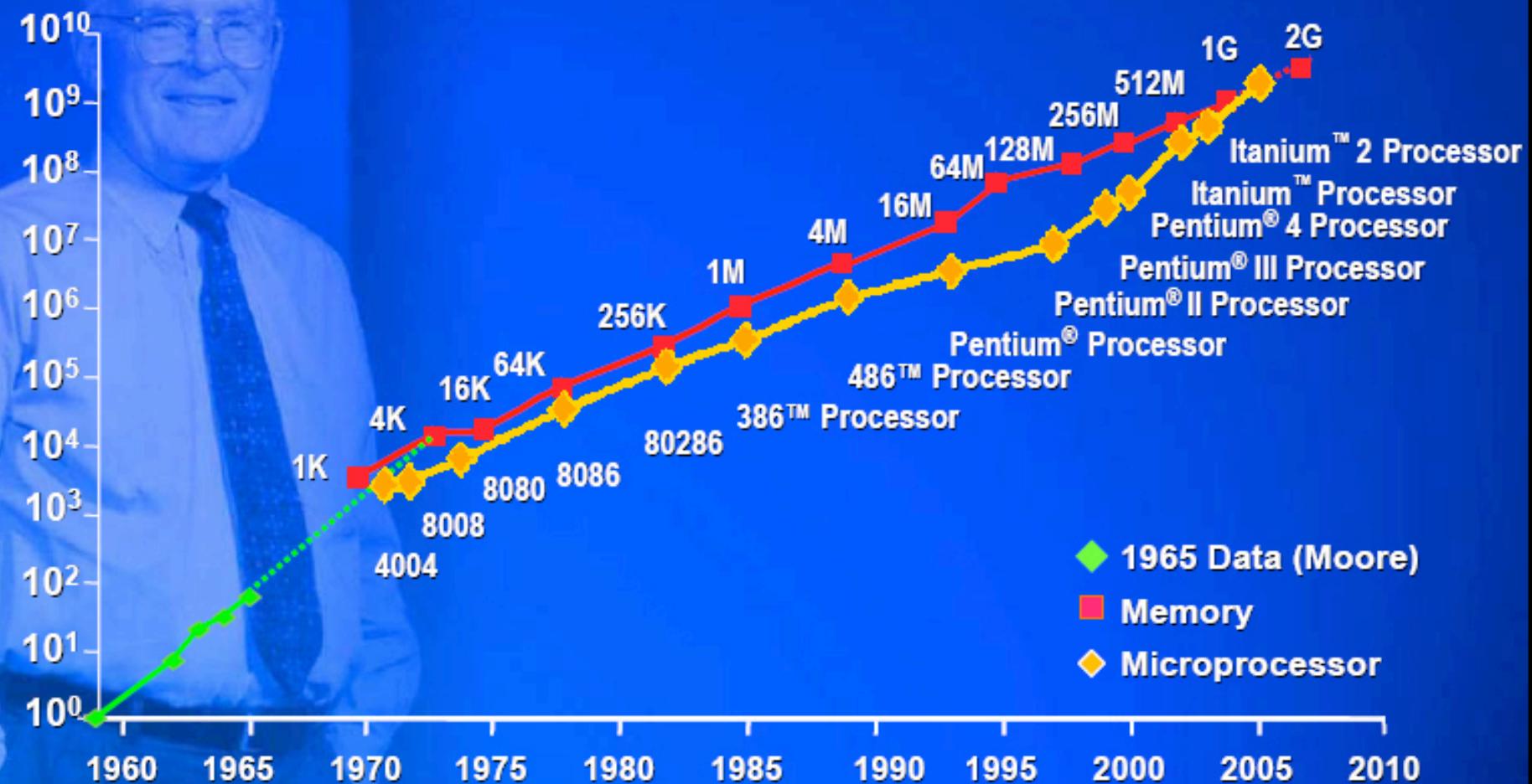
Roman Krahne

Erice – August 2012

50 nm

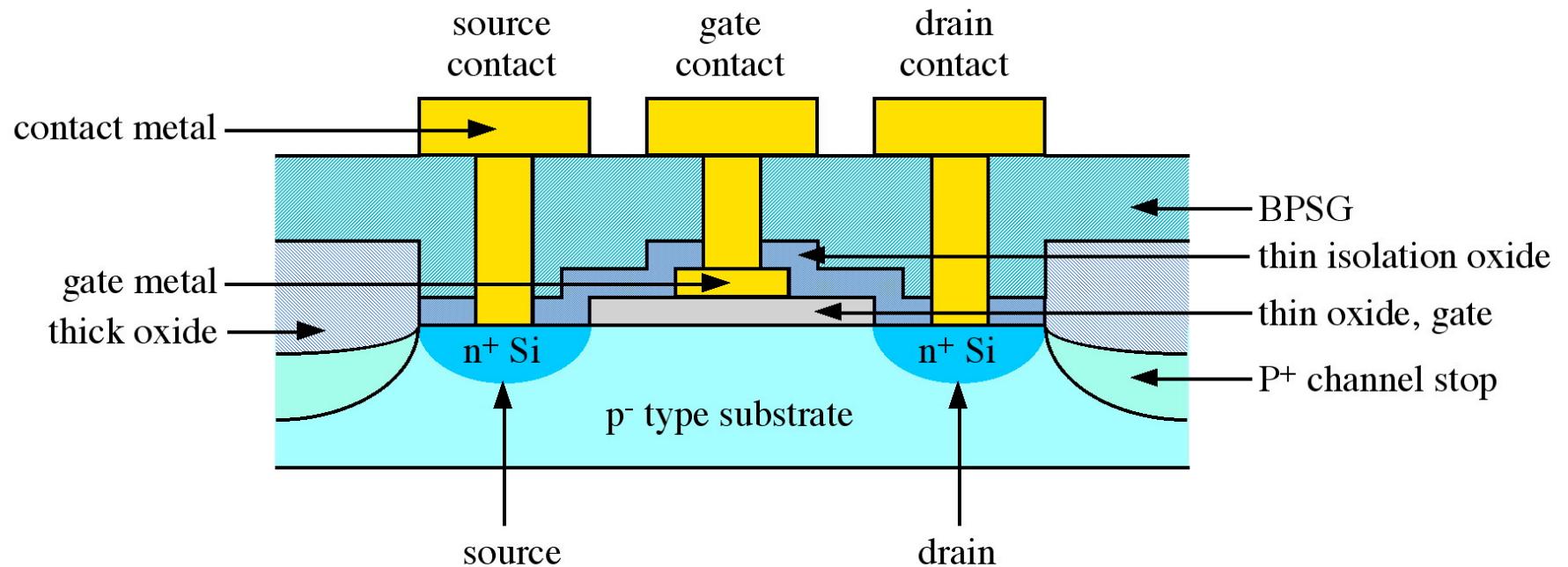
Moore's Law - 2005

Transistors
Per Die



Source: Intel

MOSFET

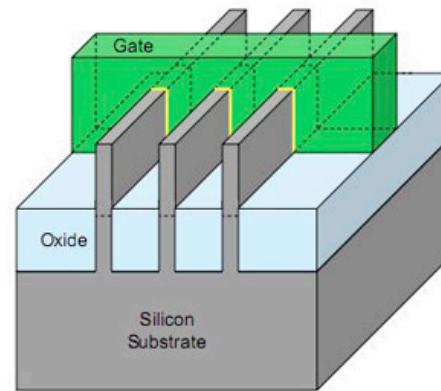


Processor	Year	Minimum feature size
Intel 4004	1971	10 µm
Intel Pentium	1993	0.8 µm
Core i7	2011	0.032µm

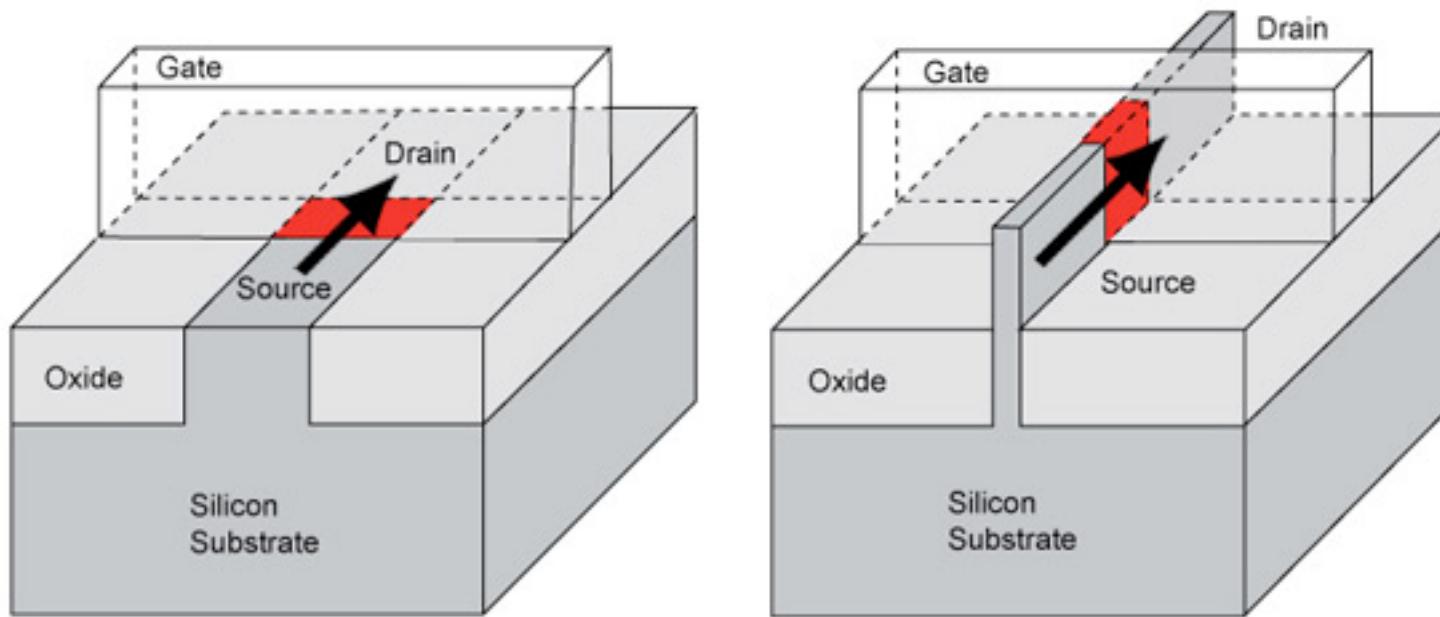


Bumble bee cannot fly
- theoretically

22 nm Tri-Gate Transistor



Tri-Gate transistors can have multiple fins connected together



Prototype from Berkeley Labs

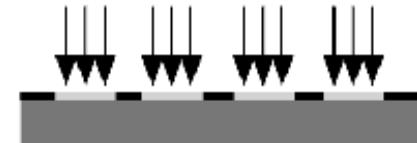
Tools: parallel processes

Standard lithography

photoresist

Si/SiO₂ substrate

exposition (hv / electrons)



development,
evaporation of catalyst



lift-off



CVD growth



Shadowmasking

Si/SiO₂ substrate

shadow mask

evaporation of catalyst

mask removal

CVD growth

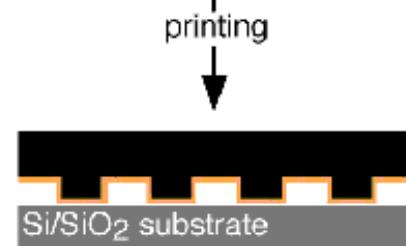


Soft lithography

Stamp (PDMS)

inking

ink solution

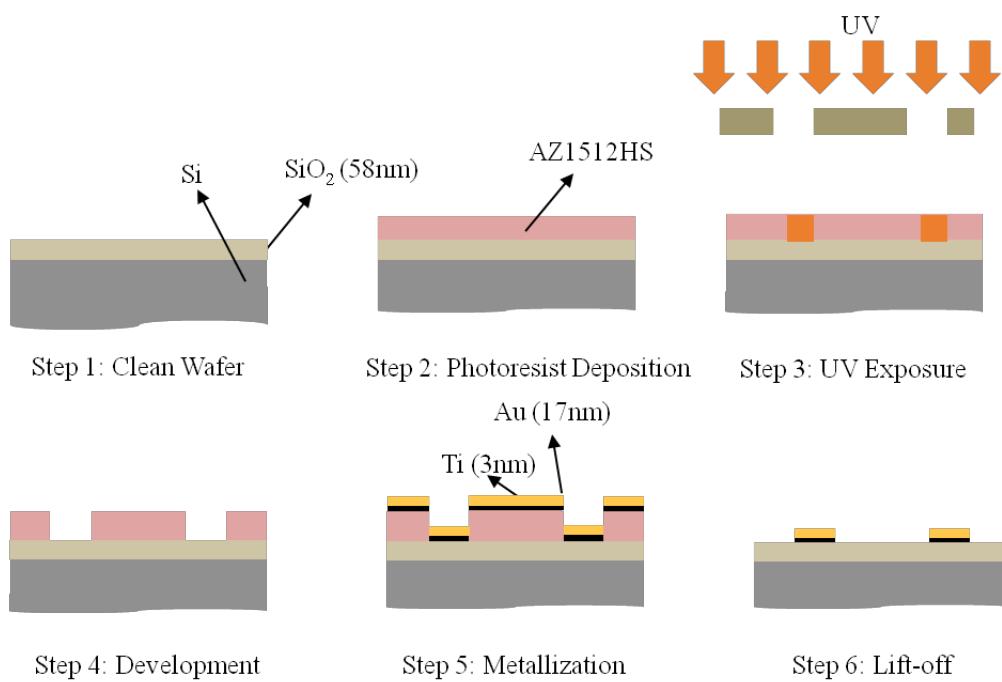
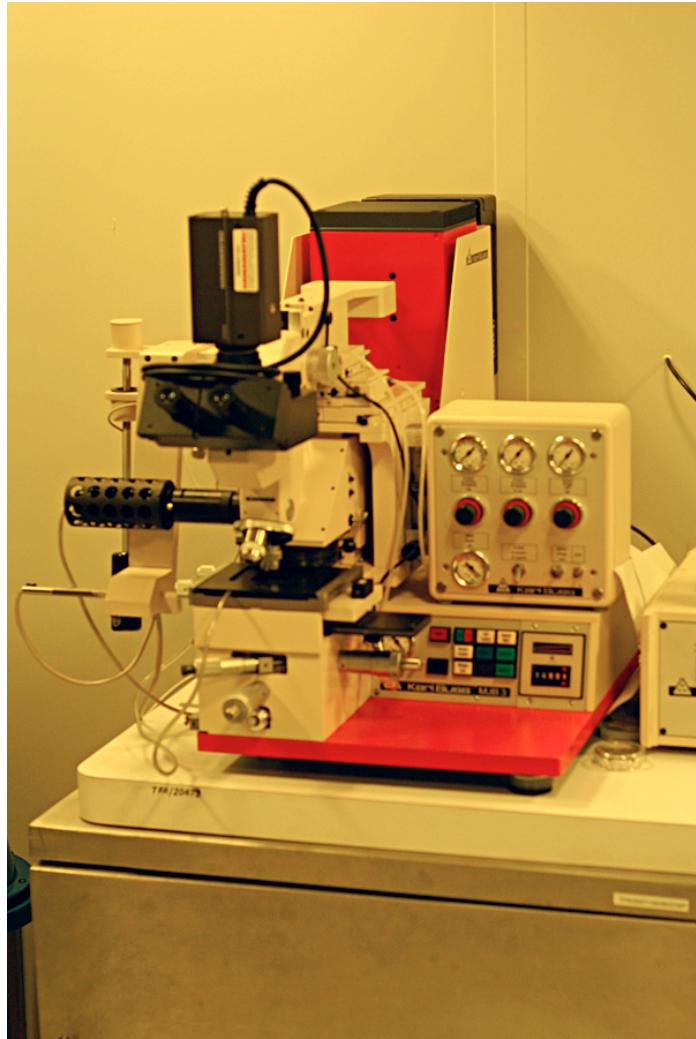


printing

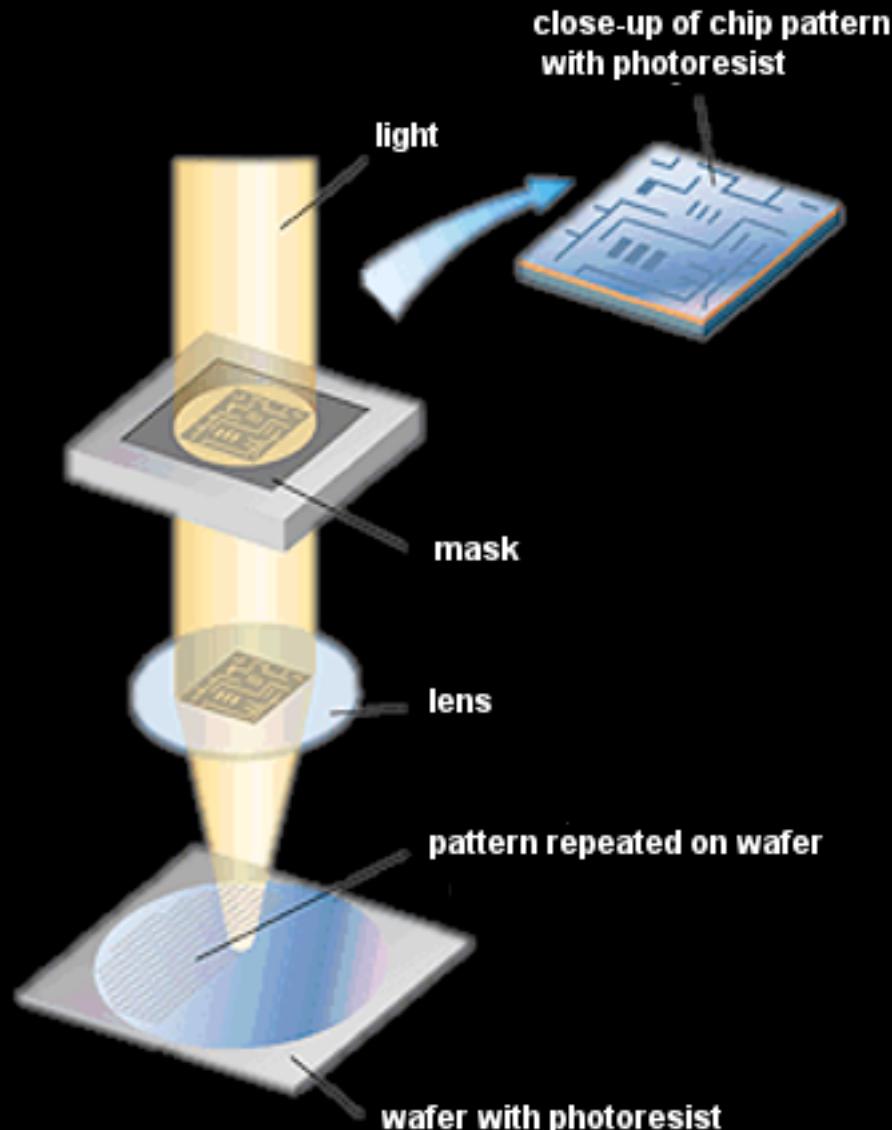


CVD growth

University style photolithography



Photolithography

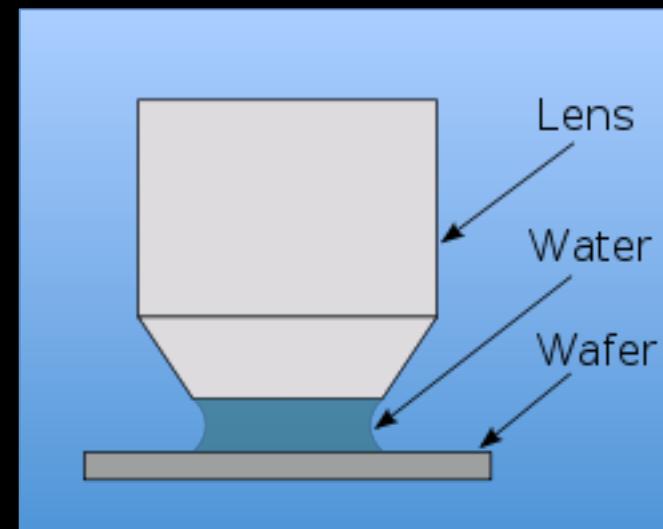


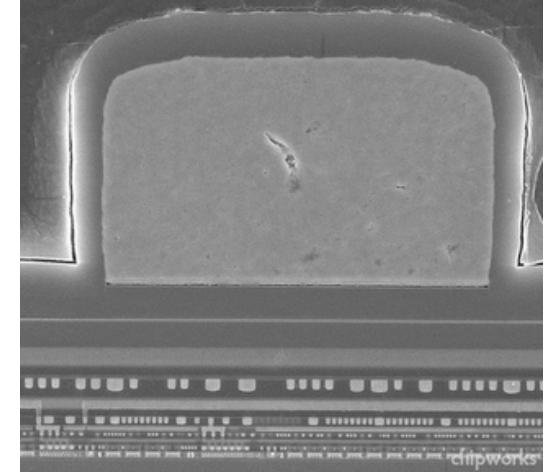
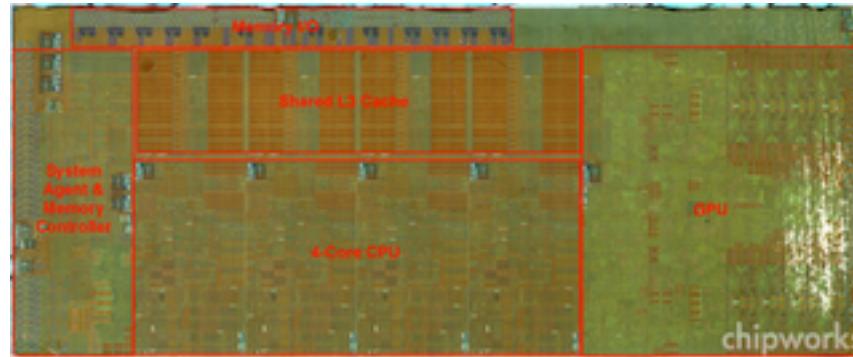
$$F = k \frac{\lambda}{N_A}$$

"straight forward" resolution:
Around 1 μm

BUT

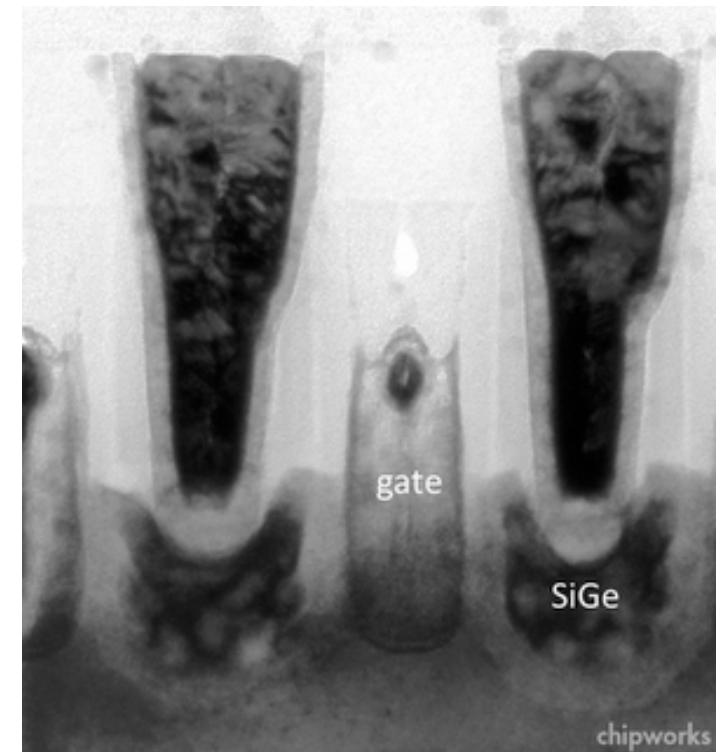
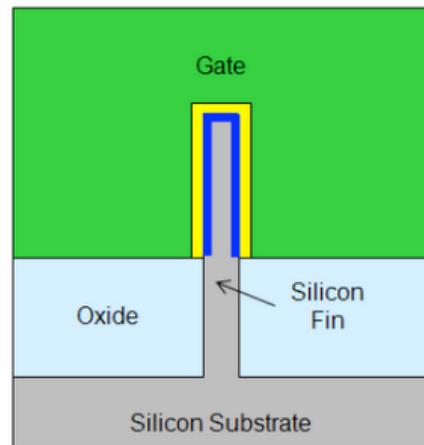
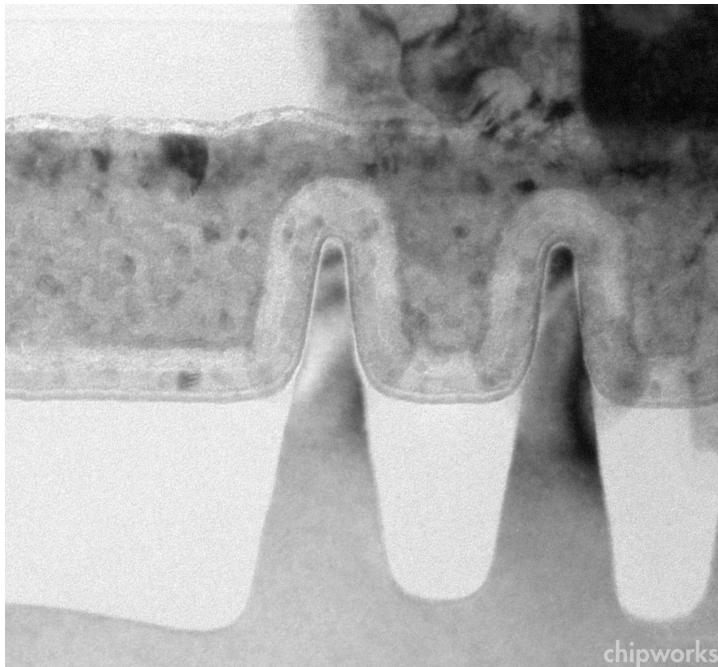
Industry gets it down to
currently 22 nm





Intel's 22-nm Trigate Transistors

<http://www.electroiq.com>



**Biggest problem is not size,
but heat dissipation!**

And of course fabrication cost

-> research on alternative systems

Research tools

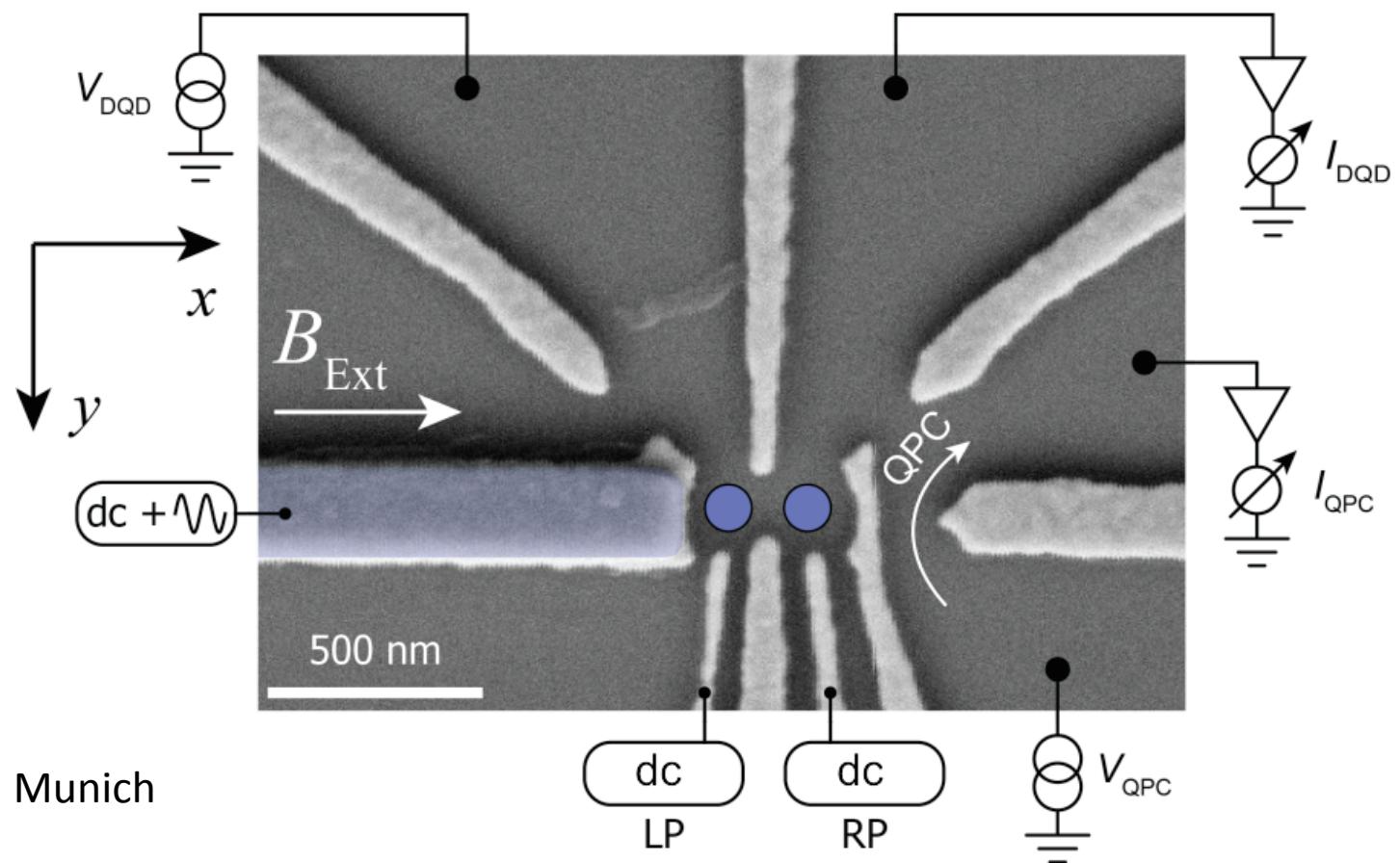
First were used to image

Then to manipulate!



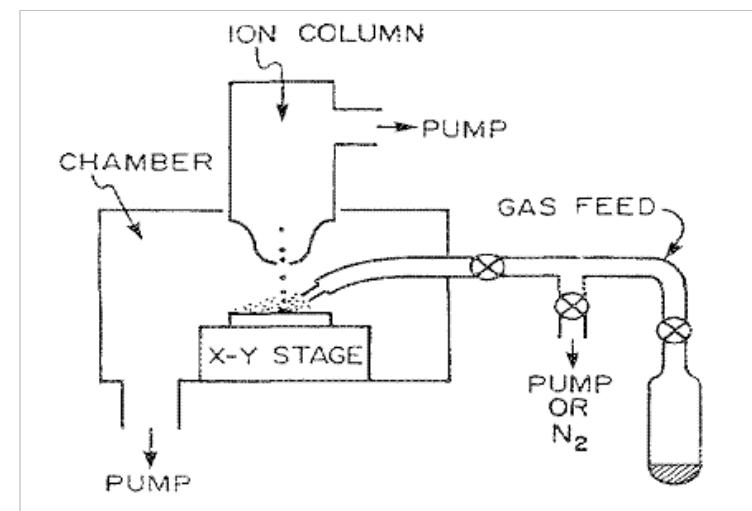
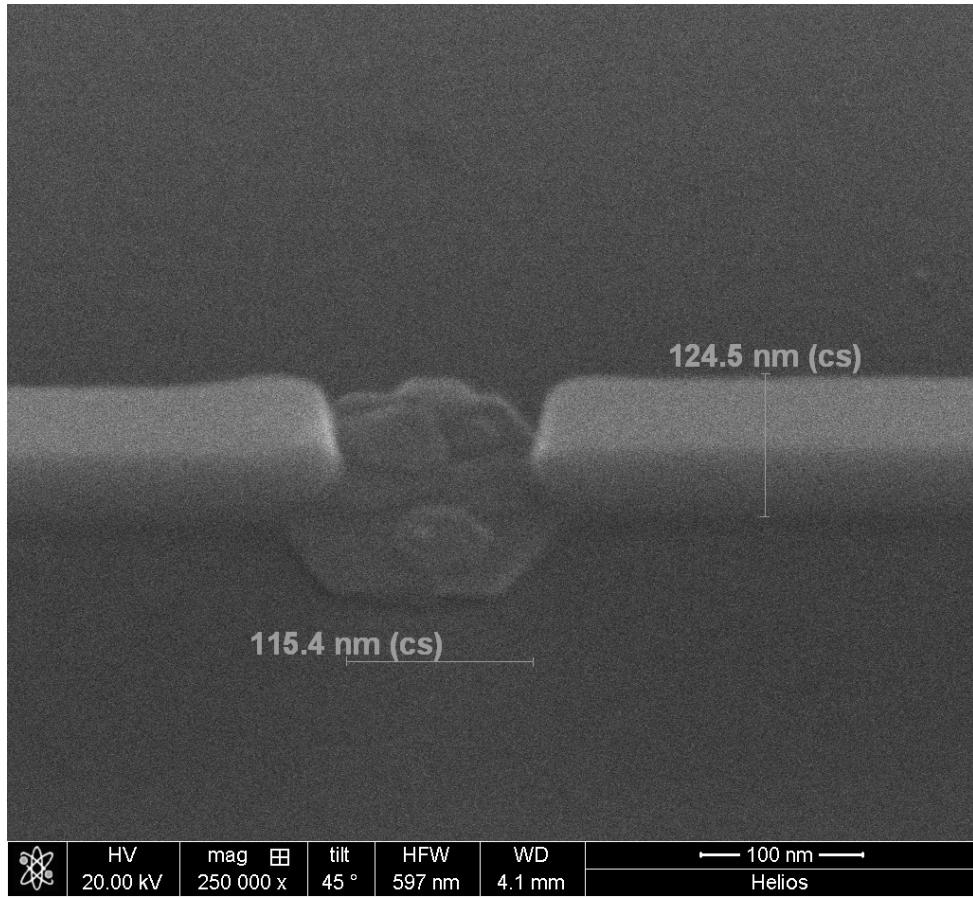
Electron beam lithography

Resolution down to few nm

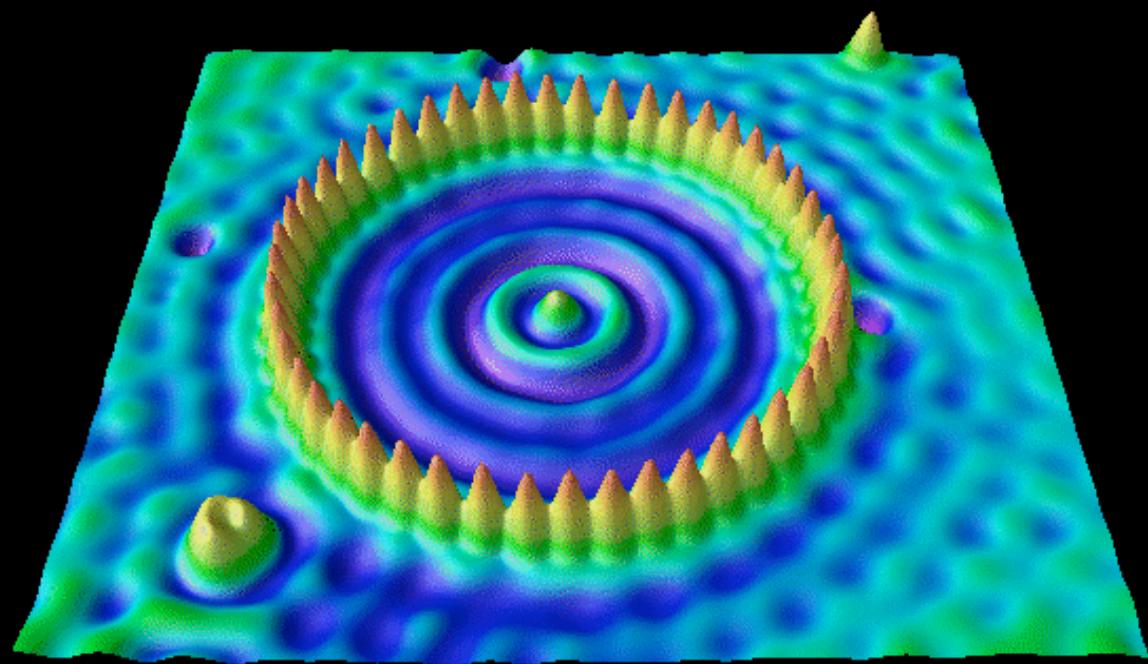


Kotthaus group, TU Munich

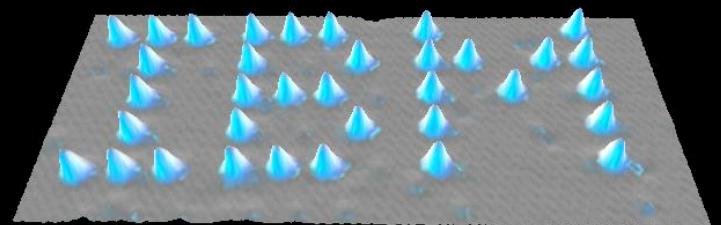
Focused ion beam deposition



STM/AFM lithography

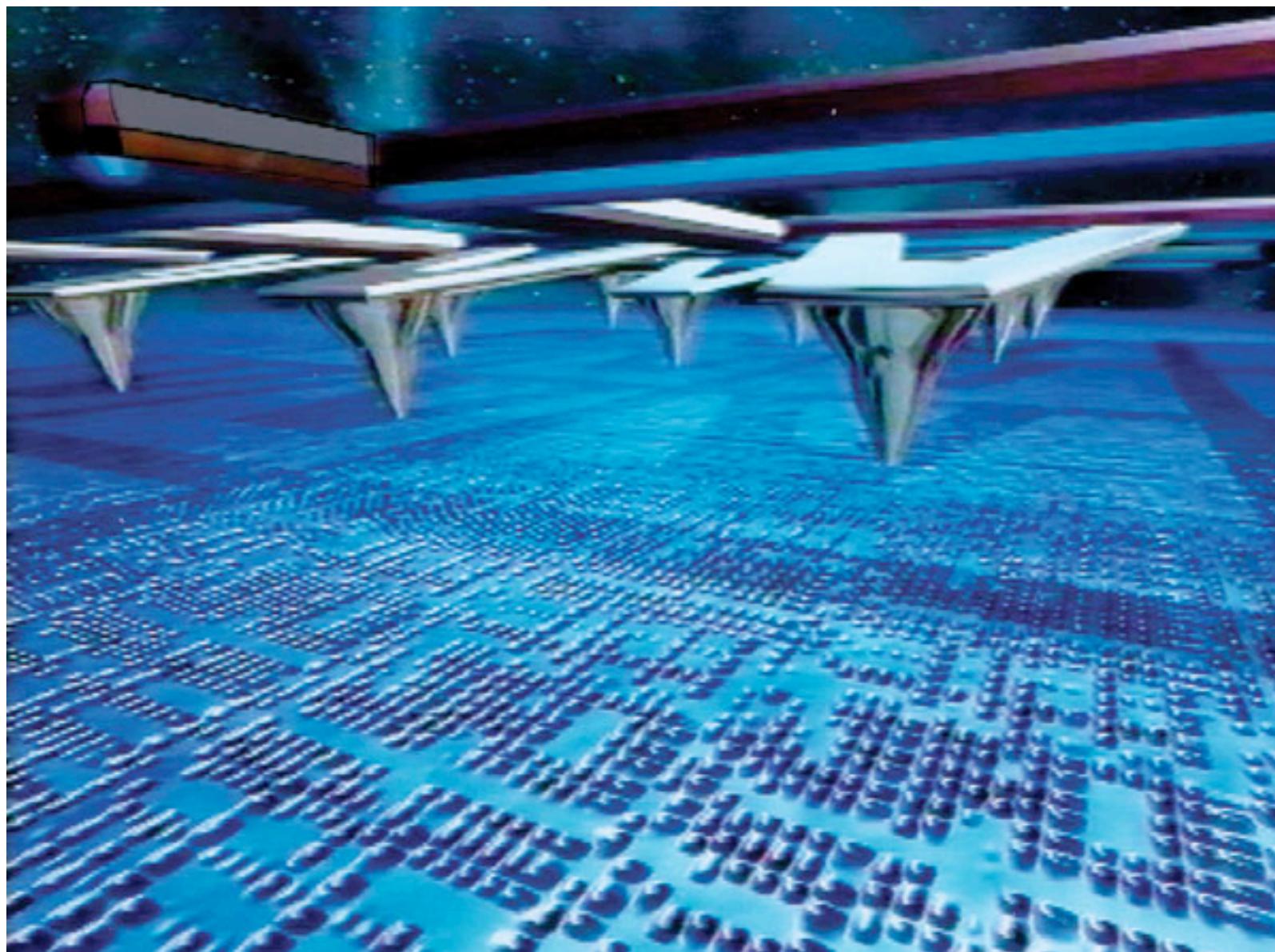


Single atom manipulation



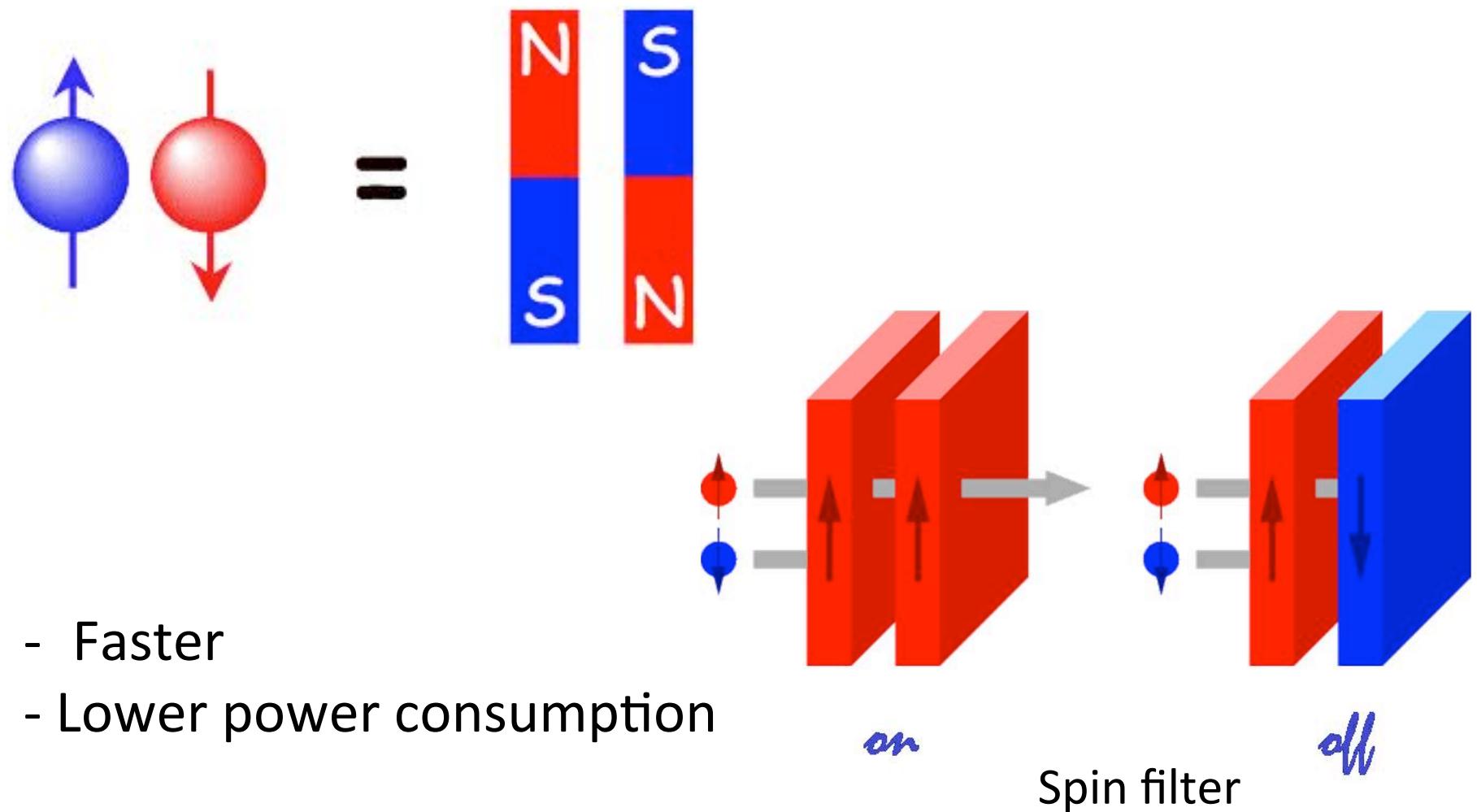
IBM movie

IBM millipede project



Spintronics

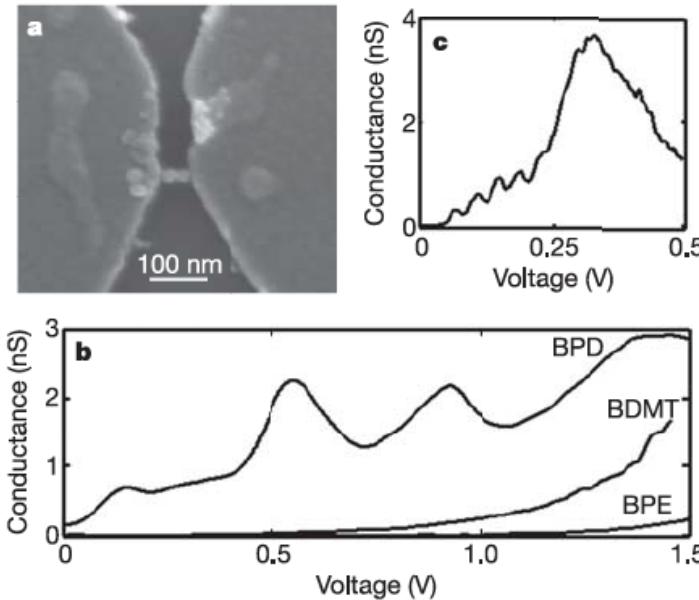
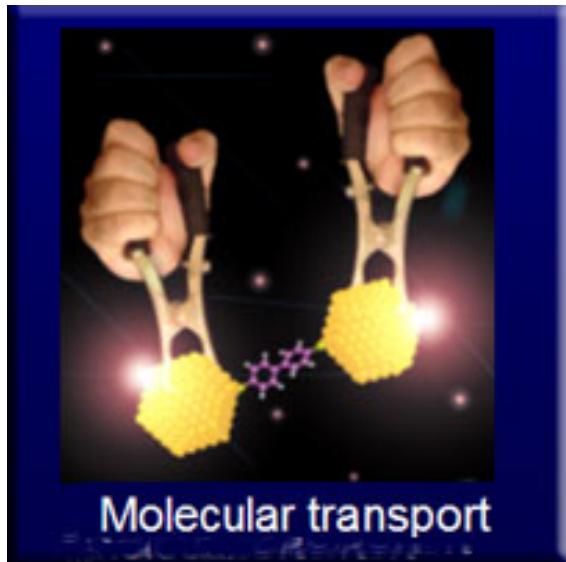
Electron spin =magnetic flux



- Faster
- Lower power consumption

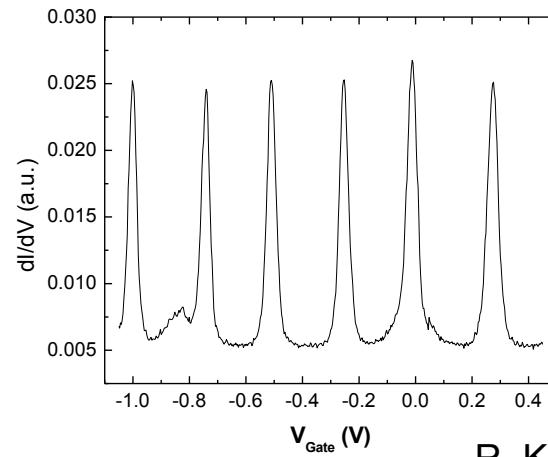
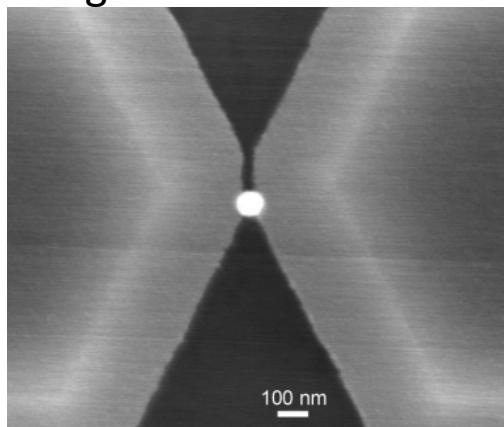
Molecular electronics

Single molecule conduction



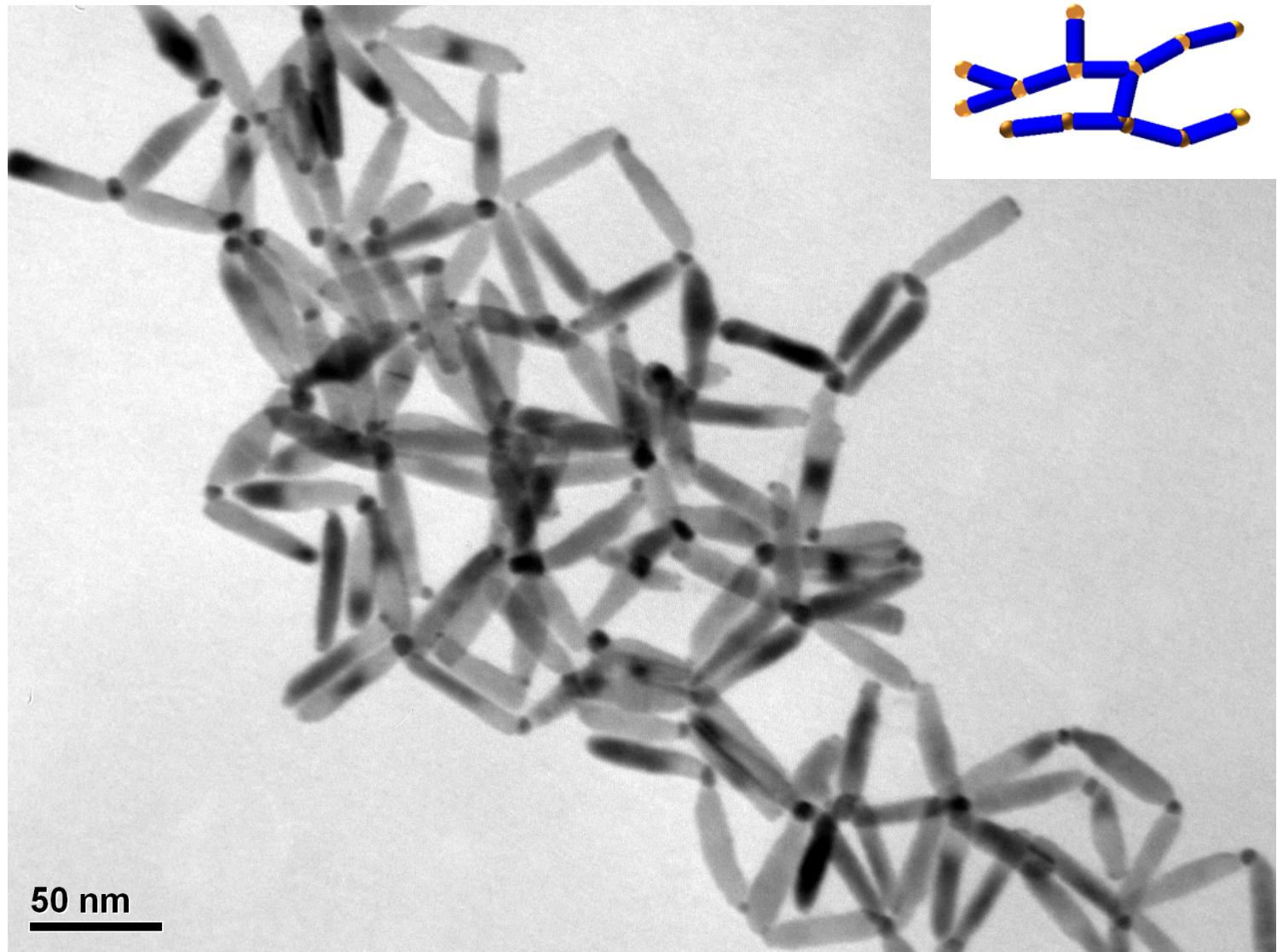
T. Dadosh, R. Krahne et al., **Nature 436** (2005)

Single electron transistor



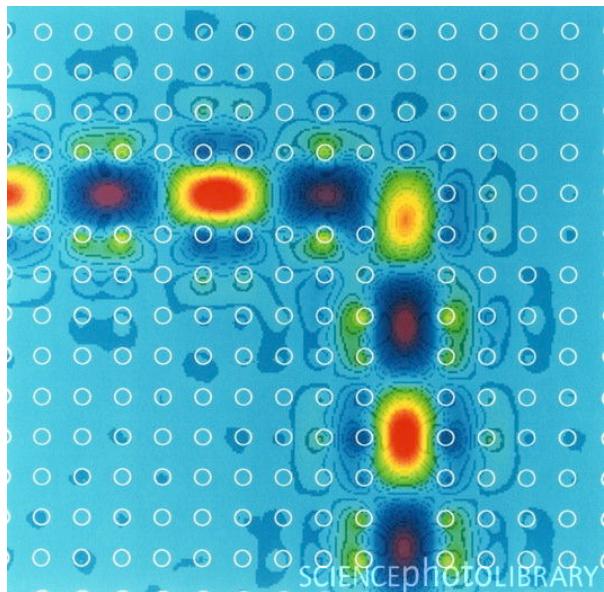
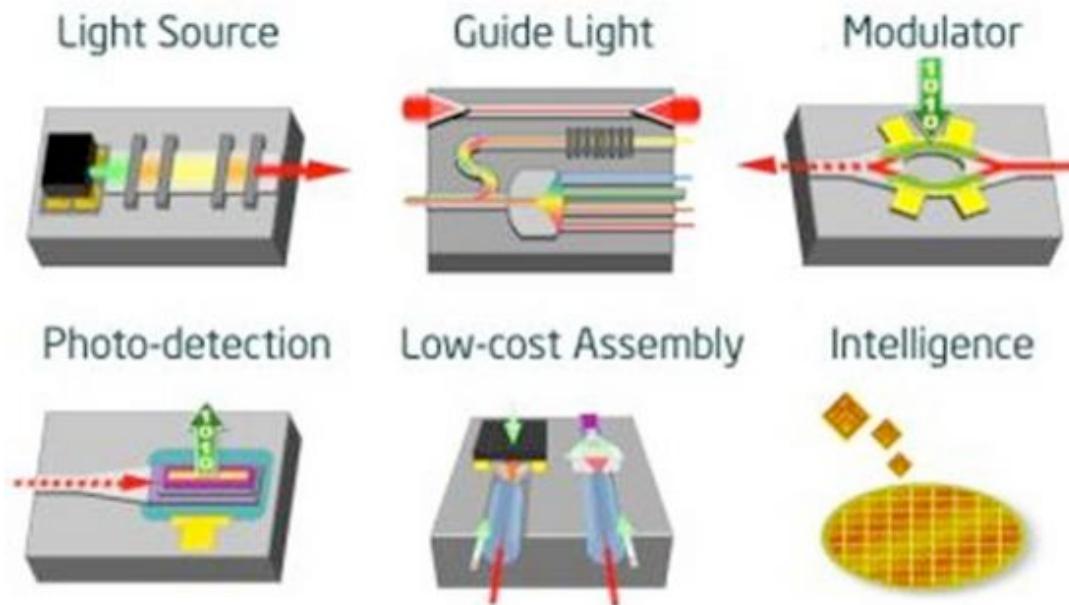
R. Krahne et al., **APL 81** (2002)

Bottom-up approaches



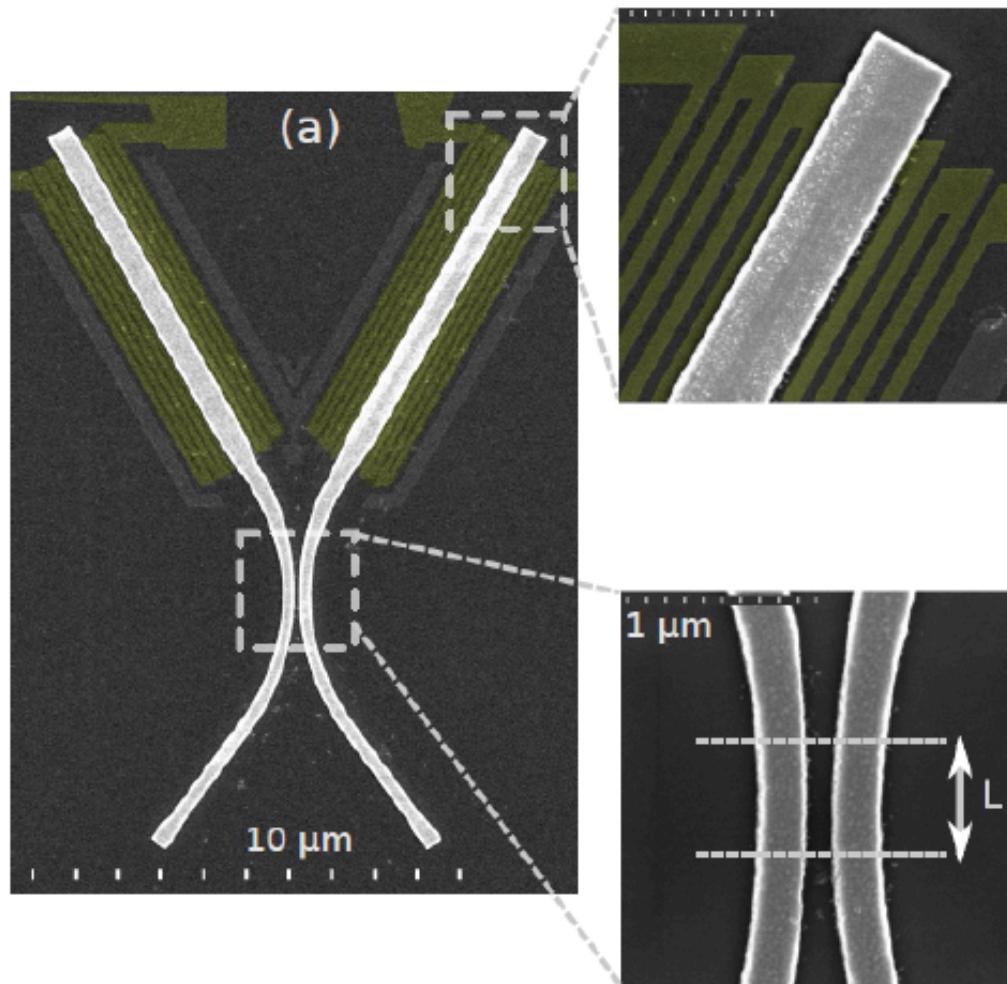
R. Lavieville, R. Krahne et al., ACS Nano 6 (2012)

Silicon Photonics



Vision: Plastic photonic circuits
Who cares if the circuit board is large,
if it is light, flexible, and can be fabricated by
your home printer.

Plasmonics



Val Zwiller group (Delft)

Nanotechnology advantages

- Photovoltaics: large surface to volume ratio -> large absorption area for incoming light.
- Energy consumption: small wires, precise energy level structure
 - > low current
- Low fabrication cost due to bottom-up approaches
 - > material self-assembles into functional structures (like coffee stain laser)