SVT activities

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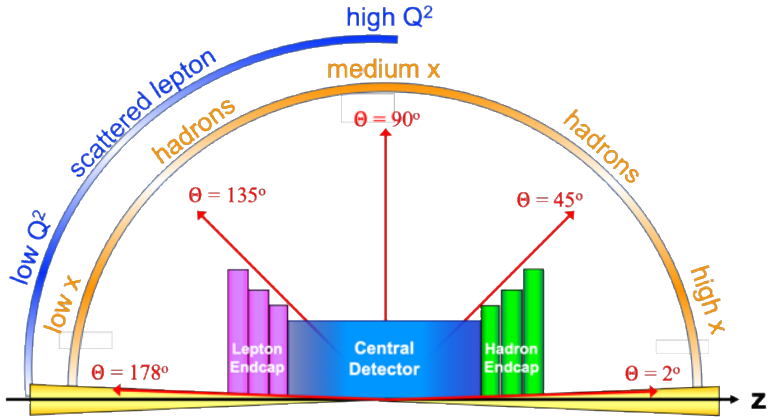
ePIC Trieste meeting

13 March 2025

ePIC Silicon Vertex Tracker

ePIC Silicon Vertex Tracker Motivation



	Momentum Resolution	Spatial Resolution
Backward (-3.5 to -2.5)	~ 0.10%×p⊕ 2.0%	~ 30/p_T μm ⊕ 40 μm
Backward (-2.5 to -1.0)	~ 0.05%×p⊕ 1.0%	~ 30/p_T μm ⊕ 20 μm
Barrel (-1.0 to 1.0)	~ 0.05%×p⊕ 0.5%	~ 20/p_T μm ⊕ 5 μm
Forward (1.0 to 2.5)	~ 0.05%×p⊕ 1.0%	~ 30/p_T μm ⊕ 20 μm
Forward (2.5 to 3.5)	~ 0.10%×p⊕ 2.0%	~ 30/p_T μm ⊕ 40 μm

EIC physics requirements on charged-particle tracking and vertexing are stringent,

They drive the need for a well integrated, large acceptance, high granularity, and low-mass tracking and vertexing subsystem,

and drive the choice for a new generation MAPS technology — based off the ALICE-ITS3 development.

ePIC Silicon Vertex Tracker

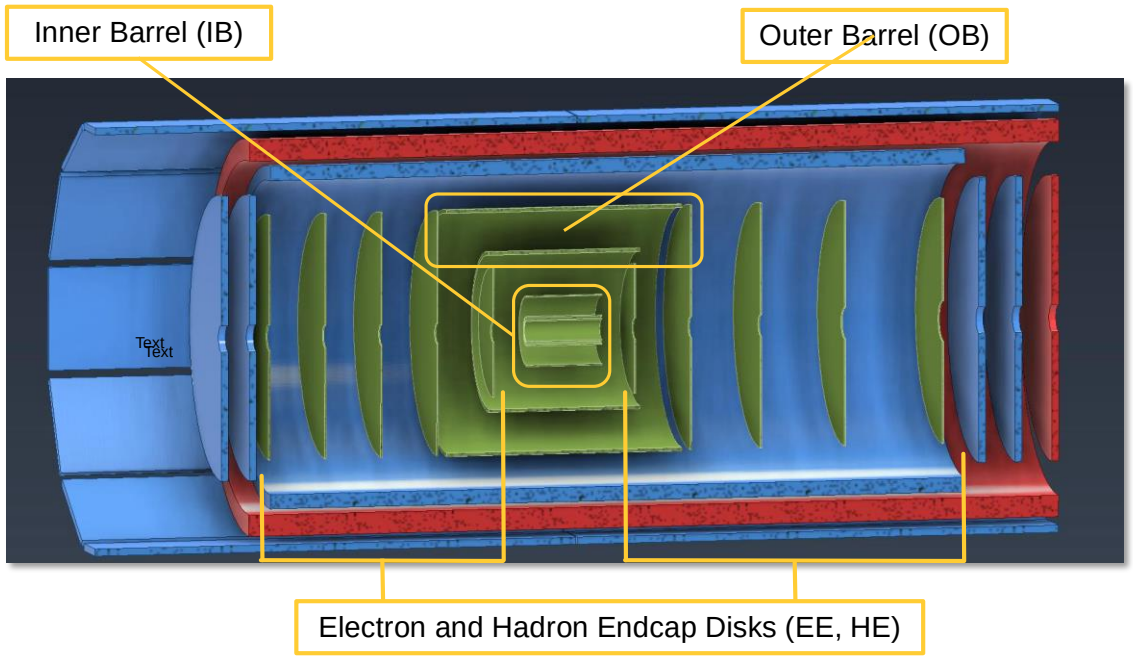
Silicon Vertex Tracker Concept

INFN

- **Inner Barrel (IB)**
  - Three layers, L0, L1, L2,
  - Radii of 36, 41, 120 mm
  - Length of 27 cm
  - X/X_0 ~ 0.05% per layer
  - Curved, thinned, wafer-scale sensor (ITS3),
  - Approx. 20µm pixel pitch

- **Outer Barrel (OB)**
  - Two layers, L3, L4
  - Radii of 27 and 42 cm
  - X/X_0 ~0.25% and ~0.55%
  - More conventional structure w. staves
  - Sensor derived from IB sensor

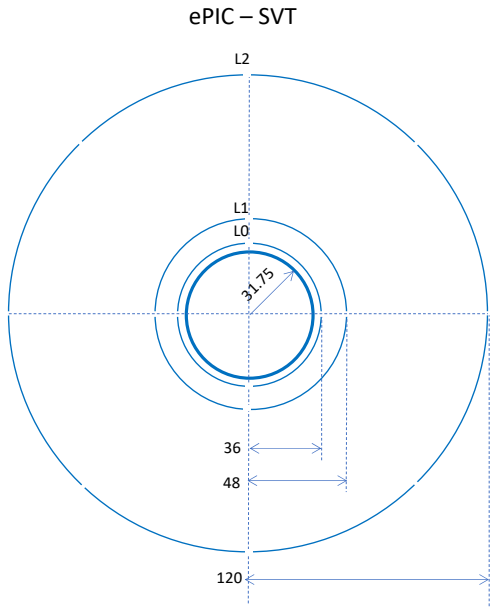
- **Electron/Hadron Endcaps (EE, HE)**
  - Two arrays with five disks
  - X/X_0 ~0.25% per disk
  - More conventional structure
  - Sensor derived from IB sensor; common with OB

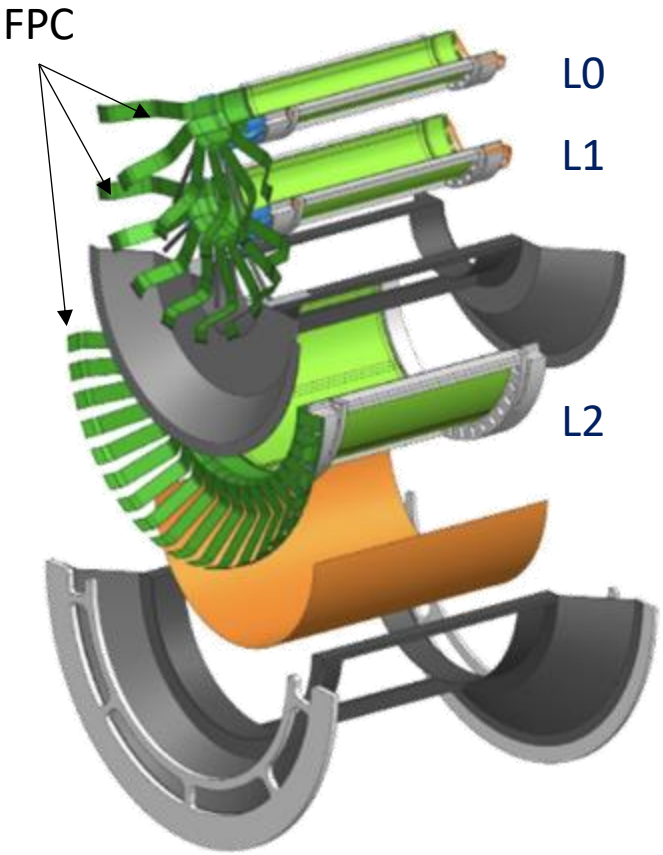


- **Lengths for L2—L4 increase so as to project back to z = 0; disk radii adjust accordingly**

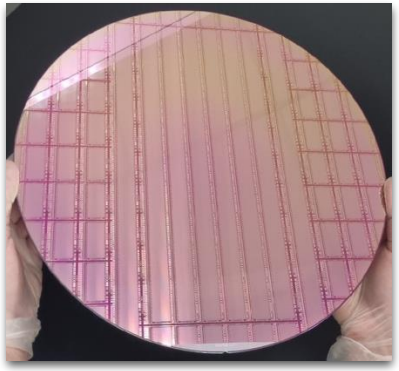
SVT Inner Barrel

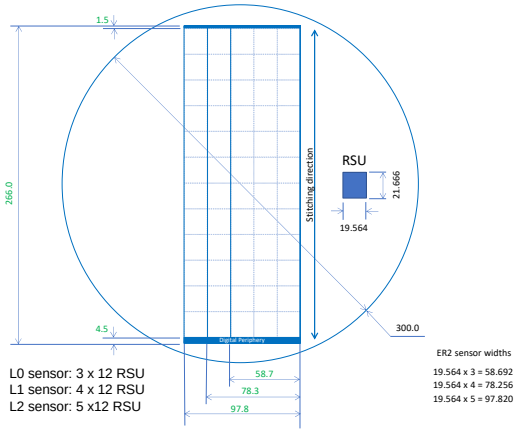
- SVT IB will use ALICE ITS3 sensor, MOSAIX
- ITS3 detector concept adapted to ITS3 geometry
  - Larger EIC beam pipe → larger layers radii; more sensors in each layer
  - Due to the beam pipe geometry, and the need for full disk acceptance services need to be routed along service cones → FPC design equivalent electrically to ITS3 one, but mechanically different, Alu instead of Cu technology

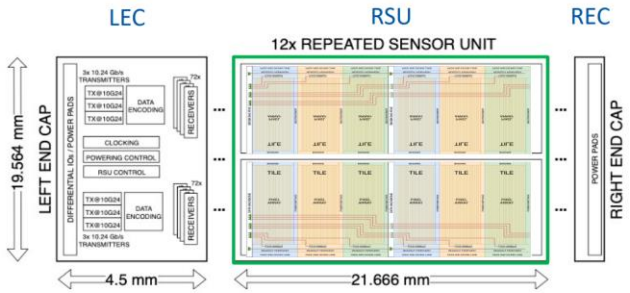




ER1 wafer





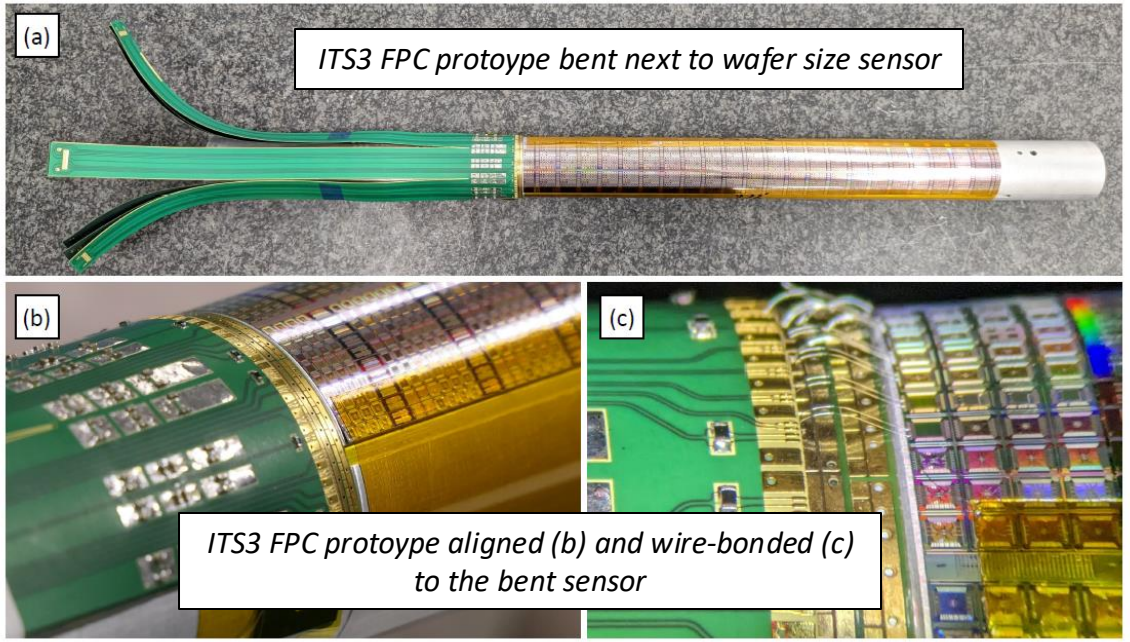


Pixel size: ~ 20 x 22 μm²
Frame duration: 2 to 5 μs
Data link: 10.24 Gbps

Qualification, test and production of the SVT IB FPCs

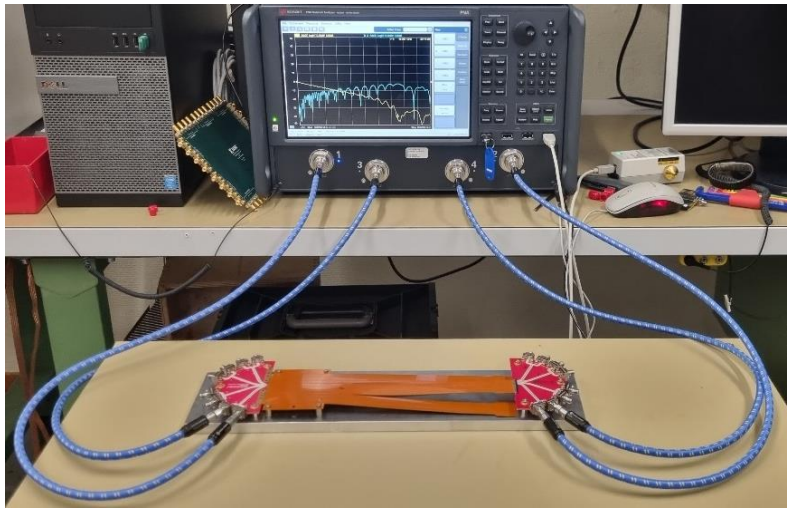
- Activity on SVT IB FPC:
  - **Collaboration with Daresbury LAB** and SVT WGs for **FPC design adaptation from ITS3** version to the SVT constraints and characteristics
  - SVT FPC **prototyping and qualification tests**
  - Production **quality control**

- Existing expertise from ITS2 OB FPC:
  - Definition of production specifications
  - Vendor search and production tendering
  - Qualification tests
  - Final integration with power bus
  - Vendor search and quality assurance



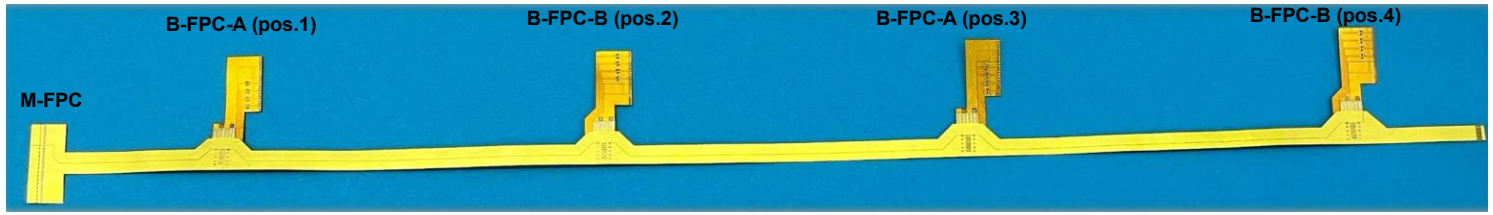
FPC R&D in Trieste

- FPC signal integrity to verify 10 Gbps data transmission
  - S-Parameter measurement (VNA) and eye diagram (High speed scope), BERT (FPGA)
  - FPC bent to different radii
- Test structures to be received
  - ITS3 prototype FPC from CERN
    - Same electrical functionality as ePIC IB FPC; Cu traces
  - ePIC SVT L4 prototype FPC from Daresbury Lab
    - Al traces, ePIC IB preferred technology



ITS3 FPC test setup and interconnections

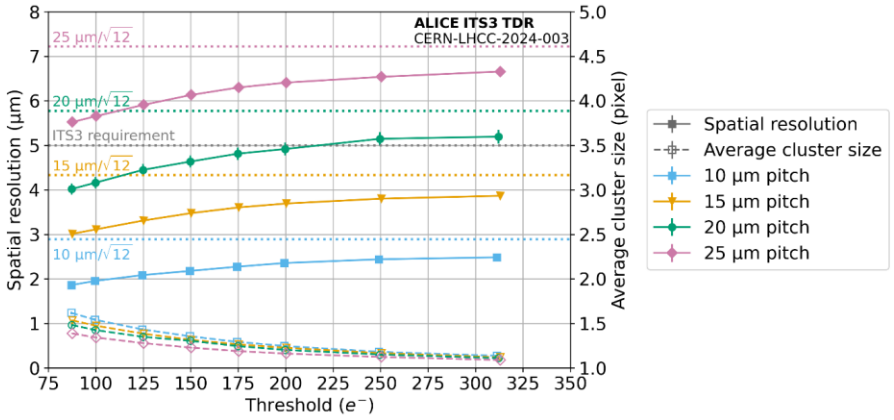
EPIC SVT L4 prototype FPC by RPE LTU



Sensor characterisation

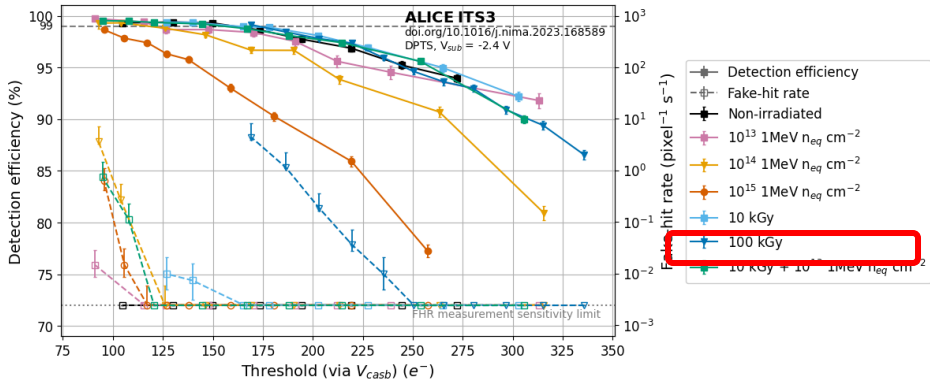
- **Characterisation of ITS3 sensor prototypes** in the context of ALICE
  - MLR1: DPTS and APTS
  - ER1: babyMOSS
  - Efficiency, noise, power consumption, charge collection, spatial resolution, cluster size, energy response

- Plans:
  - Characterisation of (baby)MOSS, ER2 MOSAIX and final ITS3 sensor
  - **Specific studies for ePIC SVT** (spatial resolution, fake hit rate, tests in climate chamber, …)



APTS

Spatial resolution *Vs threshold and pixel pitch, as measured in testbeams on* ***APTS***



DPTS

Detection efficiency and fake-hit rate *Vs threshold and irradiation levels, as measured on 15 µm pitch* ***Digital Pixel Test Structures (DPTS)***

Generic R&D for EIC

- **Aerosol Jet Printing redistribution layers on MAPS**
- In-silicon power distribution over long distances not yet validated
  - If *stitching* yield is sub-optimal for excessive voltage drop across the chip, a **post-processing** of the sensor is needed (measurements are ongoing)

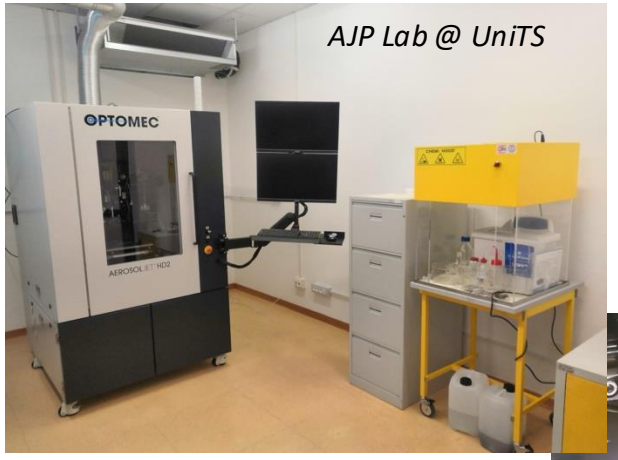
- Application of a Re-Distribution Layer (RDL) with **Aerosol Jet Printing technique**
  - Additional copper and polyamide layer(s) added to the wafer where needed
  - Trade-off between resistance and material budget
  - Aerosol Jet Printing (AJP) machine available at INFN TS – UniTS:
    - 10 µm spatial resolution, on planar and bent substrate

Generic R&D for EIC

- AJP acquired in 2023 by the University through a '**large instrumentation call**'
  - Additional funds from '**EIC Generic R&D Program'** and **MAECI-funded project**
  - Interdisciplinary research (Physics, Engineering, Chemistry Departments)

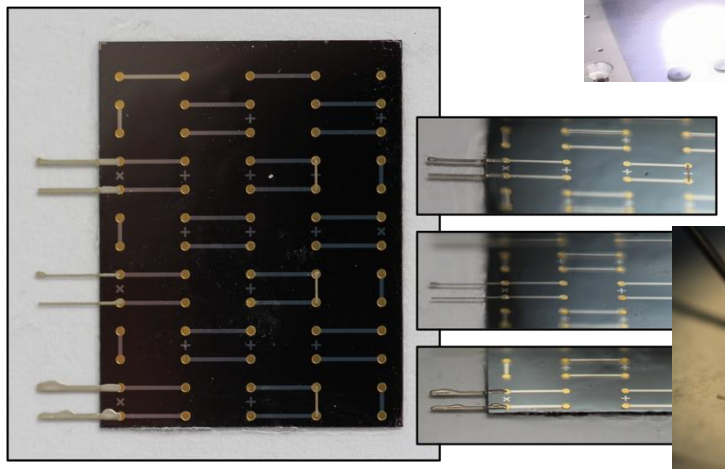
- Ongoing work
  - **Systematic studies** to control the process
  - Several **conductive and dielectric ink** deposition campaigns
  - Deposition on **silicon and glass**
  - Mechanical and electrical tests

- **Collaboration with LBNL** for next round of EIC Generic R&D funding



AJP Lab @ UniTS

AJP printing process



AJP printed samples

Electrical characterisation