ER2 characterisation and test system plans

Luca Aglietta and Valerio Sarritzu

ER2 submission overview

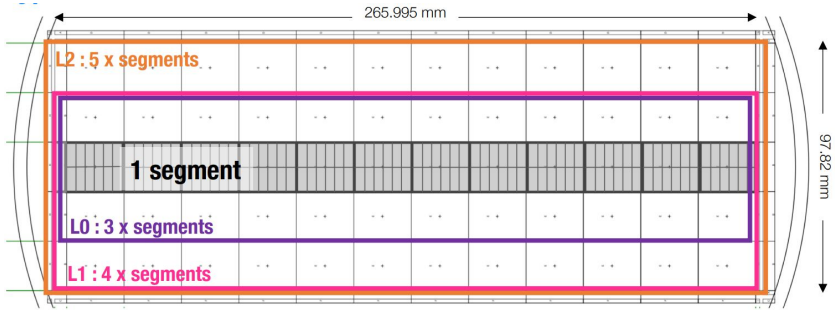
In an ER2 wafer we should have:

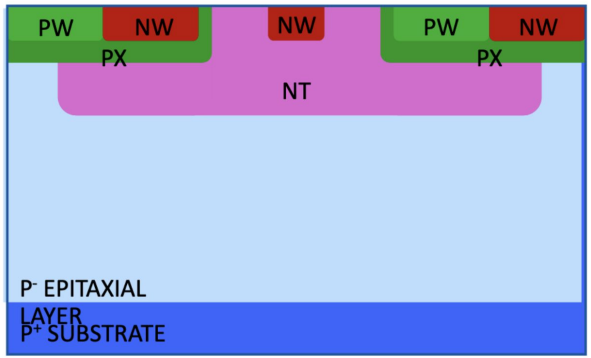
- 5 Large MOSAIX
- ≈20 babyMOSAIX
- Small scale chiplets
  - Pixel test structures
  - Other test structures

In total there should be 4 **splits** with different doping profiles for faster charge collection and smaller input capacitance (-> smaller power consumption)

Primary Goals:

1. Validate MOSAIX design
2. Determine production yield
3. Select best performing split and FE variant





ER2 Chiplets

1	TTS1		Process monitoring and modeling
3	TTS2		Process monitoring and modeling
5	APTS - SF standard	15 um pitch	Sensor reference
6	APTS - SF modified	15 um pitch	Sensor reference
7	APTS - SF modified with gap	15 um pitch	Sensor reference/optimization
8	APTS - SF modified with gap	20 um pitch	Exploration of larger pixel pitches/optimization
9	APTS - SF modified with gap	30 um pitch	Exploration of larger pixel pitches/optimization
10	APTS - SF modified with gap	40 um pitch	Exploration of larger pixel pitches/optimization
11	APTS - SF modified with gap	50 um pitch	Exploration of larger pixel pitches/optimization
12	APTS - SF modified with gap and Nwell	50 um pitch	Study of impact of Nwell.
13	APTS - SF modified with gap	20.8 x 22.8 um pitch	Sensor pitch in MOSAIX/optimization
14	APTS - OA modified with gap	10 um pitch	Sensor reference/optimization
15	DPTS modified with gap	15 um pitch	Sensor + FE reference/optimization
16	DPTS modified with gap	15 um pitch	Sensor + FE reference/optimization
17	DPTS modified with gap	15 um pitch	Sensor + FE reference/optimization
18	SEU3		Custom cell libraries SEE/SEL characterization
19	RING-OSC-v1 ported		Custom cell libraries leakage and delay
20	RING-OSC-v2		Custom cell libraries leakage and delay
21	MOSAIX BIASING		Standalone qualification of other versions of DAC and biasing blocks as backup
22	MOSAIX SERIALIZER		Full chain serializer test chip as in MOSAIX
23	TDC HEIDELBERG		TDC
24	IPHC ASYNCH READOUT (SPARC)		architecture study
25	SLAC NAPA-v2		update on pulsed readout
26	BNL ADC		Special architecture for monitoring ADC
27	BNL Data transmission		Test chip for transmission without repeater
28	Bandgap/Tmonitoring		Test chip Bgap/Tmon as in MOSAIX

Evolution of MLR1 test structures in view of **ALICE 3** upgrade

APTS SF:

- Several size implemented (20-50μm)
- Study maximum pixel pitch
- Study radiation tolerance of different splits

❖ Variant with same pitch of MOSAIX: could give hint on split selection

APTS OA:

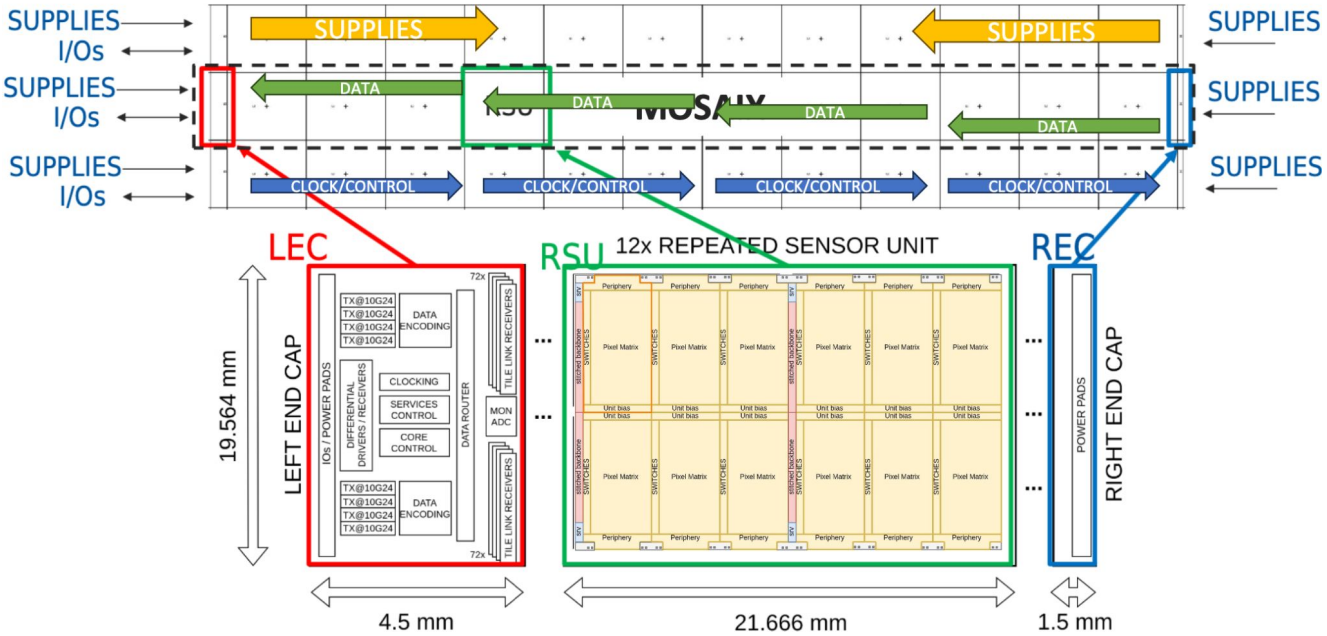
- Charge collection time and time resolution of different splits

DPTS:

- Sensor + FE reference

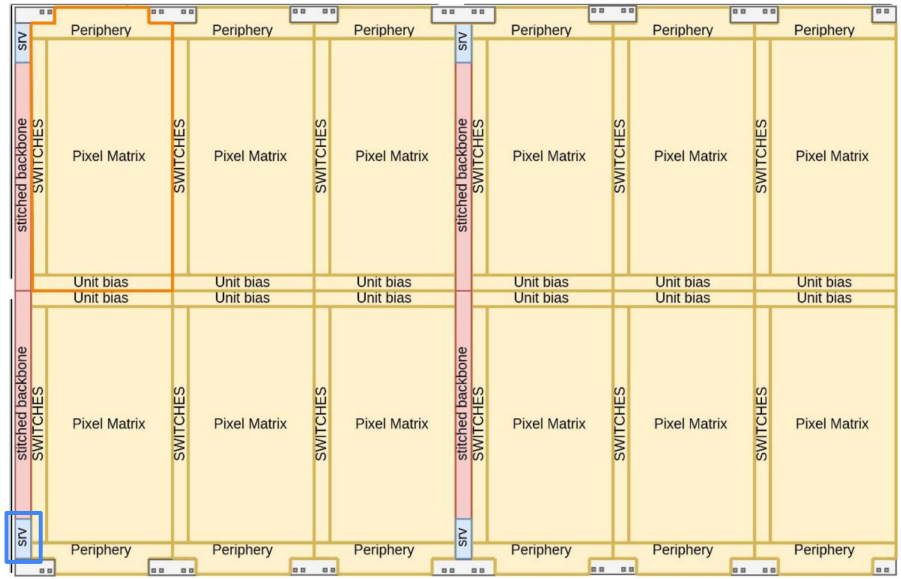
Same test system as MLR1, testing plan not yet prepared

What is MOSAIX?



Change of paradigm: MOSAIX = **Full Module** on silicon die (≈ ITS2 Stave)
LEC (Control, Powering, Data encoding, serialization and transmission) + 12 RSU
babyMOSAIX: mini module with 1 LEC + 1RSU.

Tile Variants

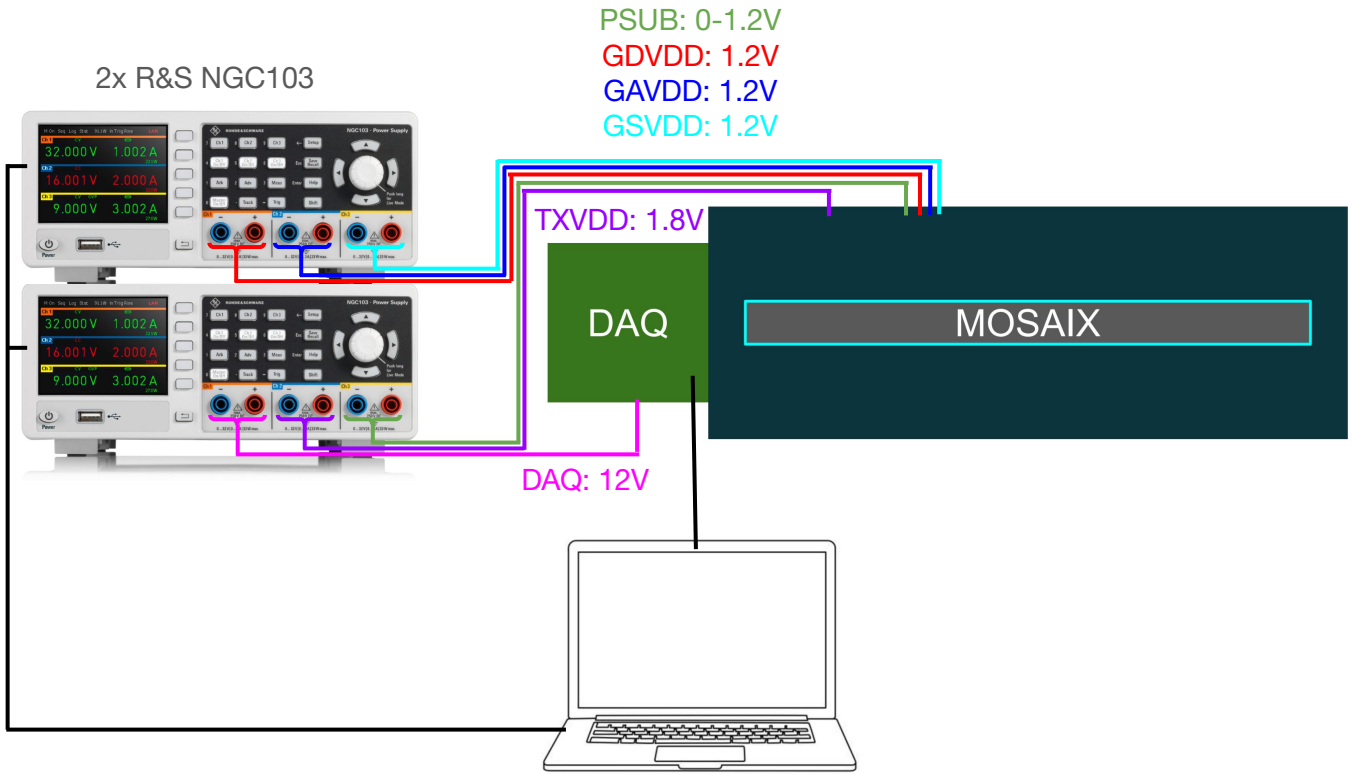


	RSU TILE											
	1	2	3	4	5	6	7	8	9	10	11	12
MOSAIX FE baseline	X			X			X			X		
Smaller input transistor (-40%)		X			X			X			X	
Longer VCASB transistor (+150%)			X			X			X			X
Antenna diodes on bias nets				X	X	X				X	X	X
Baseline biasing	X	X	X	X	X	X						
Temp. compensating biasing							X	X	X	X	X	X

Each RSU is made of: 1

- 12 tiles each implementing a different FE variant
- 4 service nodes that control 3 tiles each (also physical switches to power individual tiles)

Mosaix Test System



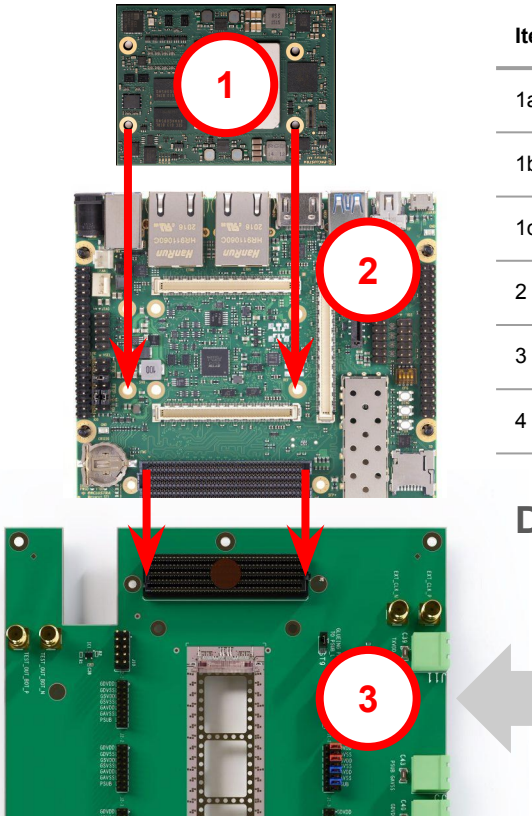
DAQ Board:
Enclustra ST1 base board + Enclustra AA1 FPGA

Biases provided directly by **Power Supply** (No proximity card):

- 6 channels needed
- Preferred model R&S NGC 103 (other models with USB TMC protocol could be used after noise profile validation, e.g. HMP4040)

PC communication via USB 3.0

Mosaix Test System



Item		Unit price (CERN via EDH)	Reference
1a	FPGA module	666,60 CHF	Enclustra ME-AA1-270-3E4-D11E-NFX3
1b	FPGA module rework	200,00 CHF	Enclustra-provided BoM & placement
1c	Heat sink	29,70 CHF	Enclustra ACC-HS4-SET
2	Base board	289,30 CHF	Enclustra ME-ST1-W
3	(baby)MOSAIX carrier	–	Design: A. Junique / J. Morant
4	Power supply (2x)	1241,00 EUR	Rhode & Schwarz NGC103

Distribution and support coordinator: G. Usai @ CERN

Mosaix testing plan:

Basic testing / Mass testing

GOAL:

- Determine if module is working
- Production yield

Standardized testing routines to be executed in a predetermined sequence

To be done for all chips before further testing, and repeated on all chips available to acquire sufficient statistics

Large part will be performed with wafer prober

Detailed characterization

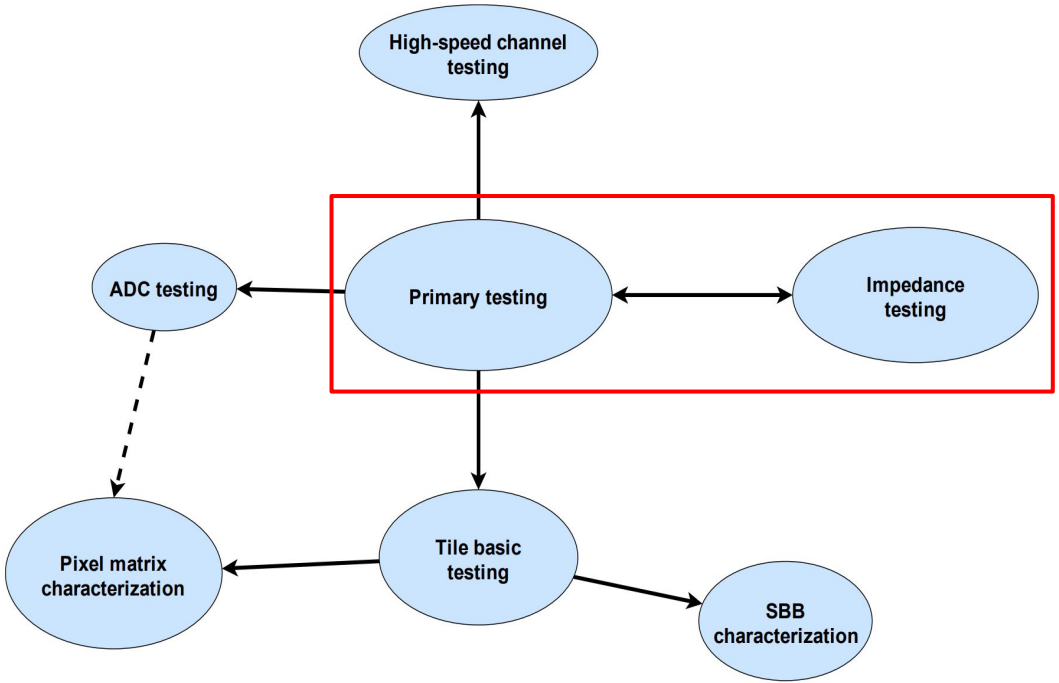
GOAL:

- Optimize working condition of modules
- Study performance

Only for a small subset of functional chips

Include lab measurements, testbeam measurements and study of single event effects

Basic testing plan



Primary testing:

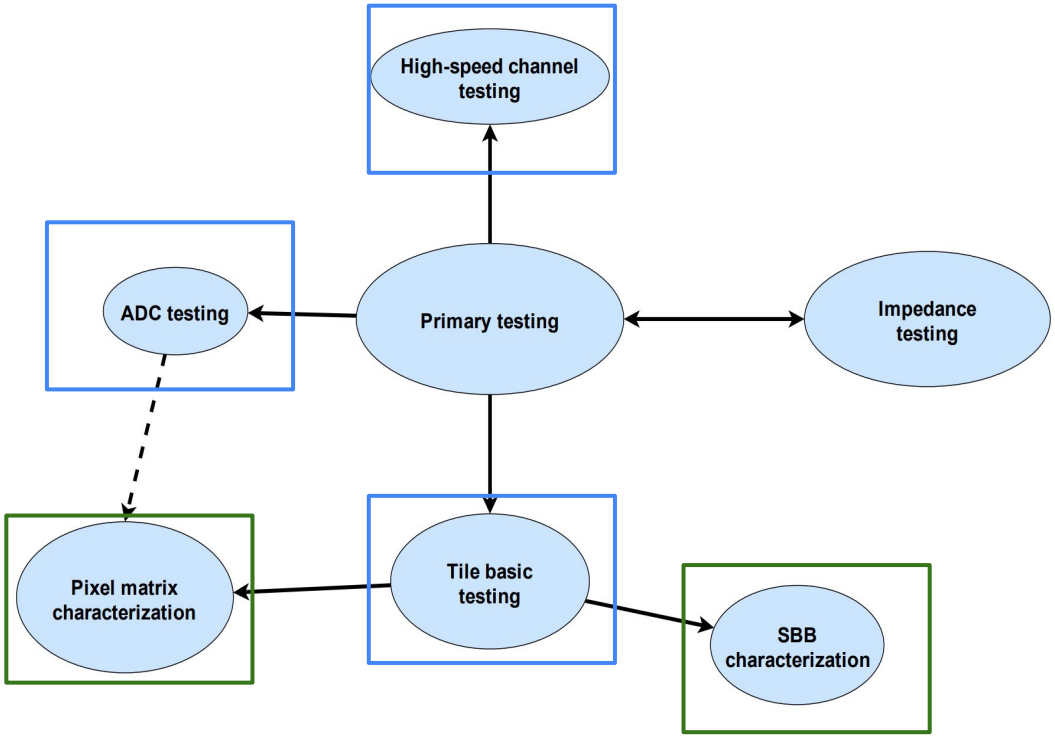
1. Service powering
2. Service slow control
3. Global powering
4. LEC core slow control

Impedance testing:

Measure impedance between different supply, ground and substrate nets

Required before any other test
Different setup required for precise current monitoring

Basic testing plan



After primary testing can be tested in any order:

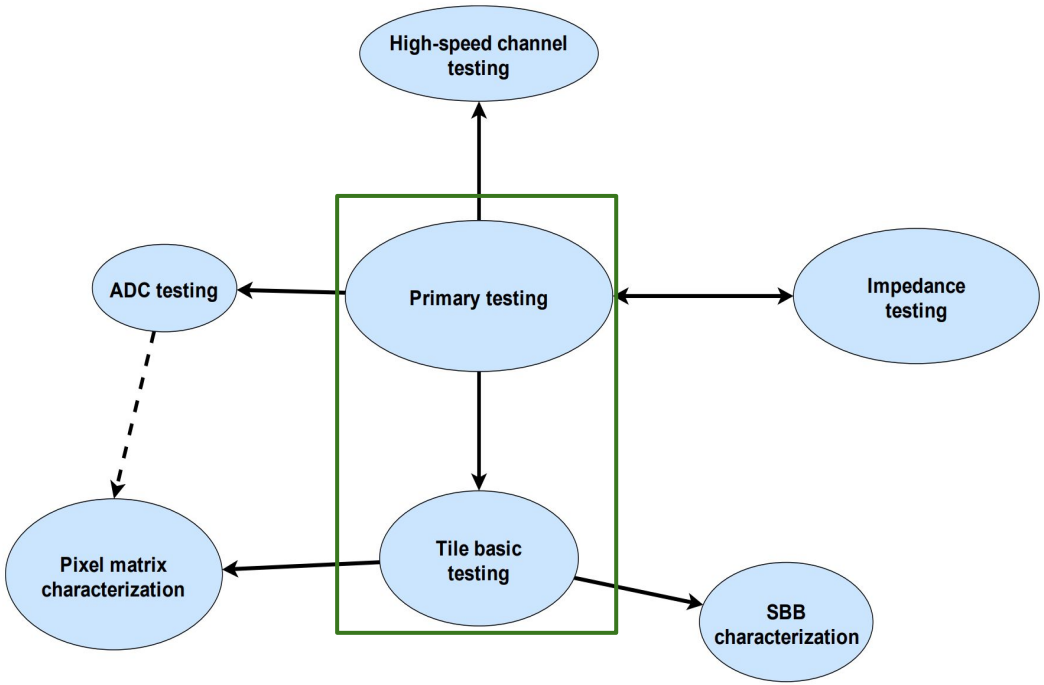
- High speed channels
- Tiles (Powering and Control)
- ADCs

Could be parallelized with several setups

After that pixel matrices and SBB can be characterized:

- Pixel Matrix: FHR, threshold
- SBB: Data transmission errors

Testing procedure preparation



Detailed procedures for primary and tile testing already provided by designers

SW development of testing routines has started!

→ Interested? **Join the effort!**

In-depth matrix characterization

Lab measurements:

1. Simple operating point finding
2. Threshold spatial distribution and uniformity
3. FHR spatial distribution and uniformity
4. Noise injection via different supplies.
5. TID and proton irradiation
6. Verify FE temperature compensation

Ecc …

Testbeam measurements:

MIPs: Detection efficiency and spatial resolution

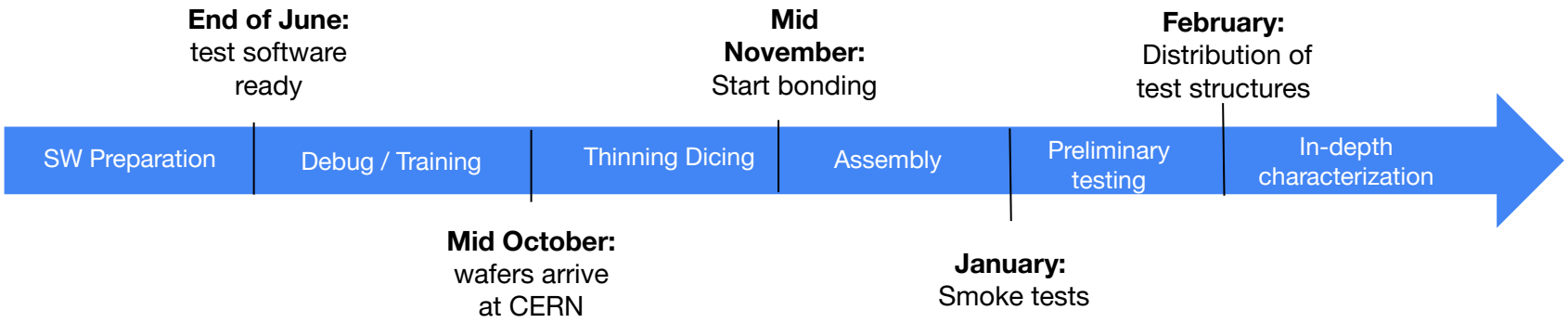
Study for different: pixel flavors, splits, biasing parameters, supply voltages, temperature, readout modes/frequency

IRRADIATION levels: NIEL 1e13, TID 10 and 100kGy, protons at ITS3 requirements

Low energy protons/light-nuclei: Study Single Events Effects

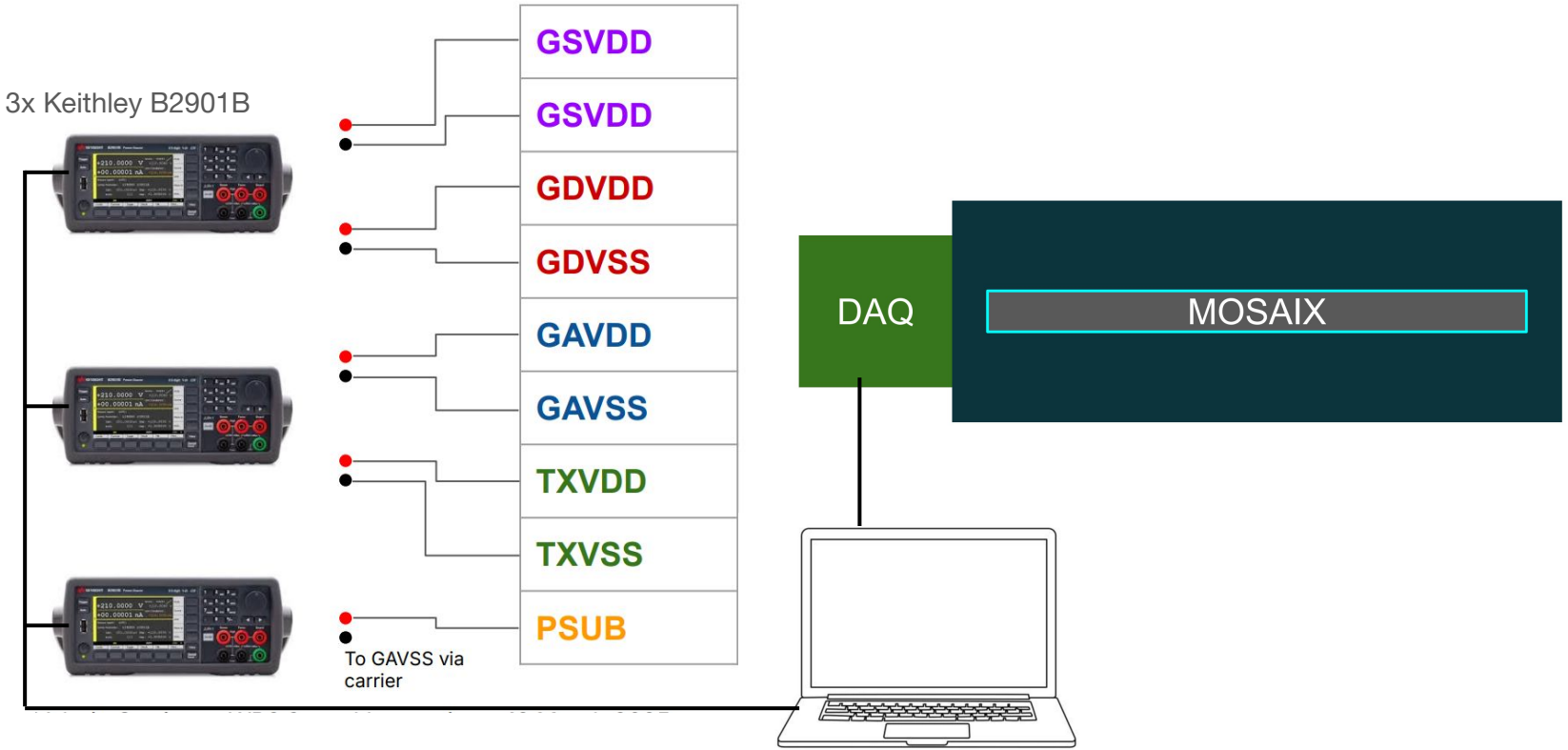
Single Event Upset and Single Event Latch-Up

Indicative timeline

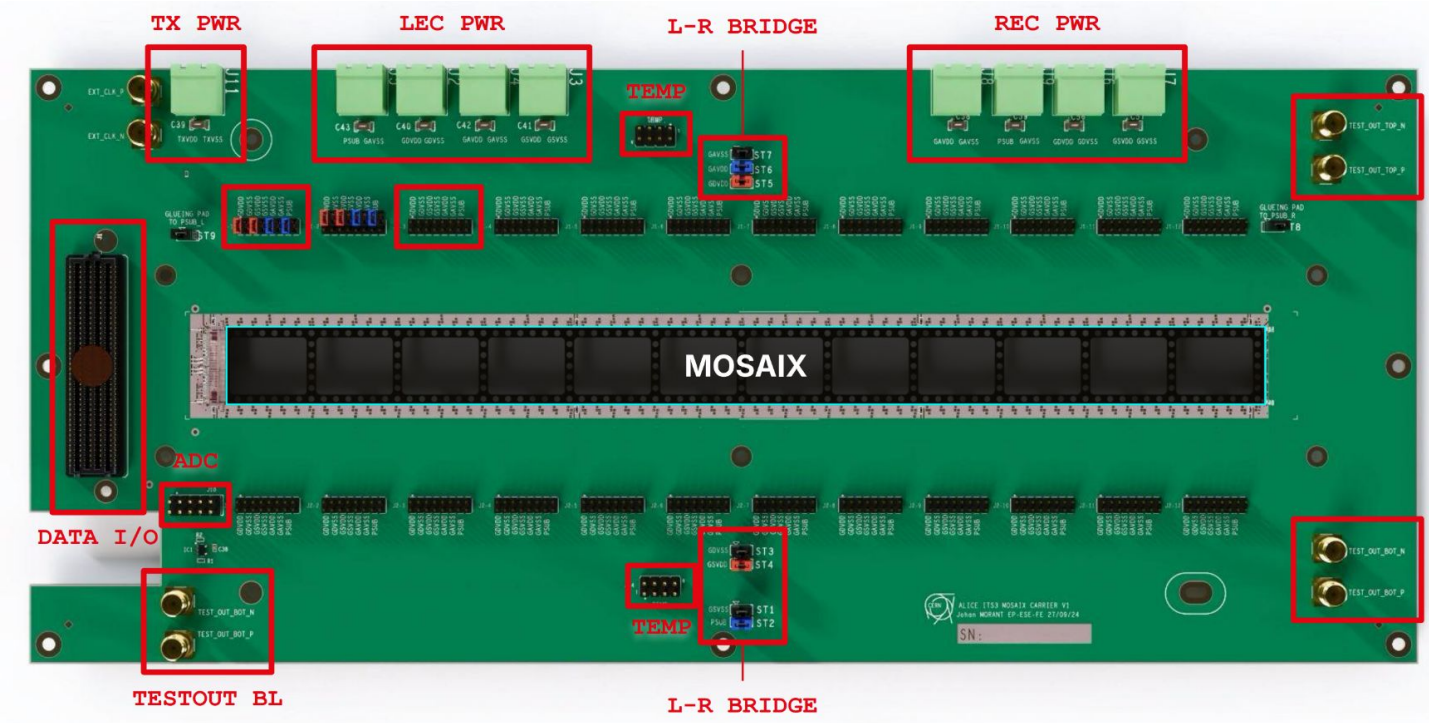


Backup

Setup for impedance/primary testing



MOSAIX carrier



Powering
- LEC
- LEC + REC
- Single units
- Glueing pads to PSUB

Monitoring
- V drop along BB
- ADC calibration
- Testouts
- Temperature