ER1 characterisation status and results

Giacomo Contin

Collection of slides from Anna, Miko, Ivan, Naseem, Gregor
Work done by many (not by me!)

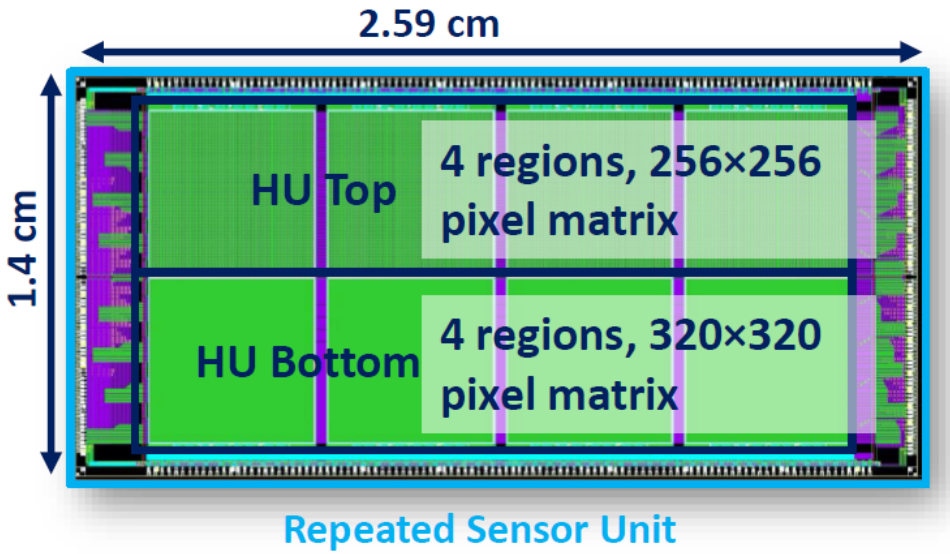
Meeting on ITS3 ER1/ER2 Characterisation @INFN
27 March 2025

UNIVERSITÀ DEGLI STUDI DI TRIESTE
Dipartimento di Fisica
Dipartimento d'Eccellenza 2023-2027
INFN TRIESTE

Outline

- (baby-)MOSS main characteristics
- Performance after irradiation
- Parameter exploration
- Issues found
- Yield study
- Conclusions

(baby-)MOSS pixel matrix characteristics



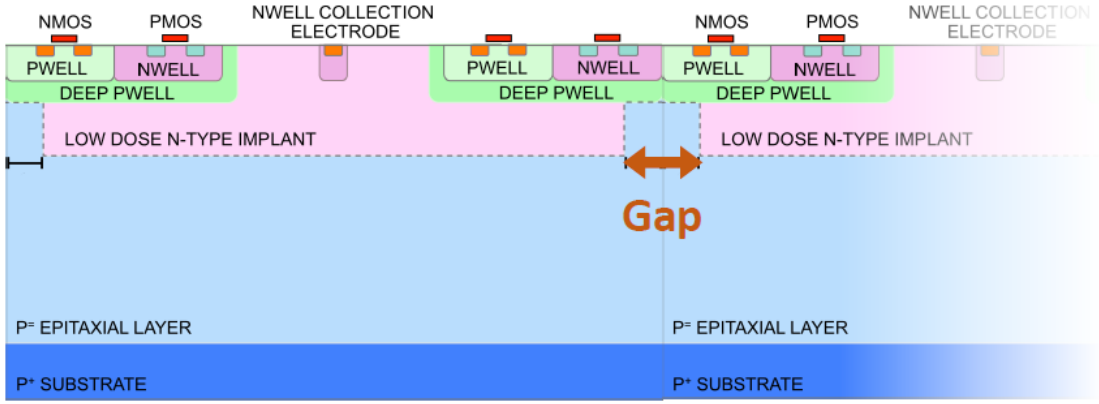
Each Repeated Sensor Units (RSU) has

- 2 **Half Units** (HU) with 4 regions (5 front-end variants)

	Region 0	Region 1	Region 2	Region 3
TOP	Standard	Larger input transistor (M1)	Larger discriminator input transistor (M11)	Larger common-source transistor (M2)
BOTTOM	Standard	Standard	Standard	Slightly different layout

1 2 3 4 5

- Pixel pitch is: 22.5 µm (top HU), 18.0 µm (bottom HU)



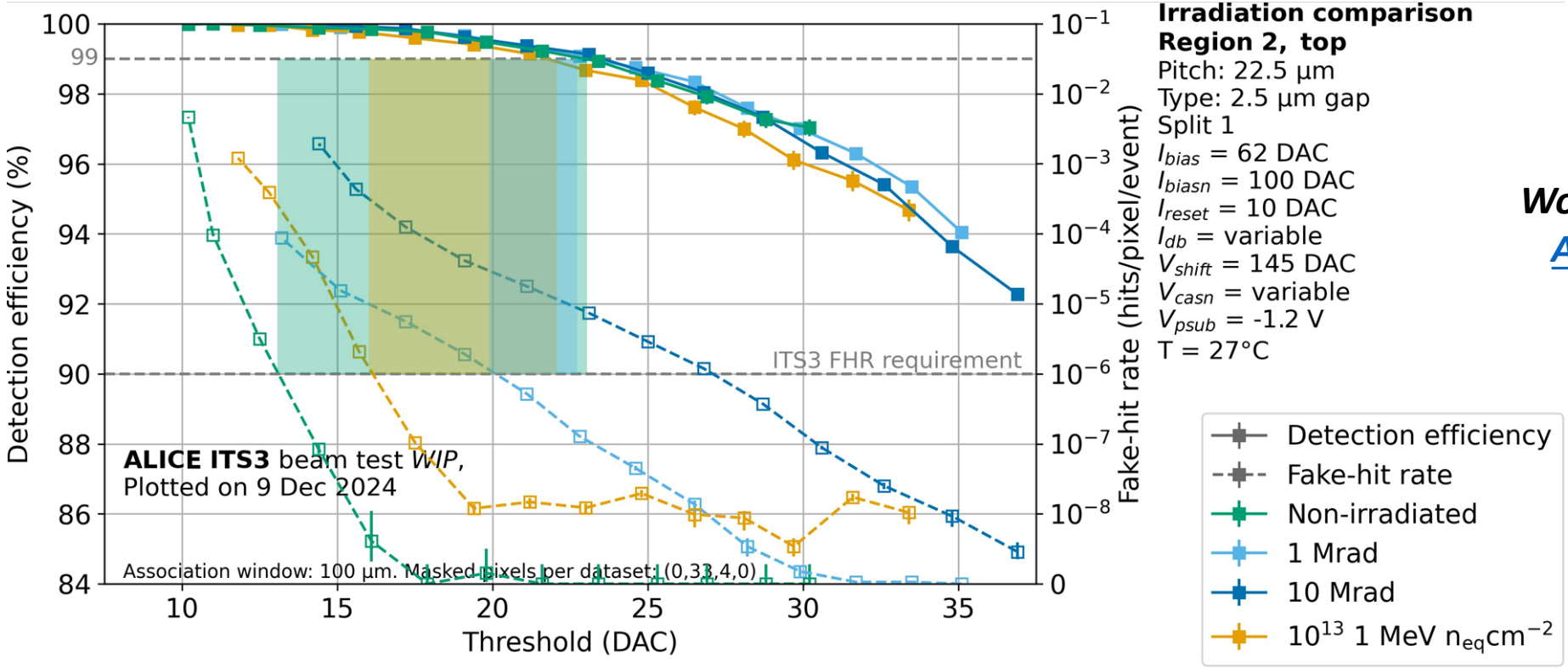
Pixel cross section, not to scale

2 splits available:

Split	Gap top	Gap bottom
1	2.5 µm	2.5 µm
2	5.0 µm	2.5 µm

Performance after irradiation

- Main message: operational margin exists at ITS3 requirements (TID-NIEL separately)



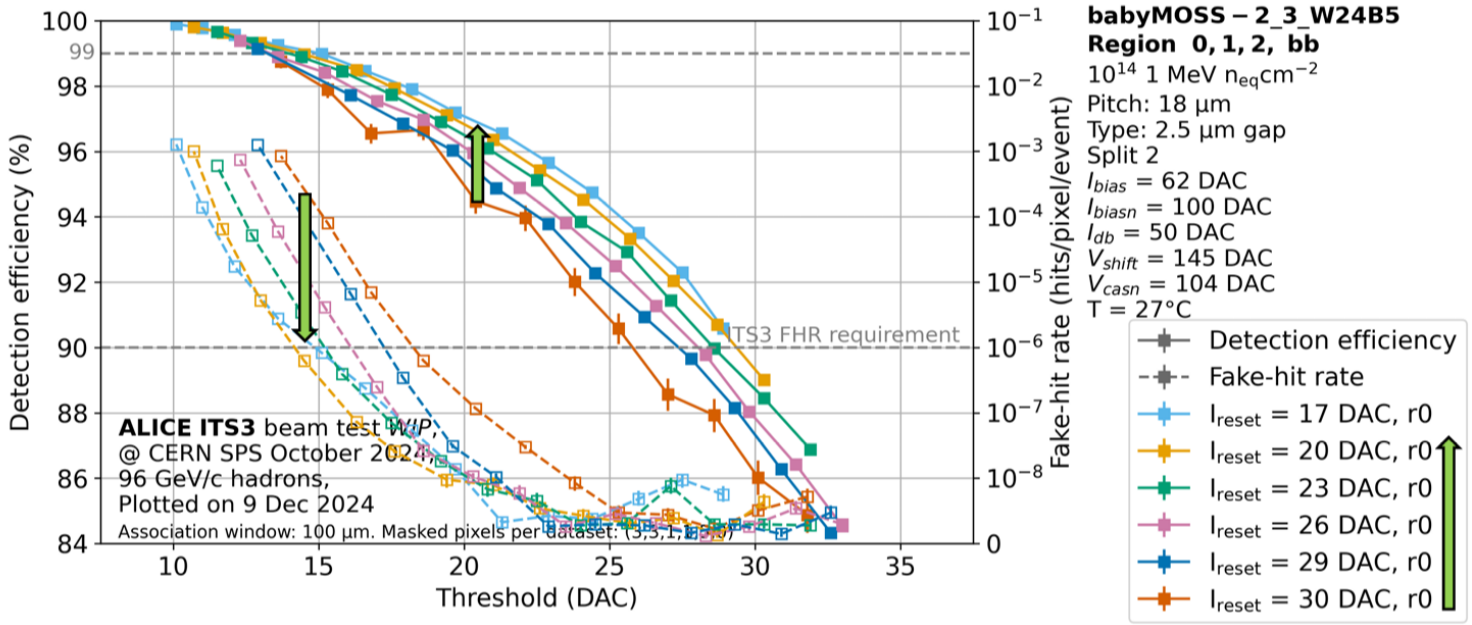
Work in progress
Anna @ WP3

- *As a reference, requirements for ALICE 3 Middle Layers are TID ~ 1.5 Mrad / NIEL ~ 5 x 10^{13} n cm^{-2})*

Key takeaways from MOSS characterization results

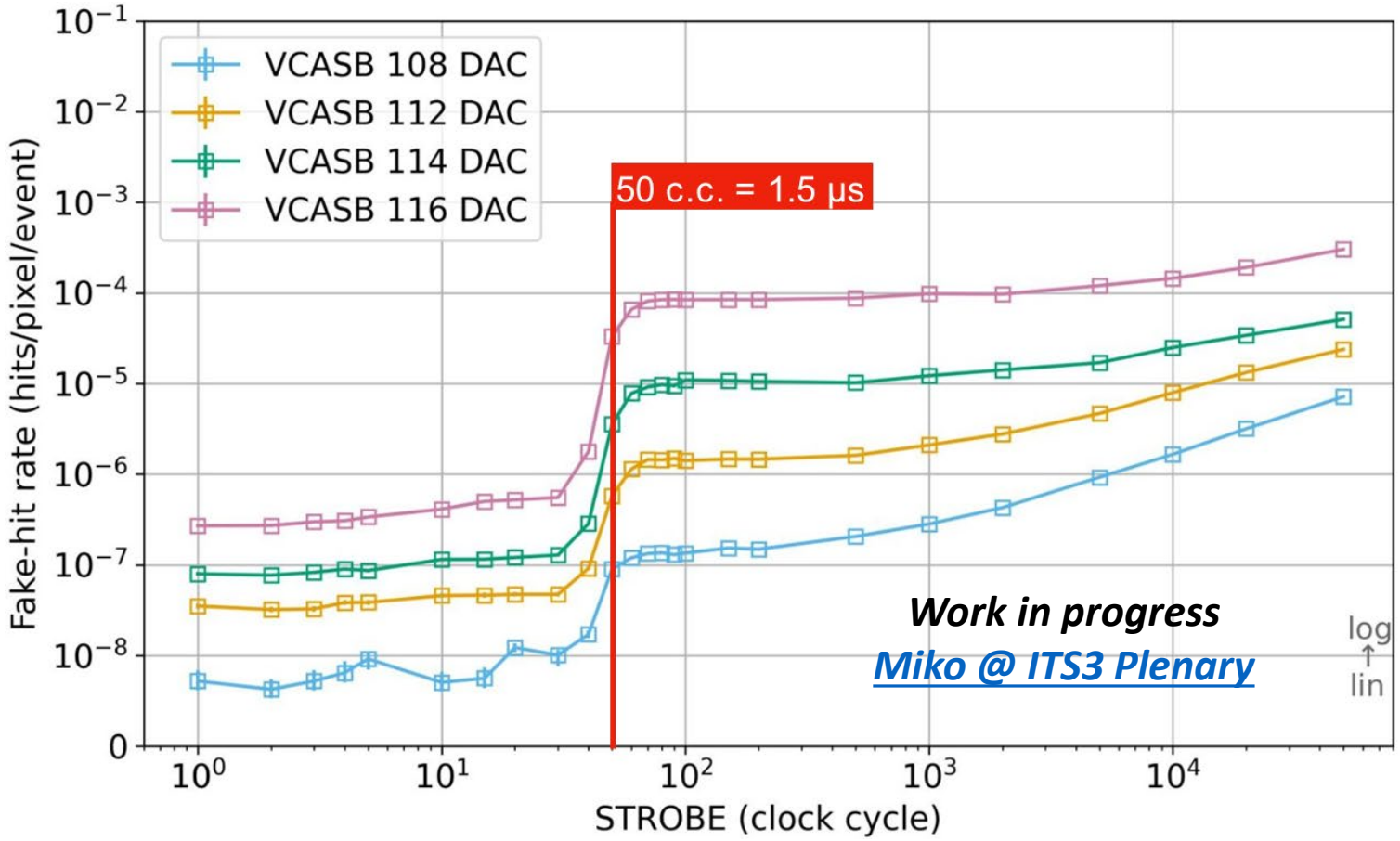
- Non-negligible chip-to-chip variations
- Different regions (front-end variants) have comparable performance
- Larger pixel pitch shows a hint of better efficiency
- Split-to-split variation is compatible with chip-to-chip variations
- Lowering I_{reset} increases the operational margin

Work in progress
Anna @ WP3



Fake hit rate dependent on strobe length

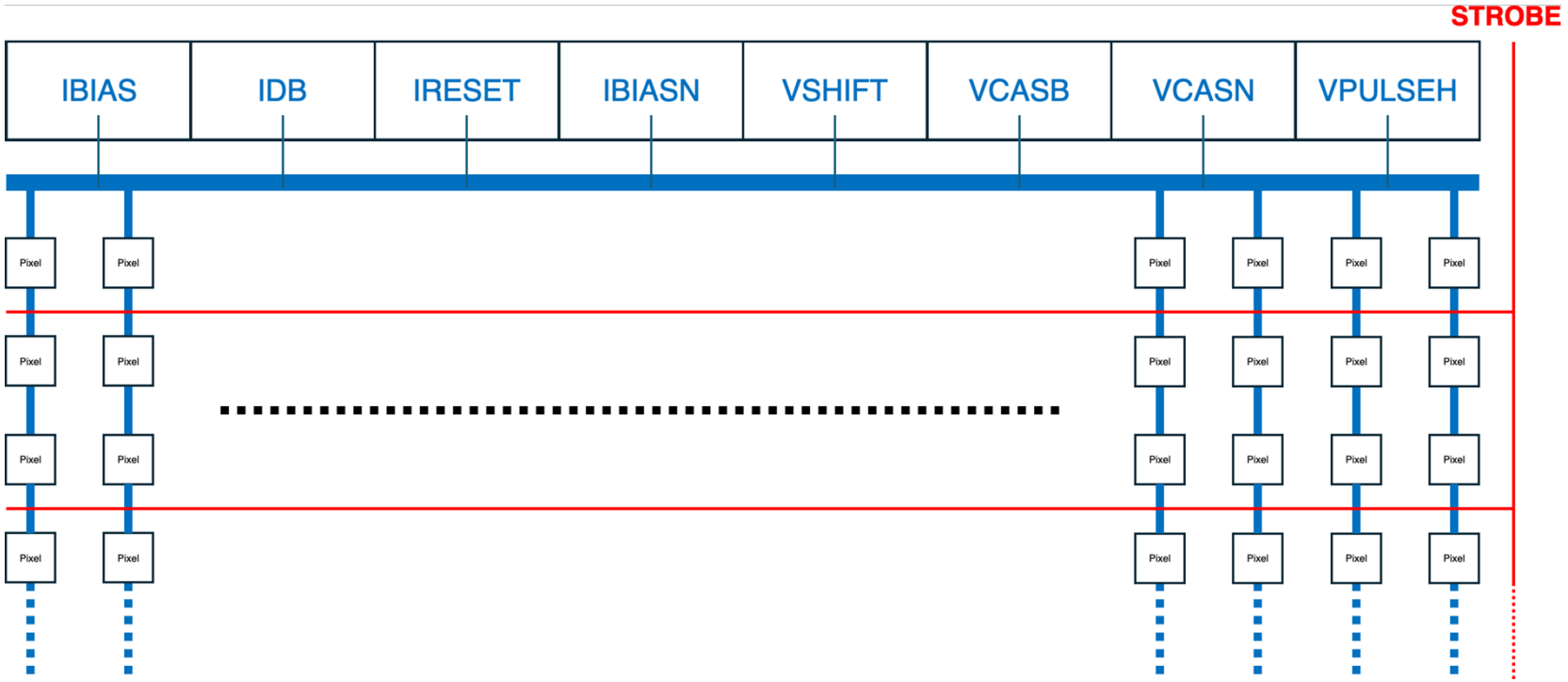
- Fake-hit rate dependence on strobe signal length



babyMOSS – 2_2_W21D4
tb region 0
Pitch: 22.5 µm
Type: 5.0 µm gap
Split 2
I_{bias} = 62 DAC
I_{biasn} = 100 DAC
I_{reset} = 10 DAC
I_{db} = 50 DAC
V_{shift} = 145 DAC
V_{casn} = 104 DAC
V_{casb} = variable
V_{psub} = -1.2 V
Strobe length = variable
T = 20°C

Analog biasing and strobe signal distribution

- Attributed to crossing of analog biasing and strobe signal distribution lines
- Effects of shorter strobe signal on efficiency currently investigated with testbeams
- *This specific interaction will be removed in MOSAIX, designers aware of similar risks*

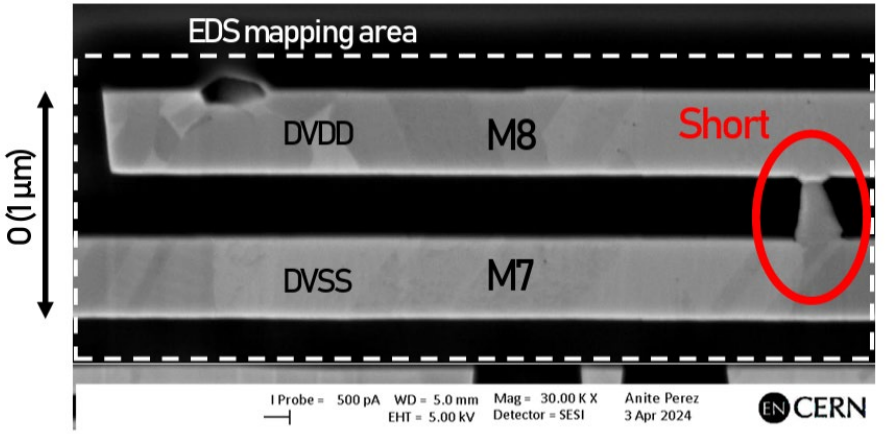


Work in progress

Miko @ ITS3 Plenary

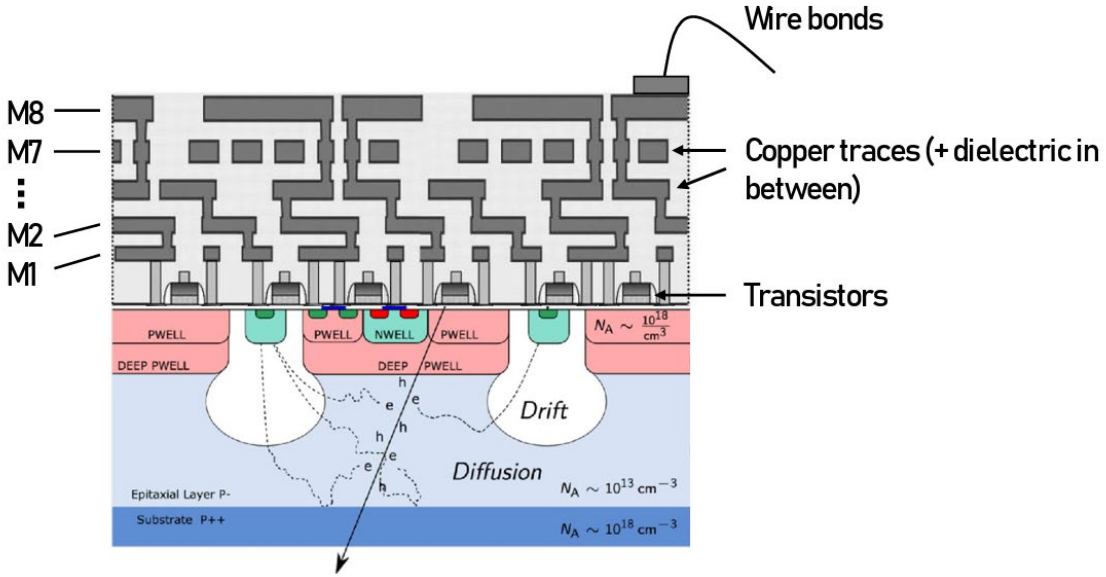
Shorts in MOSS power grid

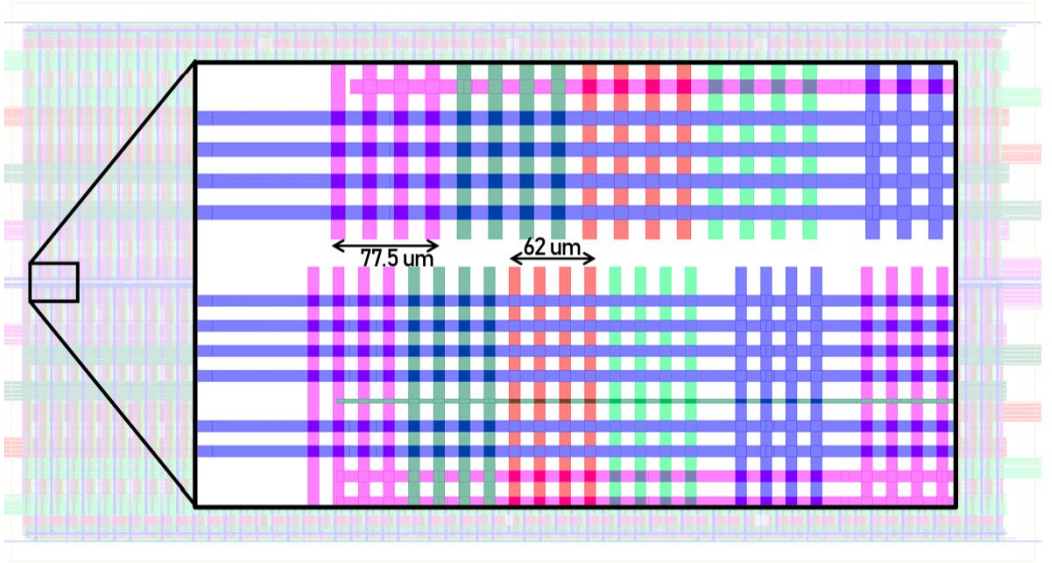
- Main cause for powering issues
- Foundry confirms processing issue in M7/M8
- *For next chips (ER2, MOSAIX): M7/M8 will be replaced by a new (thicker) metal stack*



MOSS power grid

Gregor @ TWEPP2024



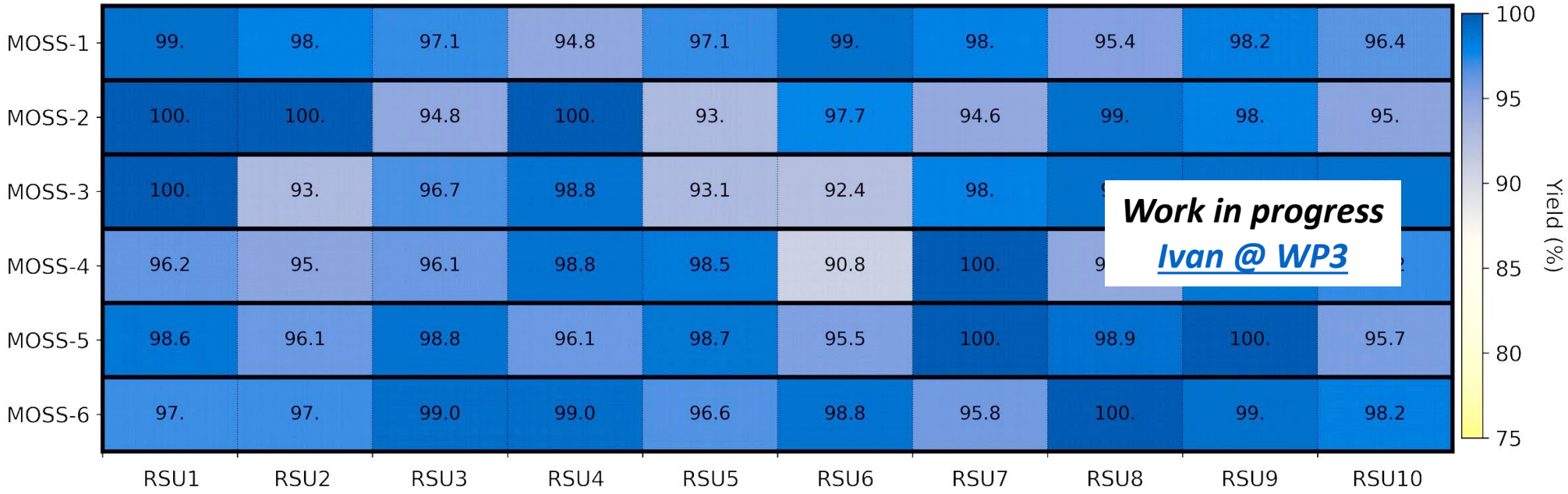


PSUB
AVDD
AVSS
DVDD
DVSS

M8: vertical
M7: horizontal

Yield: MOSS as a proxy for MOSAIX

- RSU powered and tested directly (not from LEC)
  - Integrated over the wafers, only powerable regions
  - Takes into account only defects directly transferrable to MOSAIX
  - No visible sistematic dependence on wafer, nor on position in the wafer
  - Bottom regions slightly better than Top
- *Extrapolated yield for 5-6 RSU sequence > 85% (interesting also for ALICE 3 ML)*



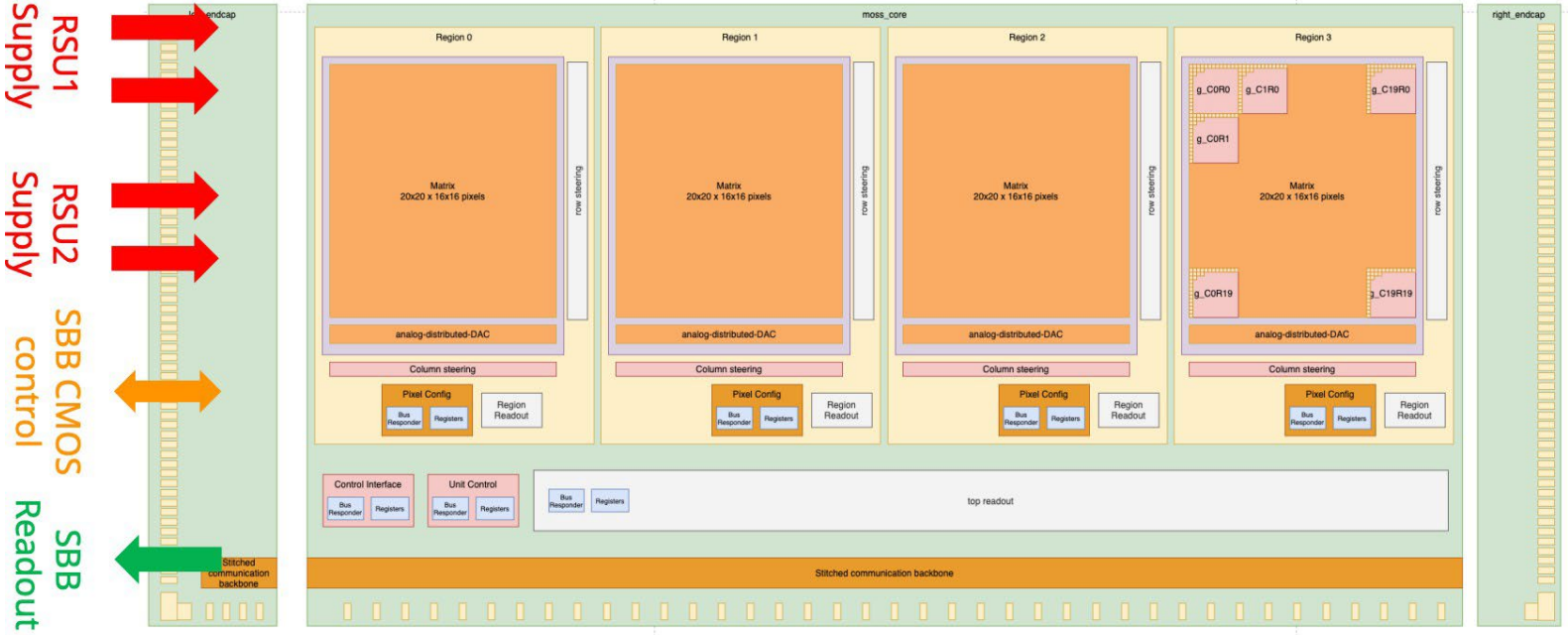
Powering&Reading out via LEC

- LEC tests successful. Working for power on scan, register scan, threshold scan, fake hit rate scan.
- Threshold and FHR scans seem compatible.

- Unexpected protocol errors occurring sporadically are under investigation

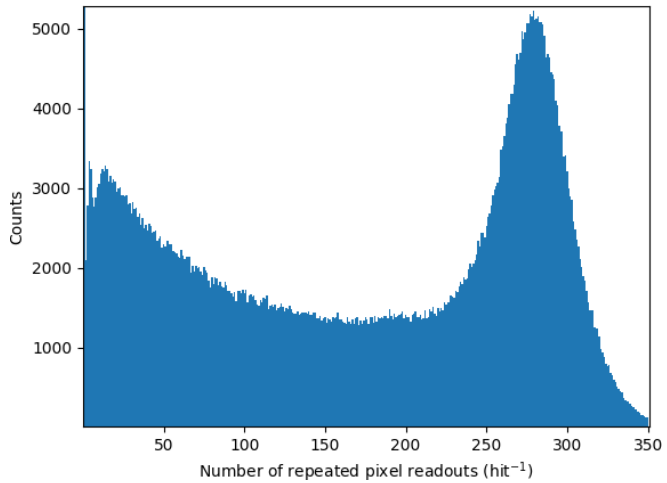
Work in progress

Naseem @ WP3



Conclusions

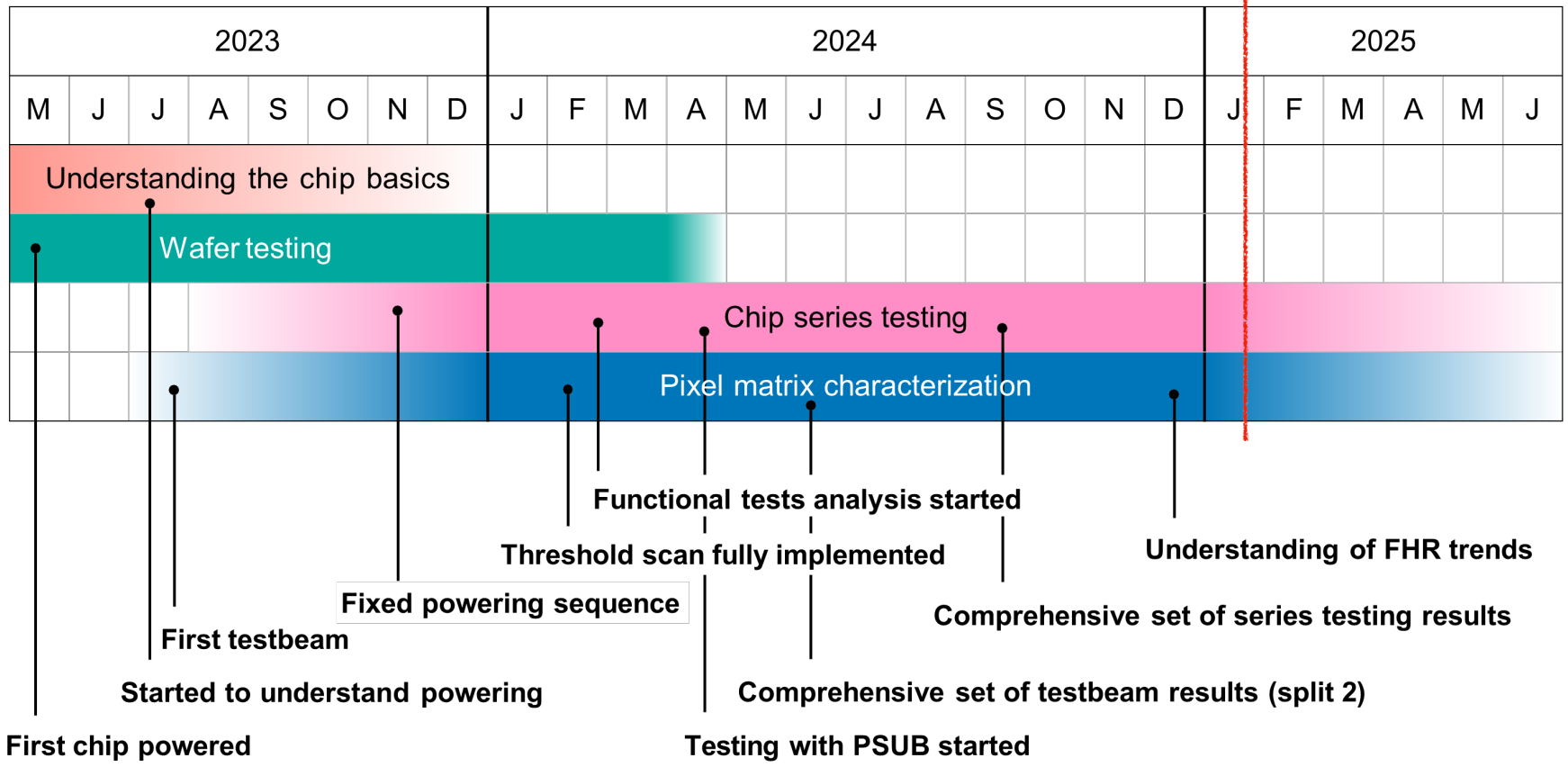
- (baby-)MOSS extensively characterised in lab and testbeams
- Operational margin exists at ITS3 expected radiation levels
- Tuning of operating parameters can improve the performance
- Several issues spotted: solutions are in place for ER2
- Projected yield is quite satisfactory so far
- Many studies currently ongoing, e.g. ToT



- *First indications towards an ALICE 3 Middle Layer sensor*

Thank you for your attention!

MOSS testing timeline



ER2 expected timeline