ARCADIA sensors development

Tracking and Timing with LFoundry 110nm CIS

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INFN Torino

INFN ARCADIA

7th RD_FCC IDEA Study Group meeting

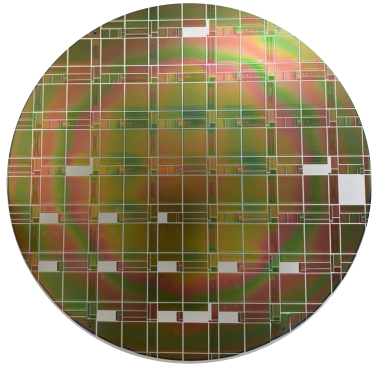
22nd April 2025

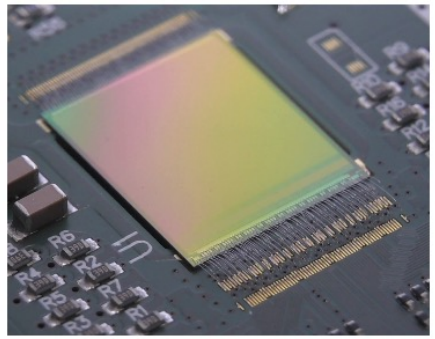
ARCADIA FDMAPS R&D at INFN

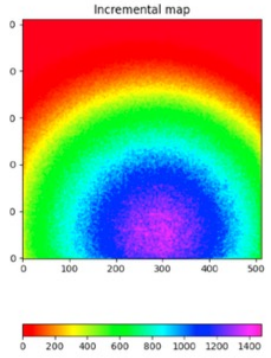
Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

CMOS sensor design and fabrication platform on LF11is technology:

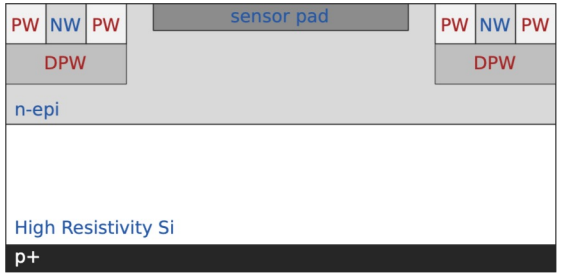
- Sensor R&D and Technology, CMOS IP Design and Chip Integration, Data Acquisition
- Main Demonstrator full-chip FDMAPS for Medical (pCT), Future Leptonic Colliders and Space Instruments
- Scalable FDMAPS architecture with very low-power: 10 mW/cm2
- Custom BSI process allow to develop fully-depleted thick sensors (400µm) for X-ray imaging
- Fully-depleted monolithic active micro strips with fully-functional embedded readout electronics
- Ongoing R&D for the implementation of monolithic CMOS sensors with gain layer for fast timing







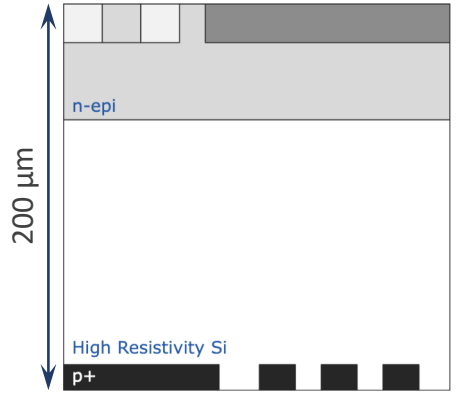
Sensor concept and substrates



- *n*-type high resistivity + *n*-epi layer (reduces punch-through current between *p*+ and deep *p*-wells) active region
- sensing electrodes can be biased at low voltage (< 1V)
- reverse-biased junction: depletion grows from back to top
- ongoing R&D: Fully Depleted pad sensors with gain layer

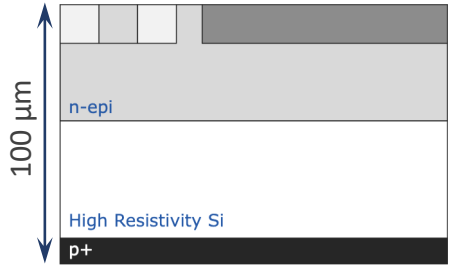
HR wafers - backside litho

thinning, **lithography**, backside ***p*⁺ implantation** and laser annealing, **insulators/metal** deposition and patterning



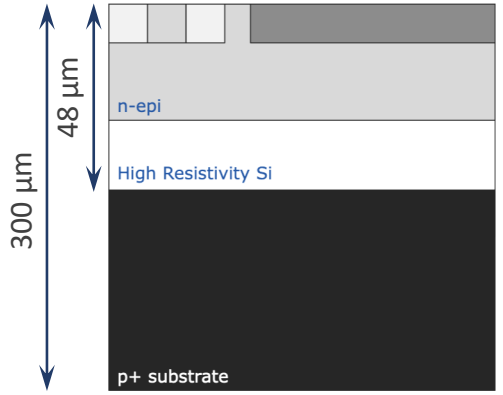
HR wafers NO backside litho

thinning, backside ***p*⁺ implantation** and laser annealing

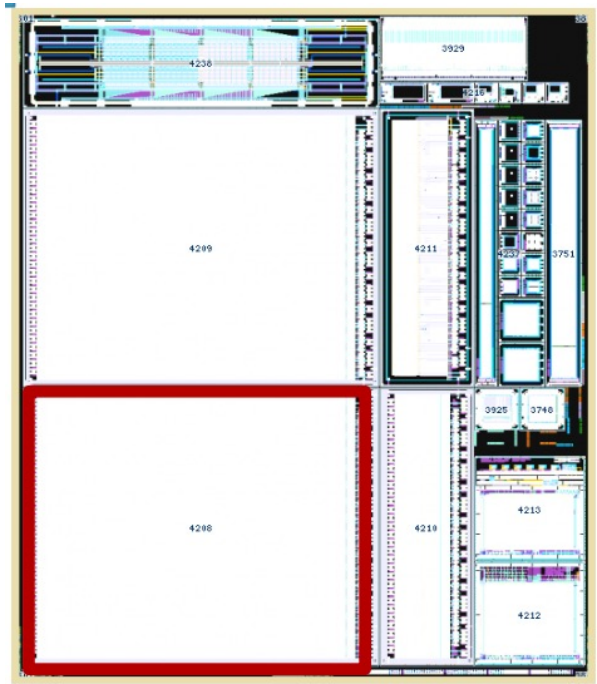


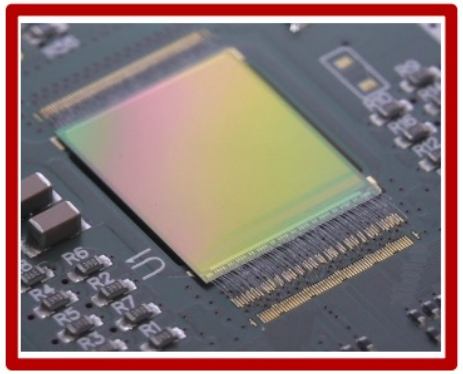
p+ wafers double epi

thinning to 100 or 300 µm total thickness



ARCADIA technology

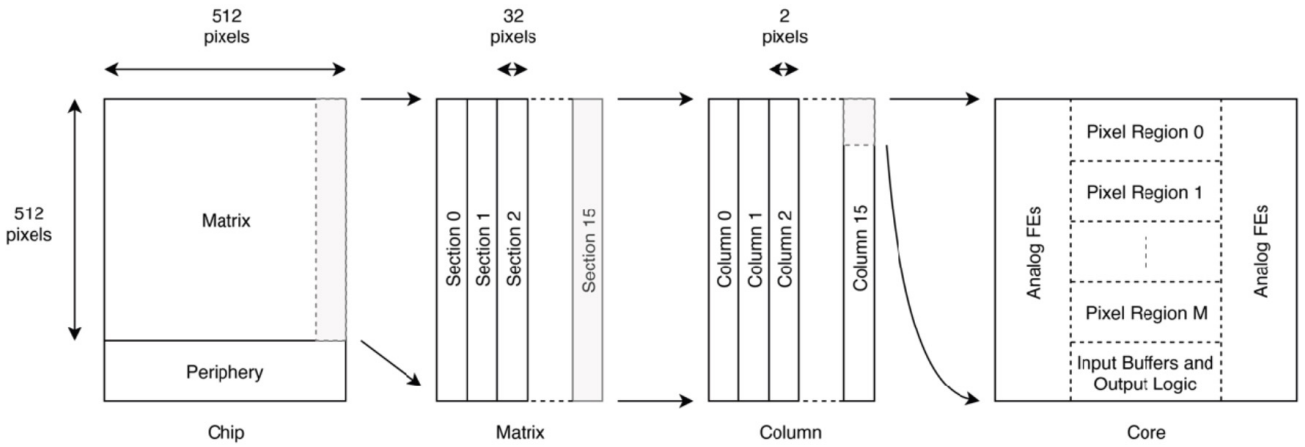


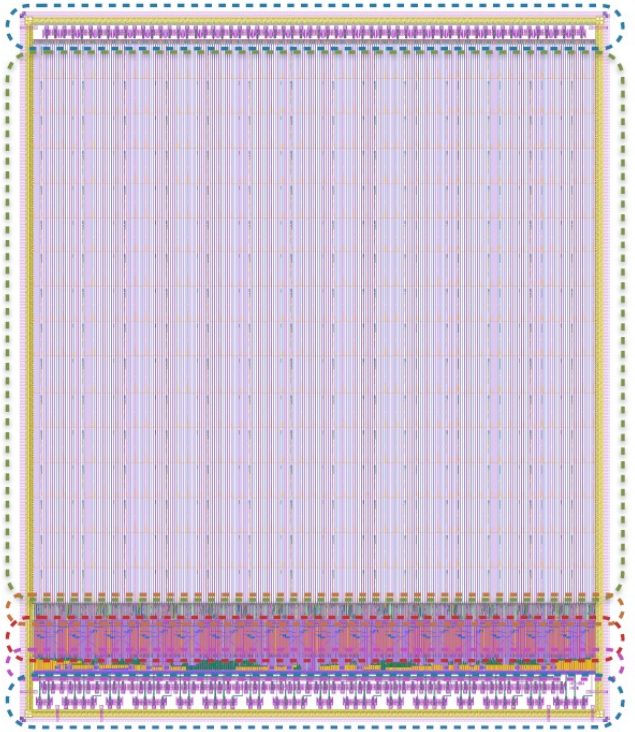


- ARCADIA-MD3 Main Demonstrator* (512 x 512 pixels)
- MAPS and test structures for PSI
- MATISSE Low Power for space applications
- pixel and strip test structures down to 10-µm-pitch
- ASTRA 64-channel mixed signal ASIC for Si-strip readout
- active pixelated strips with fully-functional readout electronics
- (ER2) HERMES: small-scale demonstrator for fast timing
- (ER3) Small-scale demonstrator of an X-ray multi-photon counter
- (ER3) Wafer splits with gain layer, new R&D towards timing
- (ER3) MADPIX*: multi-pixel active demonstrator chip for fast timing

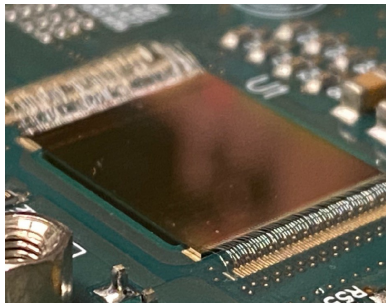
* today's presentation

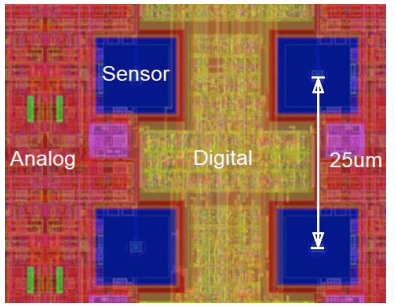
MD3: chip architecture



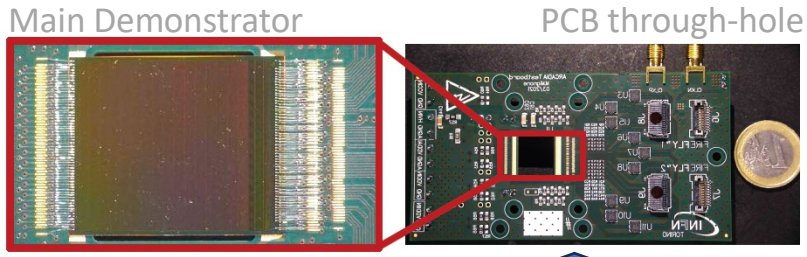


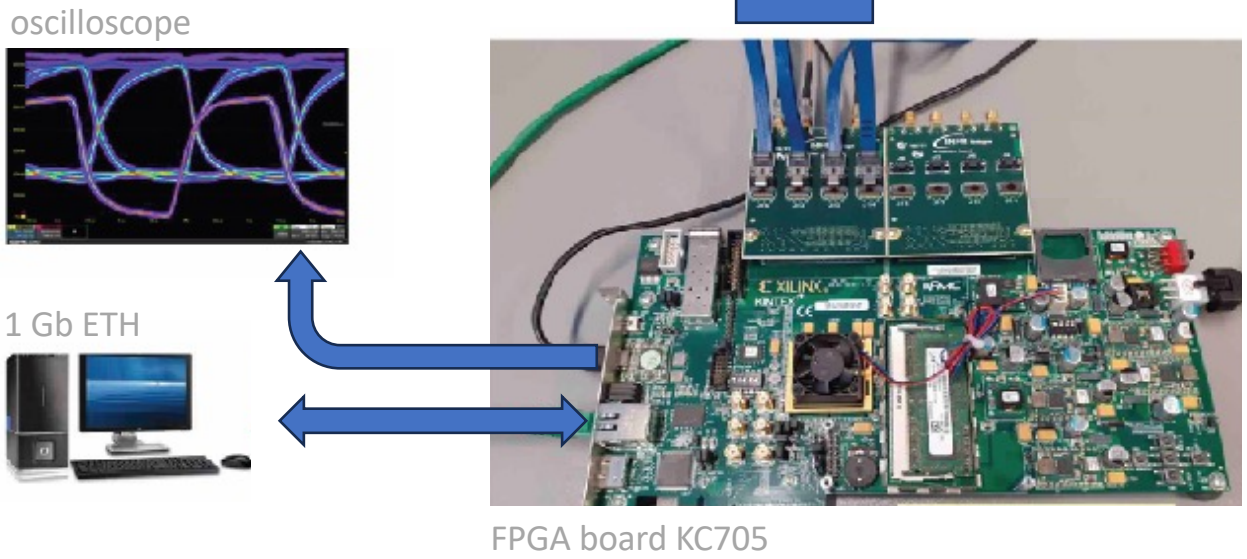
- Pixel **pitch**: **25 µm**
- Array core **area**: **1.28 cm × 1.28 cm** (262144 pixels)
- Electronics: **analog** and **digital**, with in-pixel **threshold** and **data storage**
- Architecture: **event-driven**, with active pixels sending their address to the chip peripheral circuits
- (Low) **power**: **10-30 mW/cm^2**
- (High) **event rate**: **100 MHz/cm^2**

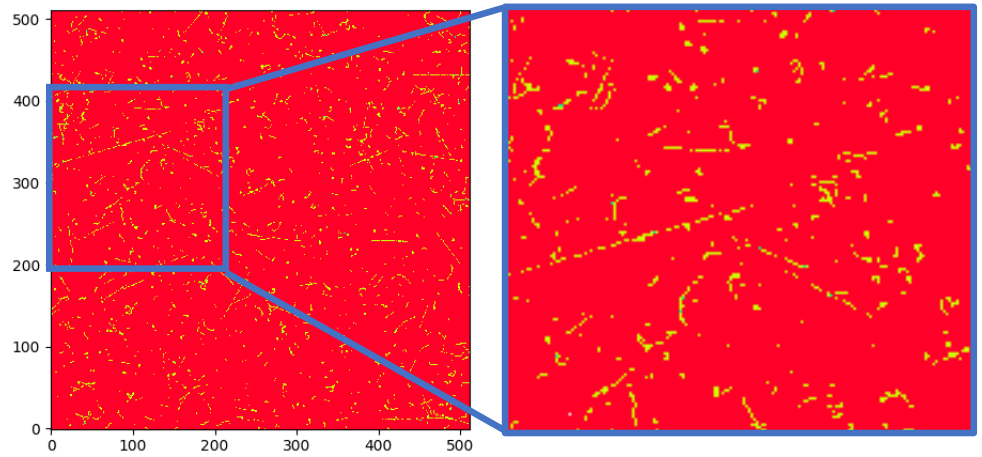




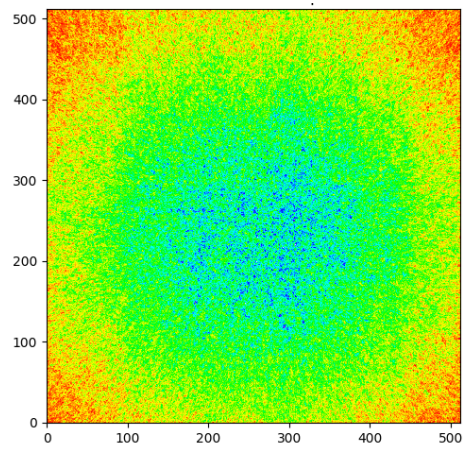
MD3: charged particles acquisition



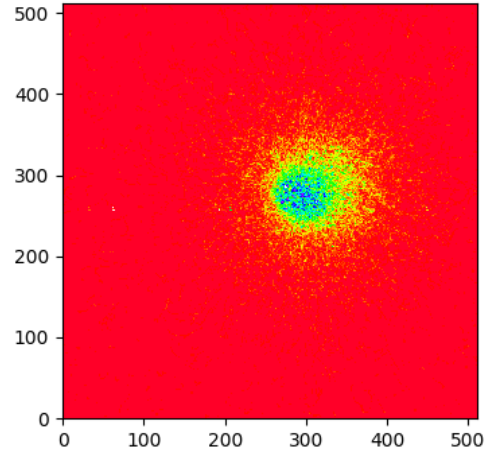




Cosmic rays acquisition (4h)



^{90}Sr beta source (1cm^2) 8 mm from the sensor surface

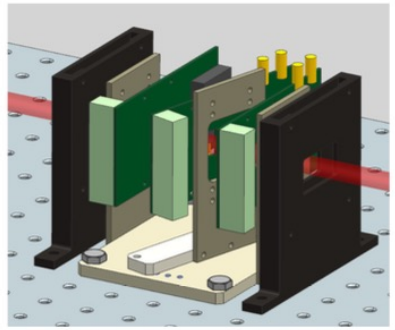
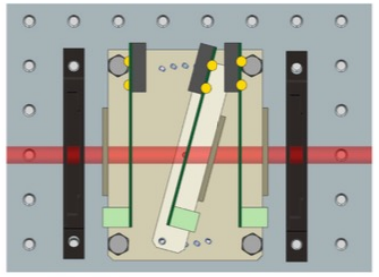
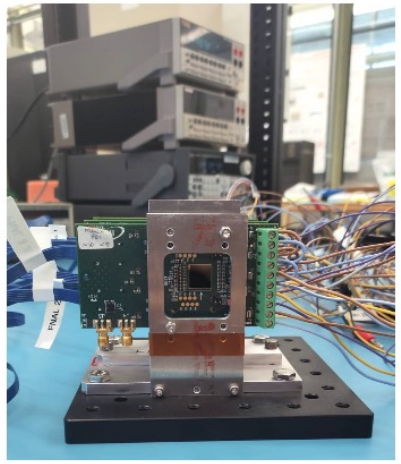
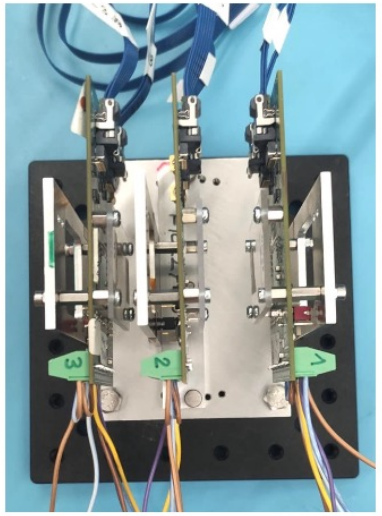


Collimated ^{90}Sr beta source
Collimator diameter: 1mm

- Total **power consumption**: **10 mW/cm^2** at low event rates
- **Design specification**: **20 mW/cm^2** at rates up to 100 Mevents/cm^2

MD3: testbeam w/ 120 GeV protons

- Mini-telescope with three 200-µm-thick ARCADIA-MD3 sensors
- Threshold, sensor HV and incidence angle parametrisation: study of cluster size, collection efficiency, spatial resolution

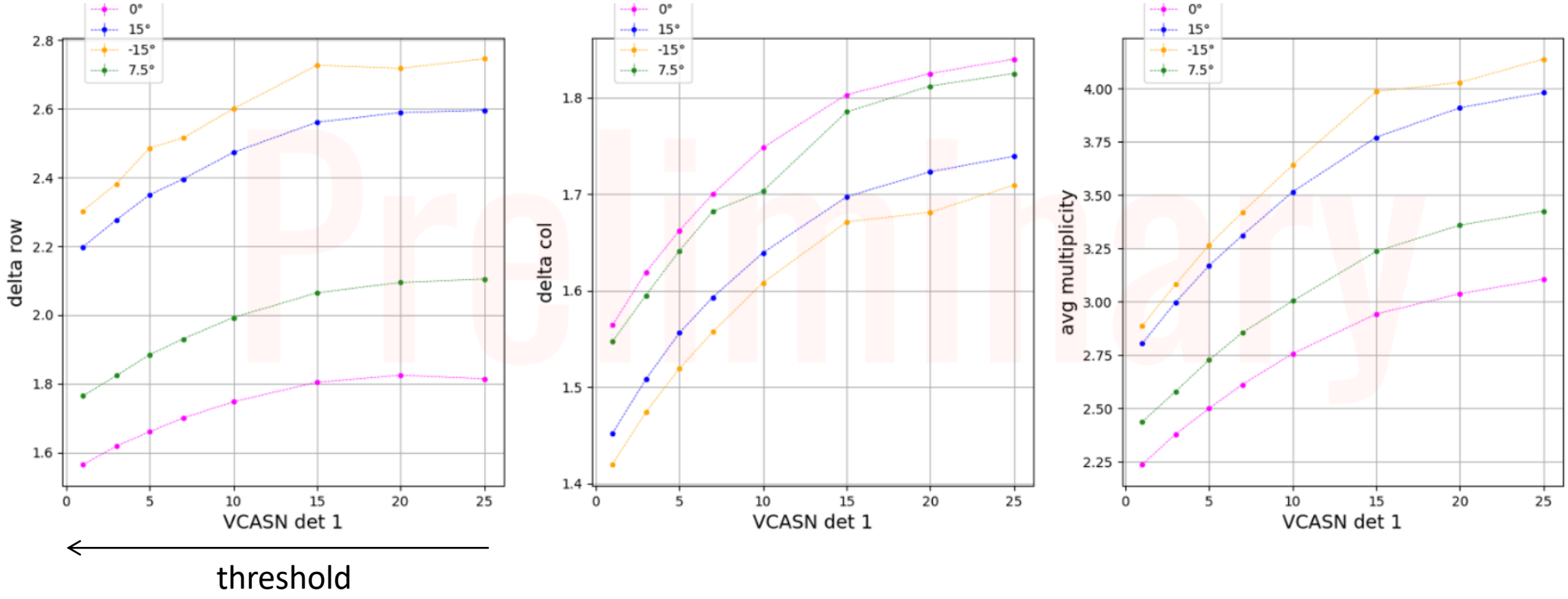





The INFN-PD Test-beam Team:
Sabrina Ciarlantini, Caterina Pantouvakis, Michele Rignanese, Alessandra Zingaretti, Piero Giubilato, Jeffery Wyss, Serena Mattiazzo, Chiara Bonini, Davide Chiappara, Devis Pantano, Patrizia Azzi e Rosario Turrisi

At FNAL:
Irene Zoi, Nicola Bacchetta, Artur Apresyan, Aram Hayrapetyan, Pierce Affleck

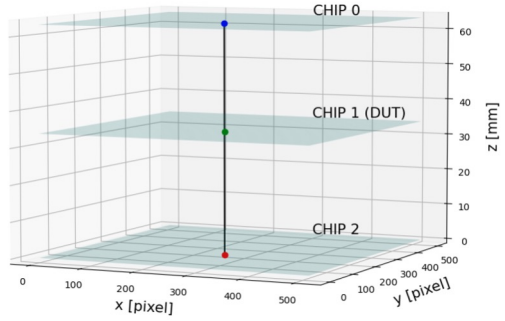

MD3: testbeam w/ 120 GeV protons

Cluster dimensions on the DUT as a function of the discriminator threshold (835 to 290 e^-) and incidence angle (0°, ±15°, 7.5°)



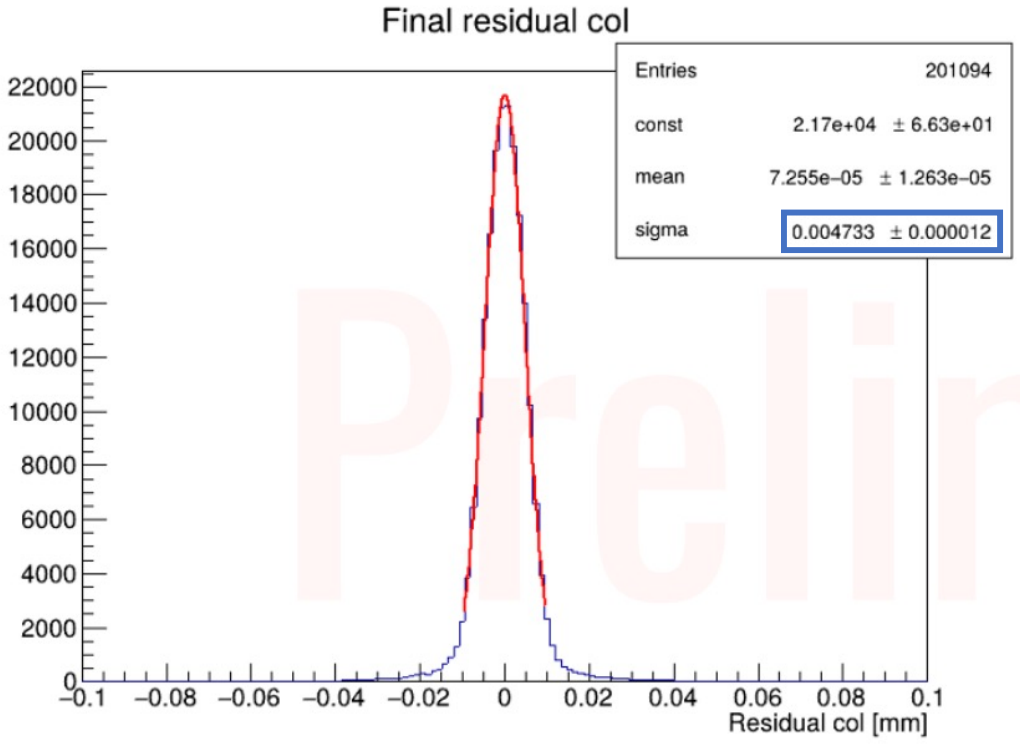
MD3: testbeam w/ 120 GeV protons

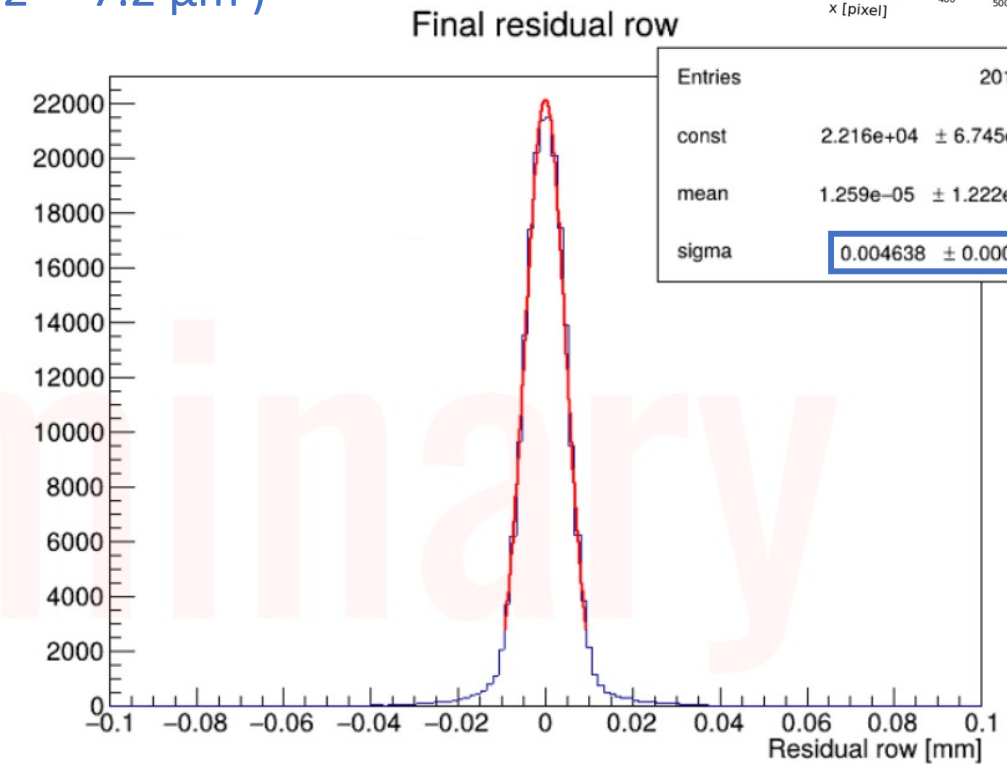
Spatial resolution with tilt = 0° and only 1 cluster per plane



$\sigma \sim 4.7$ µm

(< pitch / √12 ~ 7.2 µm)

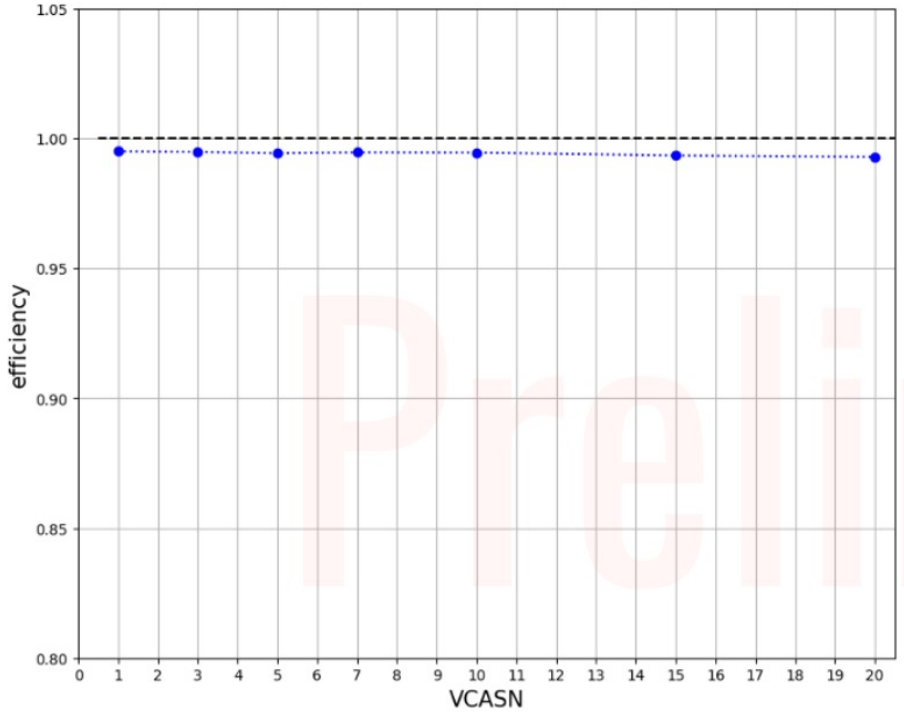


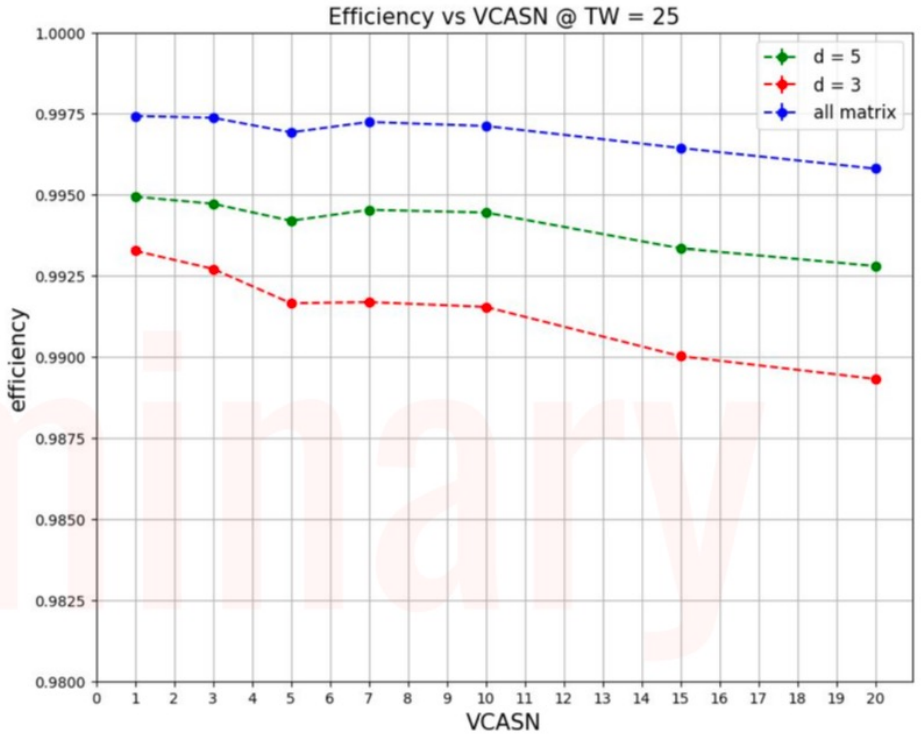


MD3: testbeam w/ 120 GeV protons

Collection efficiency versus discriminator threshold (time window 5 μs) and spatial cut

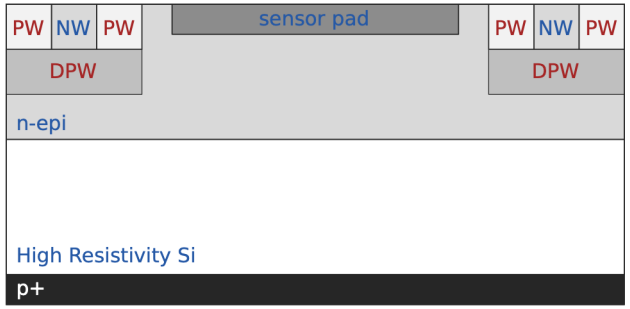
average efficiency 0.9941 ± 0.0003





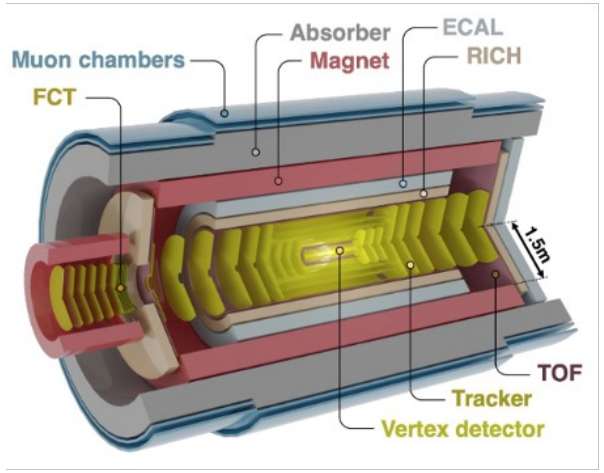
ARCADIA R&D for fast timing (ER3)

fully-depleted (FD) MAPS

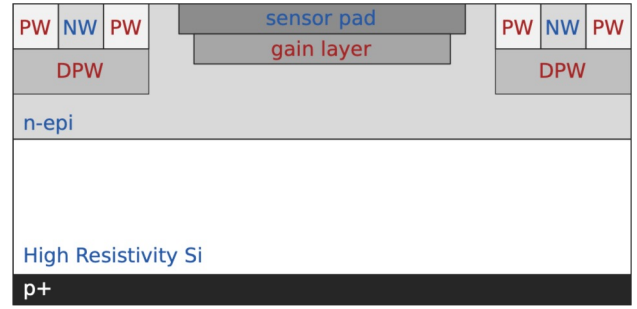


ALICE3 TOF detector:

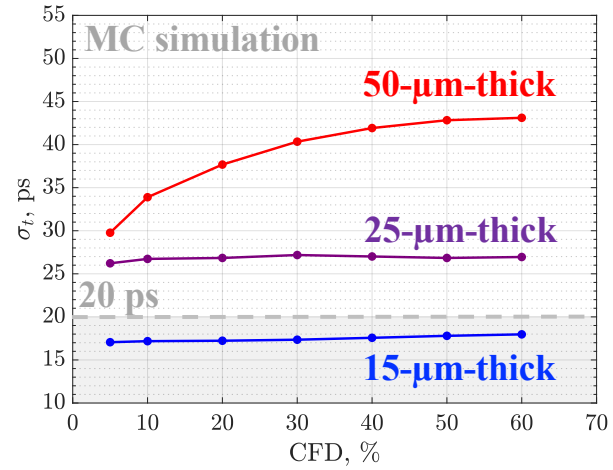
- high-resolution **tracking**
- **particle ID** at low $p_T \Rightarrow \sigma_t \sim$ **20 ps**



CMOS-LGAD

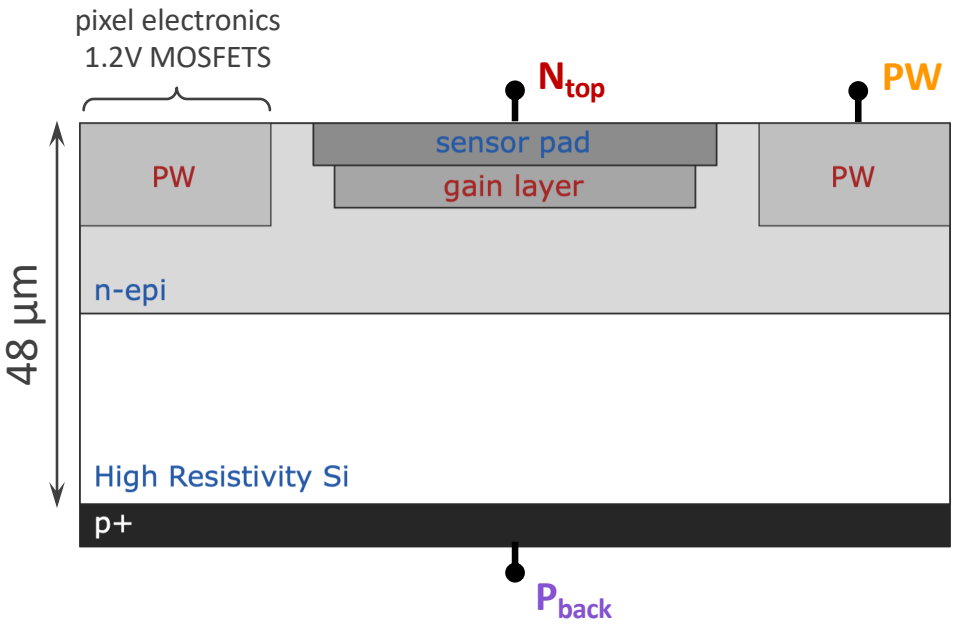


add-on ***p*-gain** implant
(**gain** target: **10 – 30**)

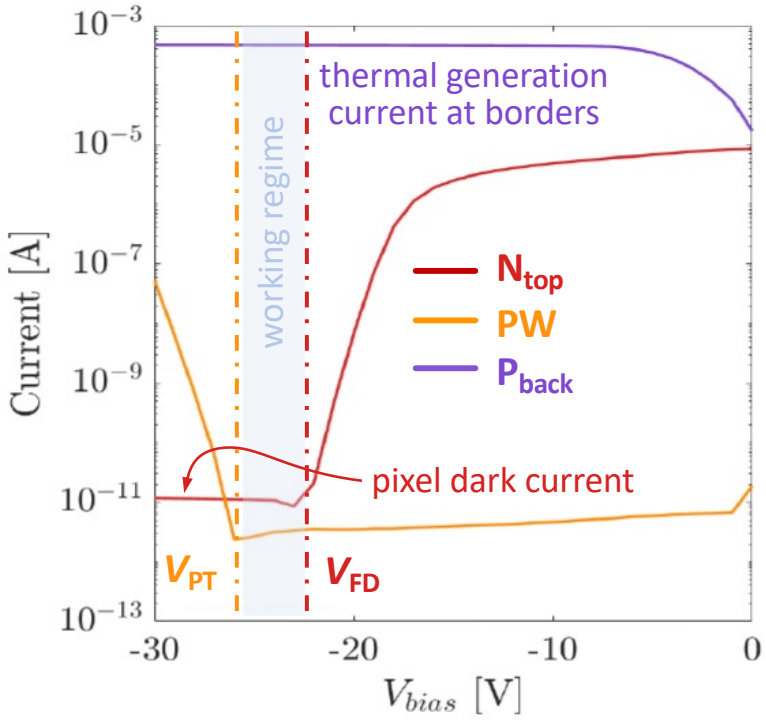


ARCADIA R&D for fast timing (ER3)

Sensor layout



Operation regime

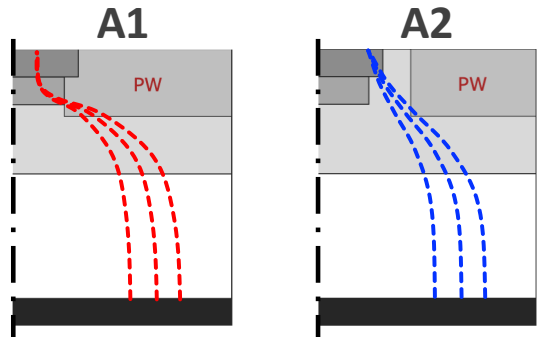


- **full-depletion** condition
- **punch-through** driven by the **backside bias**, which defines the **field** in the substrate
- **edge breakdown** (due to gain) induced by the **topside voltage**

Two border layouts

A1
pros: **uniform multiplication** (high FF)
cons: **delayed signals at periphery**

A2 (std.)
pros: **uniform response**
cons: **increased no-gain zone**



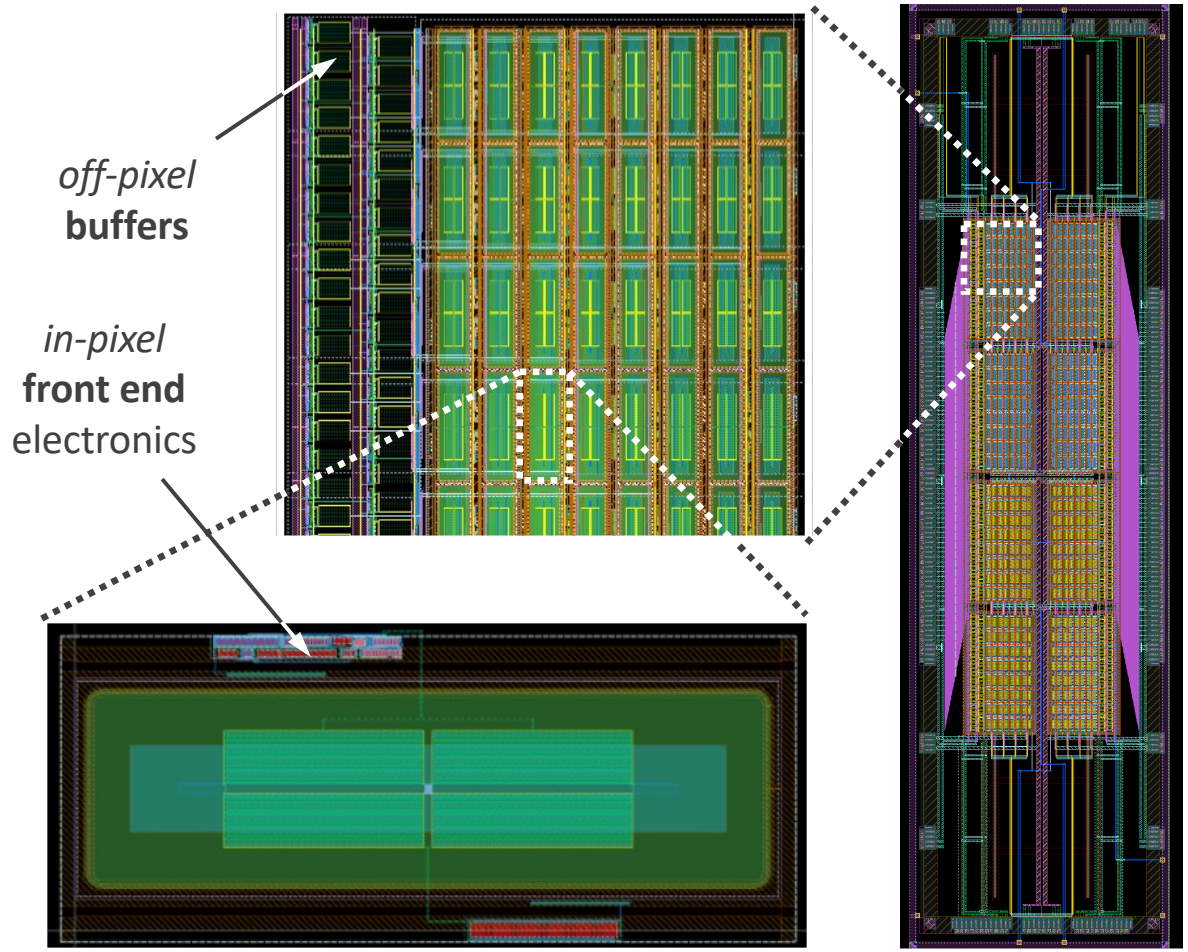
ARCADIA R&D for fast timing (ER3)

MADPIX: **M**onolithic CMOS **A**valanche **D**etector **PIX**elated Prototype for ps Timing Applications

- **8 matrices** (**64 pixel pads** each) implementing different sensor and front-end flavors
- **250** × **100 µm²** pads
- readout: **64 analog outputs** on each side, **rolling shutter** of single matrix readout

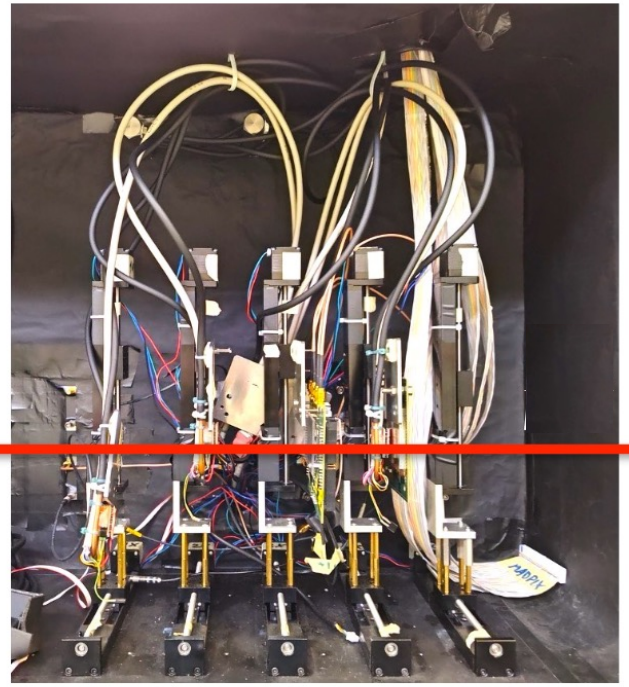
Front-end (*in-pixel*)
- **Cascoded common source** amplifier, followed by a **differential buffer** (1.2V)
- **AC-coupled** with **sensor** (to decouple it from V_{top})
- **Power** consumption: **0.18 mW/ch**

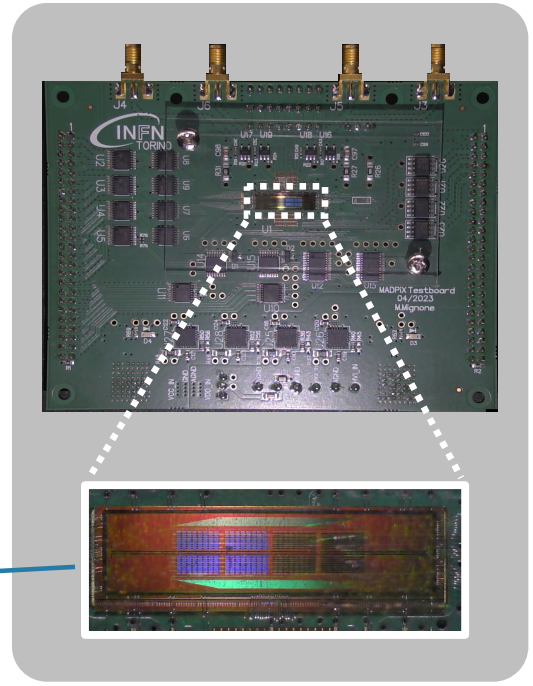
Source follower *off-pixel* **buffers** (3.3V)
- **AC-coupled** with **FE**
- **Power** consumption: **1.65 mW/ch**



MADPIX: testbeam w/ 10 GeV pions

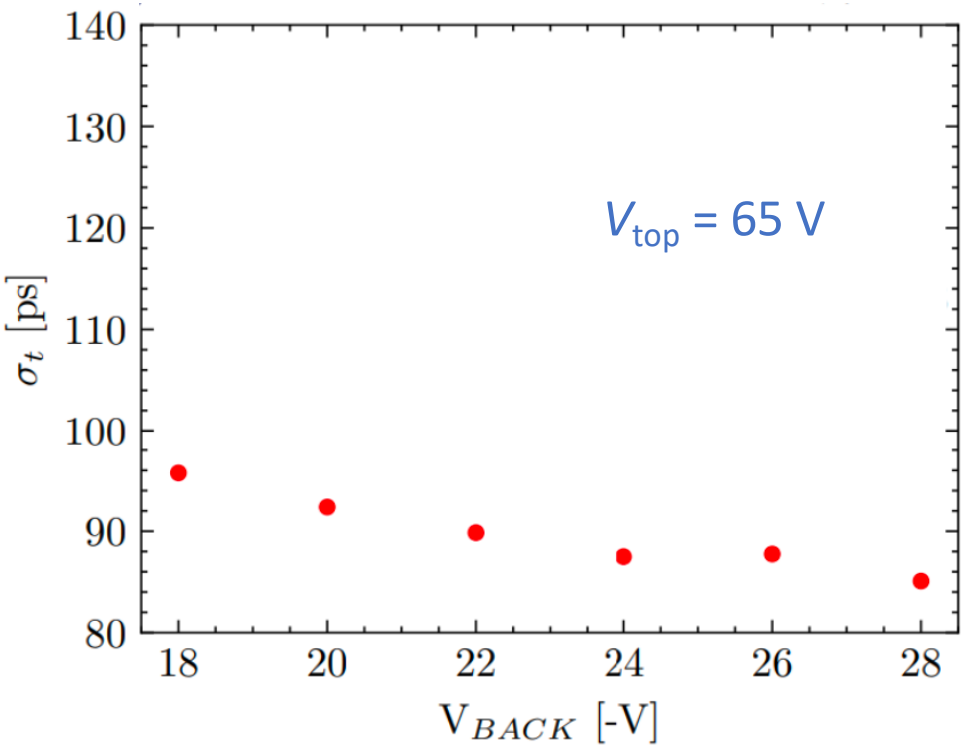
ALICE3 TOF testbeam @ CERN PS in October 2024

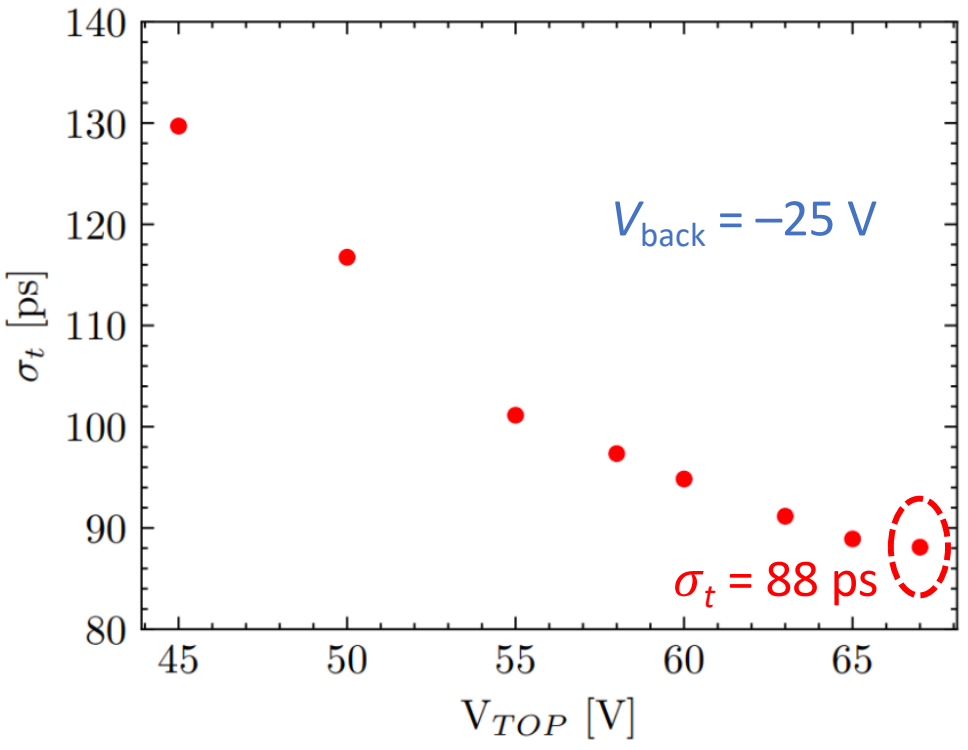




The ALICE3 TOF testbeam team:
M. Bregant, S. Bufalino, Z. Buthelezi, D. Cavazza, M. Colocci, C. Ferrero, U. Follo, J. Goodhead, S. Förtsch, G. Gioachin, M. Mandurrino, B. Sabiu, G. Souza, S. Strazzi, S. Wimberg

MADPIX: testbeam w/ 10 GeV pions





Time resolution (sensor + FE electronics) at V_{top} = 65 V and V_{back} = –25 V is σ_t = 88 ps

With boosted electronics: σ_t = 75 ps

Still not optimized substrate and geometry ⇒ improvements are expected

R&D for a Si-Wrapper with AC-LGADs

Detector requirements:

1. **high momentum resolution** through TOF measurement and extended tracking coverage
2. **large area** (~100 m^2)
3. **high efficiency** with high coverage of the acceptance area

The **IDEA** detector concept @ FCC

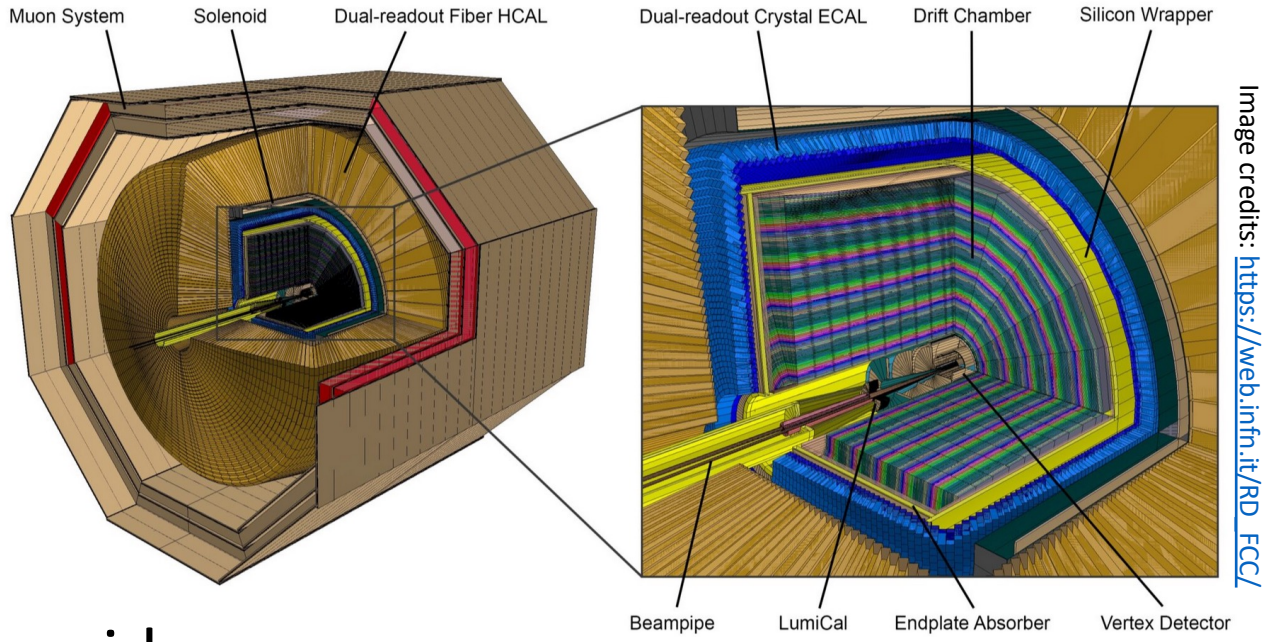


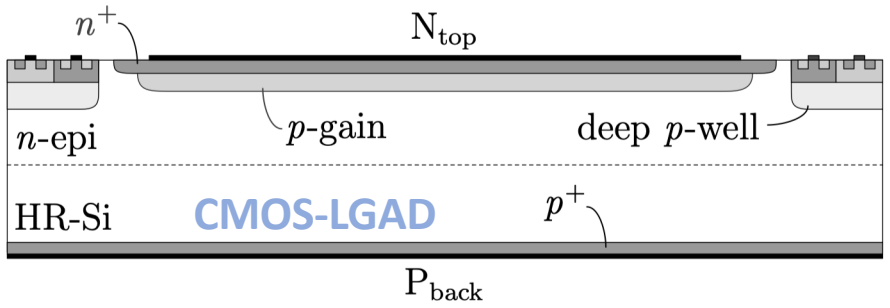
Image credits: https://web.infn.it/RD_FCC/

A good candidate technology should provide:

1. **4D tracking capabilities**
2. **monolithic integration** ⇒ **Monolithic CMOS AC-LGAD**
3. **high fill-factor**

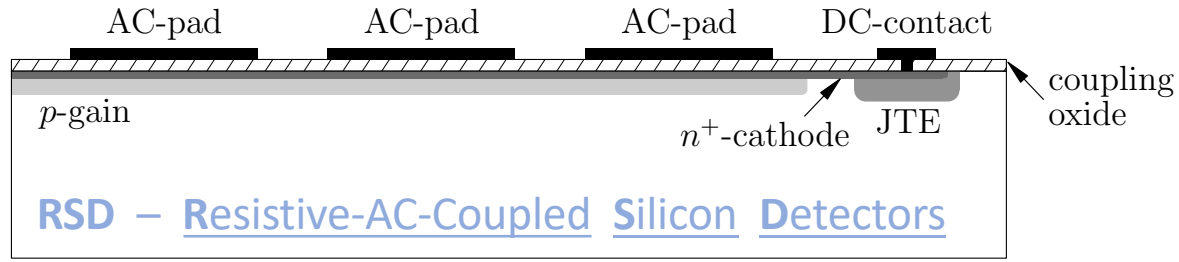
R&D for a Si-Wrapper with AC-LGADs

CMOS integration of the **LGAD technology** already demonstrated (in LF11is)



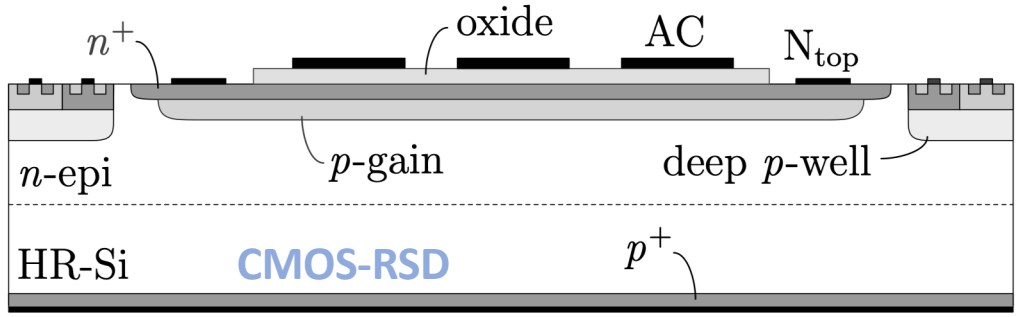
Spatial resolution **~3% of sensor pitch** (allowing to relax the channel density)

Time resolution similar to standard LGADs: **30-40 ps**



Plausible concurrent targets:

- **σ_t = 10-20 ps**
- **µm-level σ_x**
- **100% FF**



pending patent and extent of protection

Detector layout and process flow design activities are ongoing

First prototypes in next silicon production runs (std. CMOS process)

R&D for a Si-Wrapper with AC-LGADs

CMOS integration
already demo

Spatial resolution ~3% of sensor pitch
nel density)
o standard
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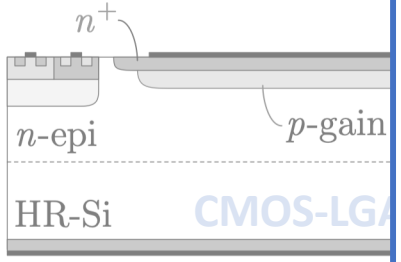
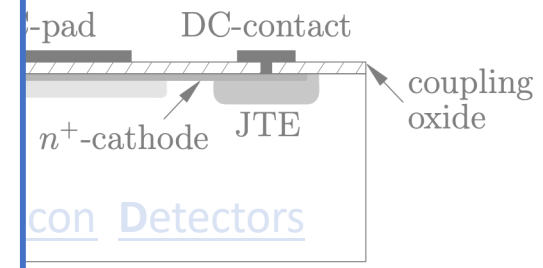
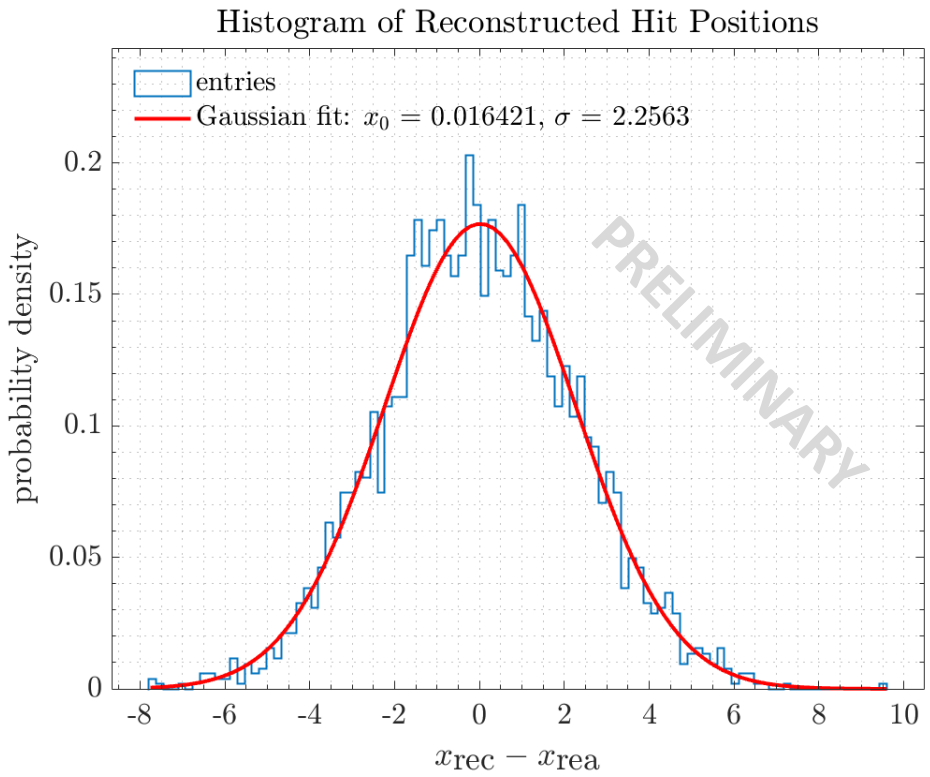




con Detectors

Simulation of a 80-µm-pitch sensor



Spatial resolution: 2.25 µm (~2.8% of the pitch)

Plausible concurrent targe

- σ_t = 10-20 ps
- µm-level σ_x
- 100% FF

extent of protection

Detector layout and process flow design activities are ongoing

First prototypes in next silicon production runs (std. CMOS process)

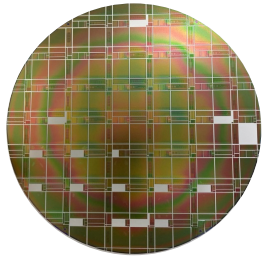
ARCADIA FD-MAPS: Status & Perspectives

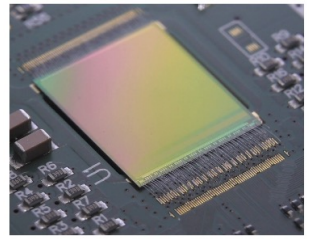
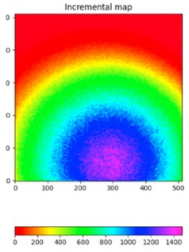
FD-MAPS development with LFoundry 11is

- INFN platform for R&D in fully-depleted monolithic CMOS sensor technology, IP and ASIC design, DAQ systems
- Low-power sensor architectures (10 mW/cm^2) for charged particle detectors
- Innovative monolithic CMOS sensors with gain layer (CMOS LGAD)
- MAPS technology for tracking and timing systems in future lepton colliders (Vertex and Si-wrapper for **IDEA**)
- Time-of-flight detector for ALICE3 (ARCADIA CMOS-LGAD is the baseline option for the **ALICE3 TOF**)

Ongoing and financed programs and projects

- Funding available towards system-grade chips for FCC and sensor tapeout for ALICE3 TOF
- ARCADIA LF11is FD-MAPS technology support through DRD7.6a
- Funding requests for CMOS-RSD development



Thank you for the attention!