CMOS SPADs at Heidelberg University

XLZD Collaboration Meeting at LNGS – 02.06.2025

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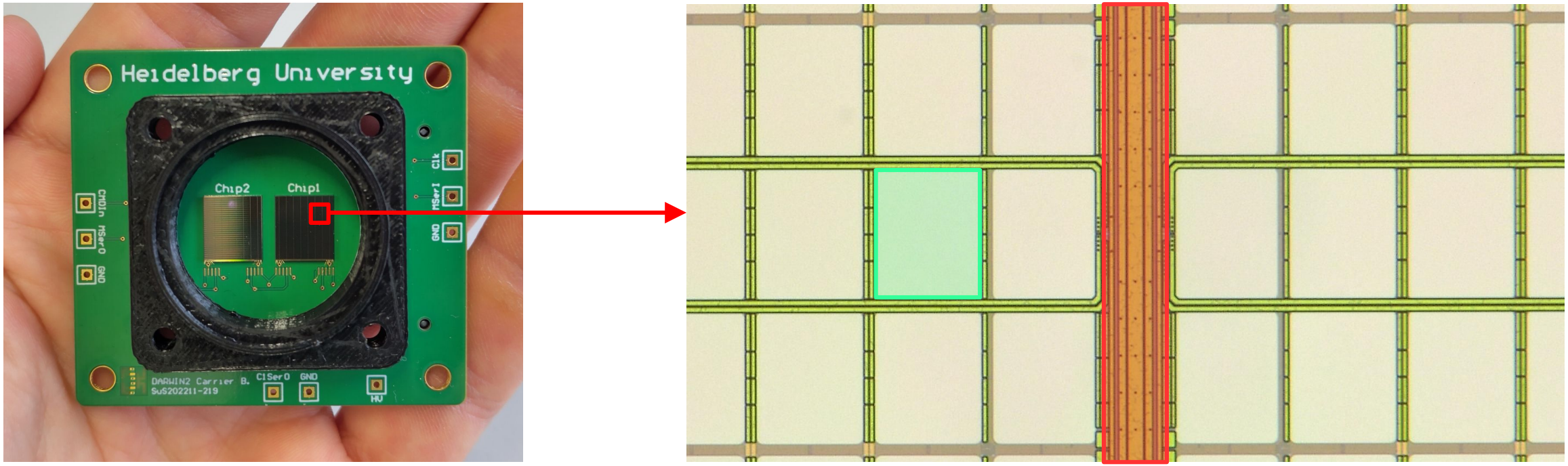
CMOS SPADs



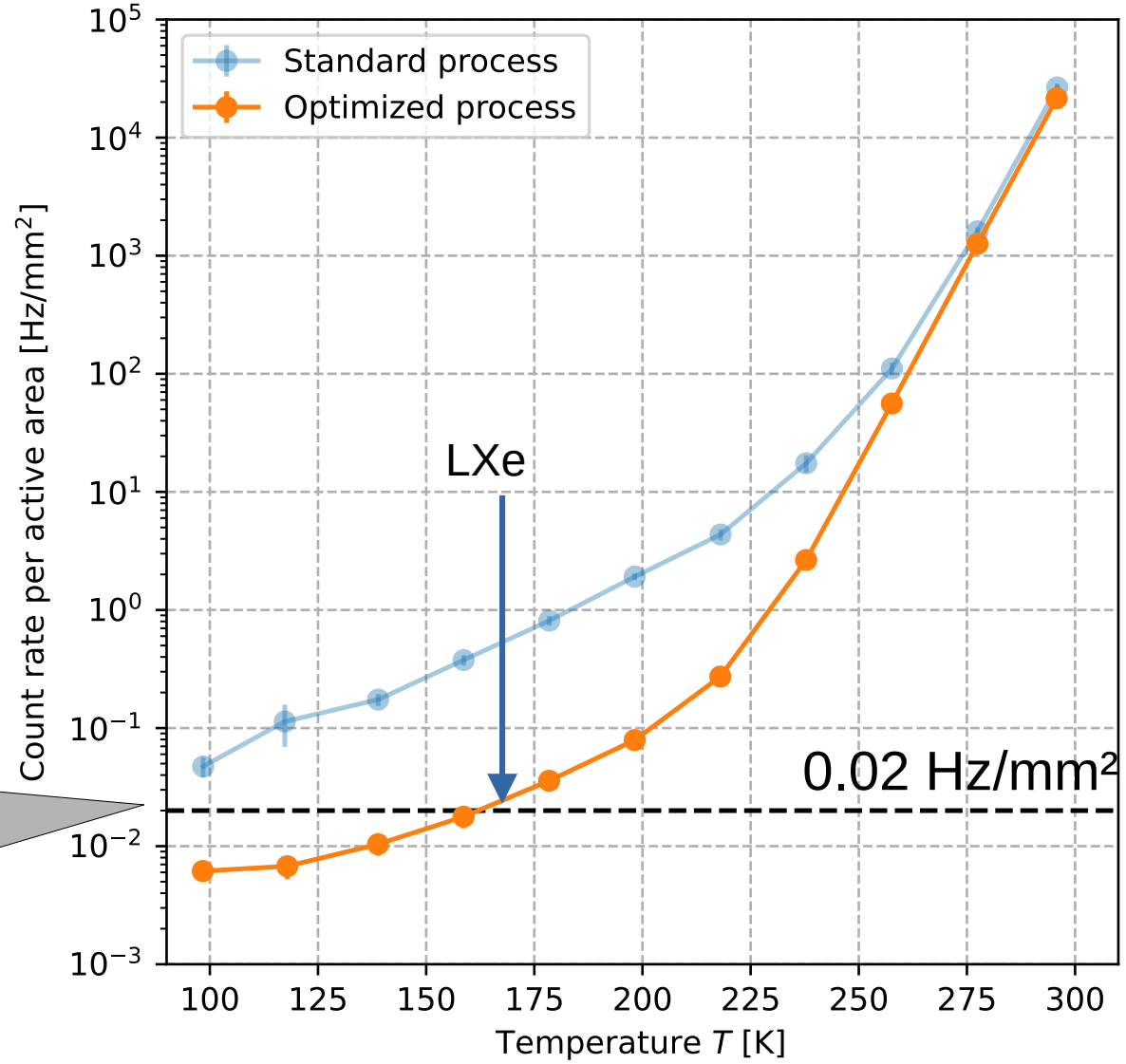
Single Photon avalanche diodes (SPAD) and CMOS electronics are fabricated on the same chip

- Readout electronics are tailored to the needs of an experiment/application eg. for high/low data rates, power constrains (no ADCs needed), mechanics, long term stability (tbc) ...
- Fill factor might be reduced due to electronics and each experiment needs its own chip…

The goal of this talk is to show the present status of Digital SiPM and to convince you that this approach in general is a promising alternative to PMTs and SiPMs that deserves further investigations and R&D

SPAD Quality

Dark Count Rate

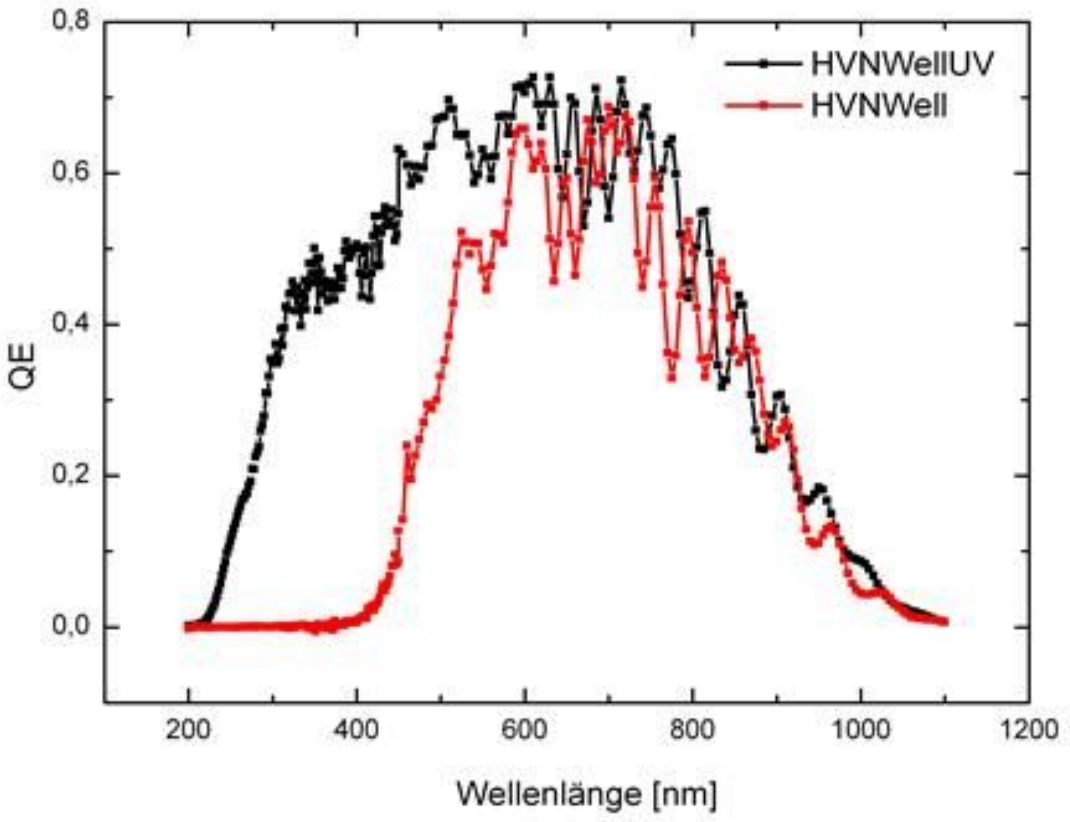


RT: ~25 kHz/mm²

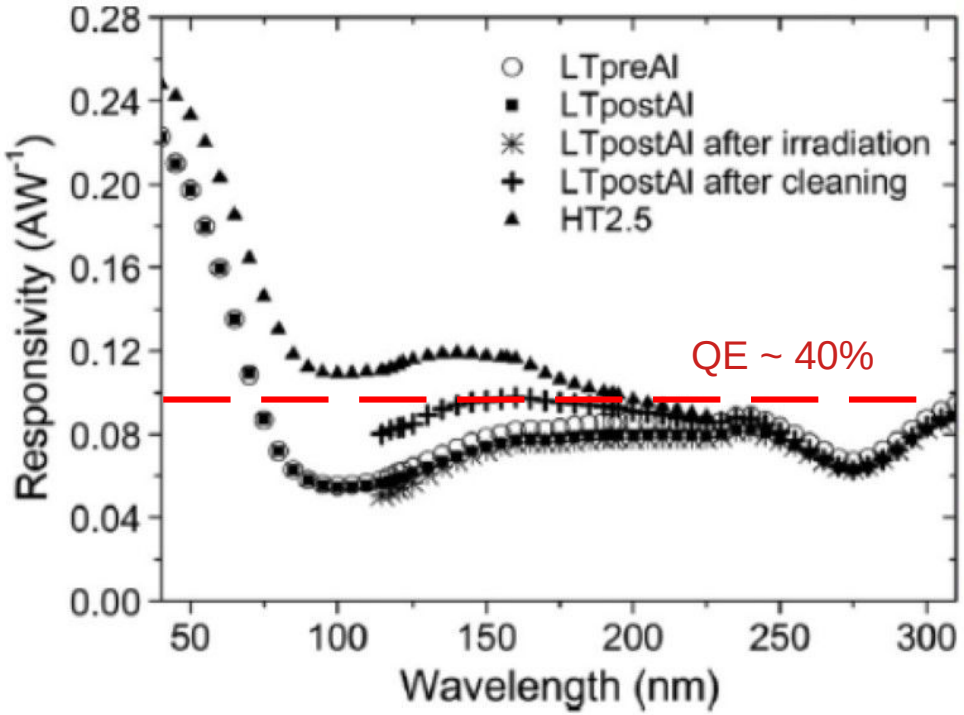
Our Manufacturer IMS improved the DCR at low T more than an order of magnitude!

Quantum Efficiency

- IMS has two established processes which offer excellent QE for visible (A) and UV light (B, UV transparent passivation)
- SPADs can be operated with wavelength shifters in LXe



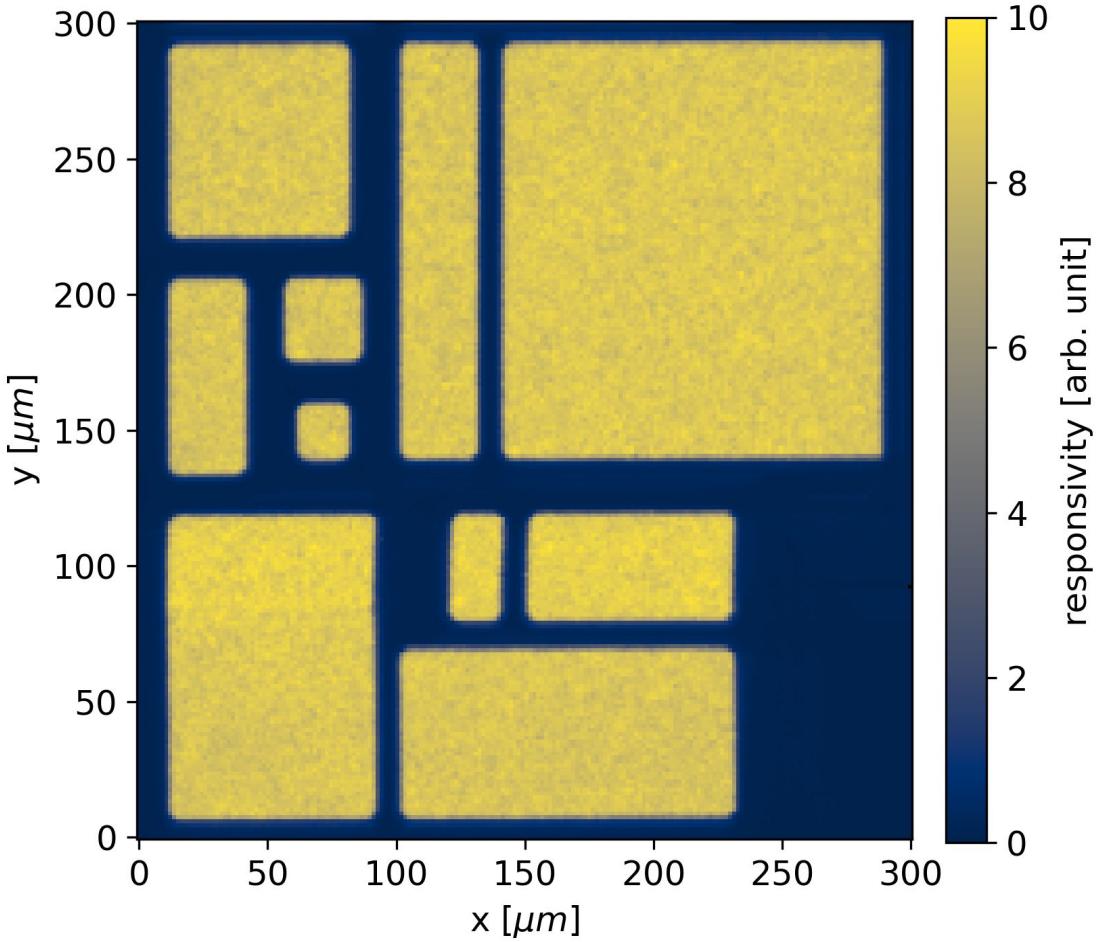
- IMS claims they can achieve the VUV sensitivity (below), the technology ('PureB Process') has been used for other devices
- They could do this if we express sufficient interest (and provide funding)

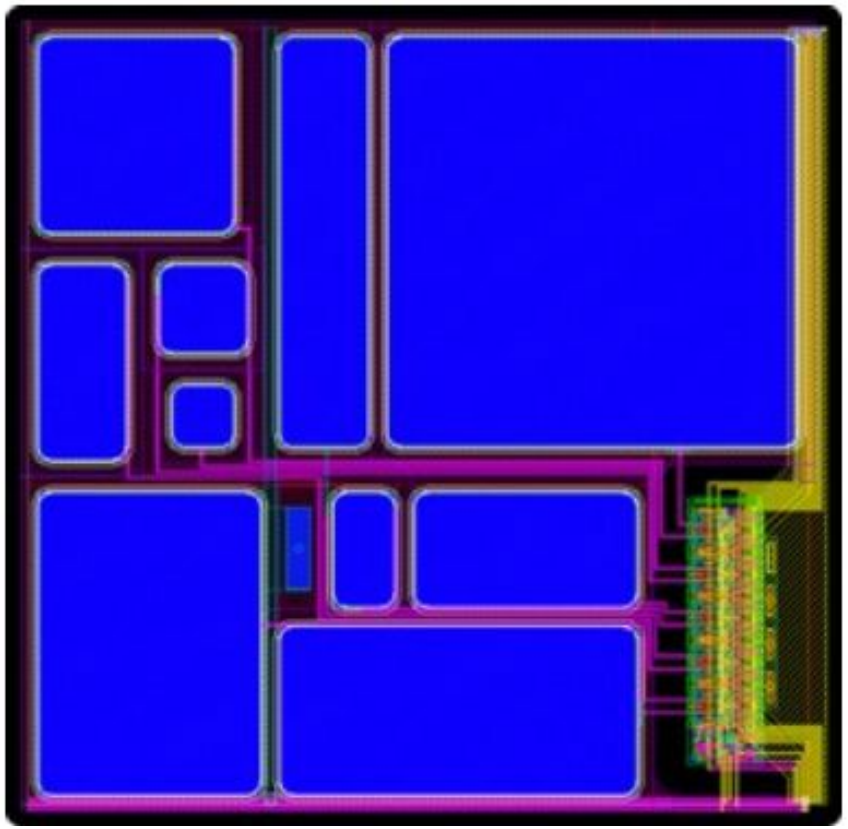


Nanver, Lis K. IEEE Journal of Selected Topics in Quantum Electronics, 20(6):306-316, 2014
QE Estimate: IMS private communication

Spatial homogeneity of sensitivity

- SPAD light response of prototype chip scanned with a small laser spot (Ø ~ 1µm)
- SPADs of various geometries and sizes show equal and very homogenous response
- Width and length of the active area matches design value well

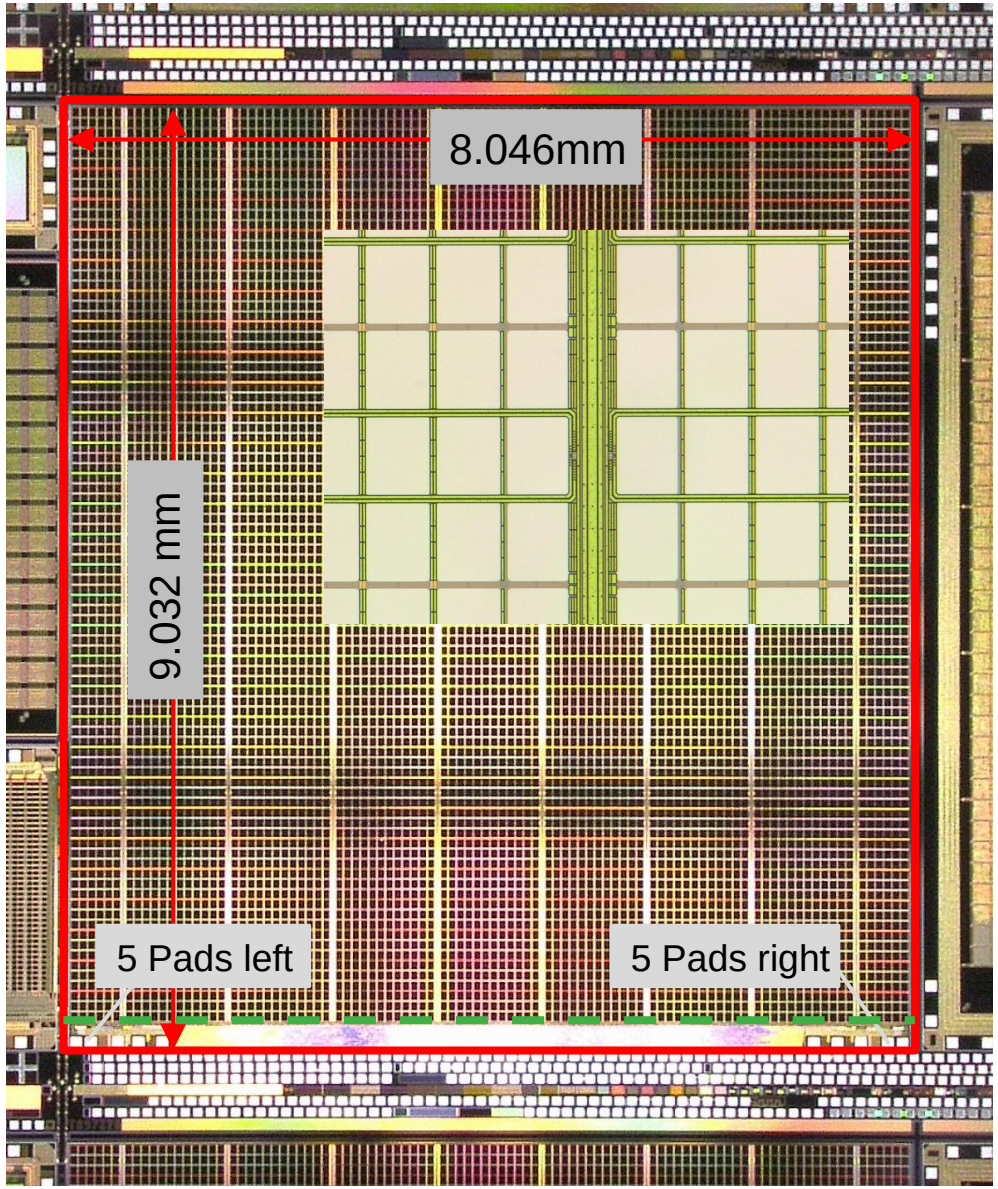




High fill factor CMOS SPAD array for rare event search experiments

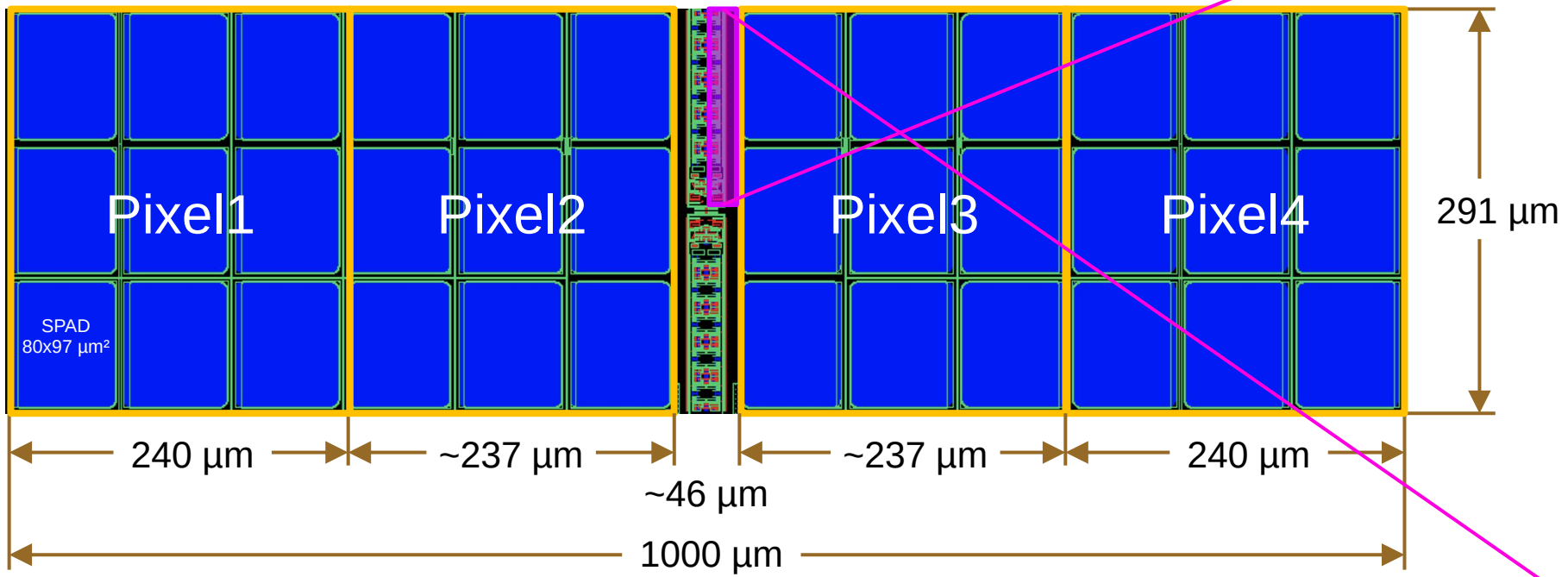
‘DARWIN’ Array

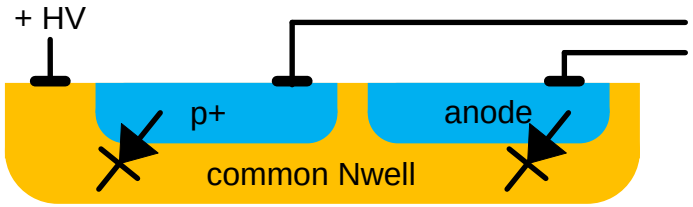
- Development triggered by DARWIN experiment
- Chip size: ~8 × 9 mm²
  32 × 30 pixels of 240 × 290µm²
  - One pixel contains 9 SPADs which can be masked individually (if noisy)
- SPAD Fill factor ~72%
  (including periphery, before pixel masking)
- Small digital readout (bottom) with serial data output.
  Chips can be daisy chained
- Readout outputs Chip ID (6Bit) **pixel-x-y-postion** (10Bit) and timestamp (10Bit) for **each photon hit** in the matrix
- Only 7 Signals:
  - 4 logic: Clk / Command / SerIn, SerOut
  - 3 supplies: GND, VDD, HV (pads duplicated)

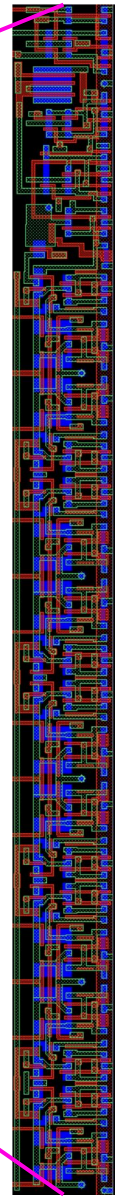


Pixel geometry

- 9 SPADs are grouped to one '*pixel*' to save CMOS circuitry
- A Hit signal is the logical OR of the 9 SPADs and is stored in a hit flip flop until readout → no hit loss.
- Individual SPADs can be switched off by changing anode voltage



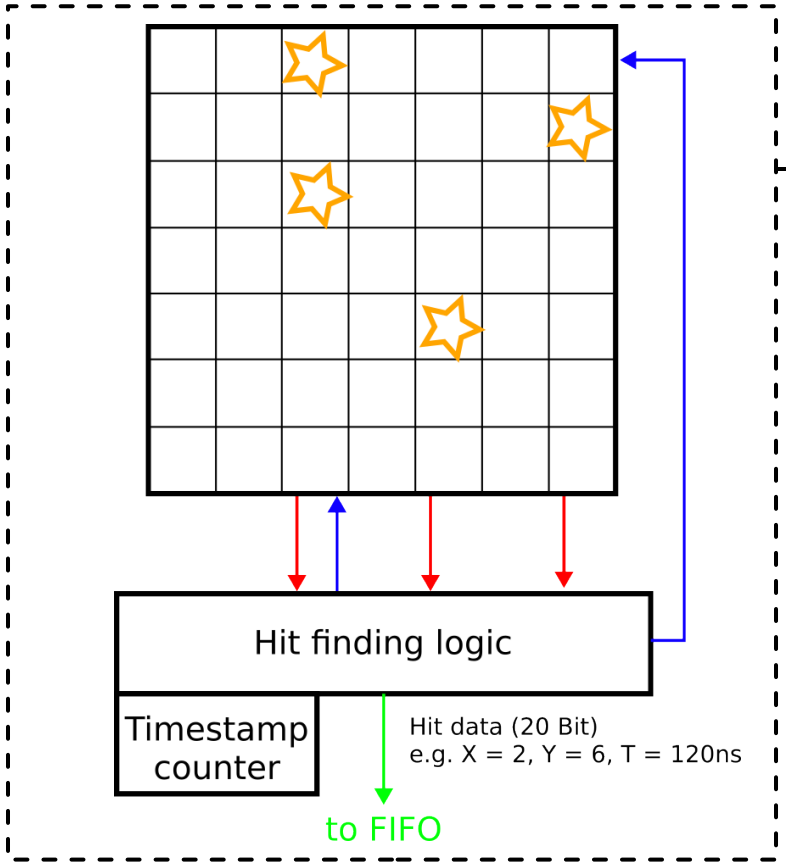


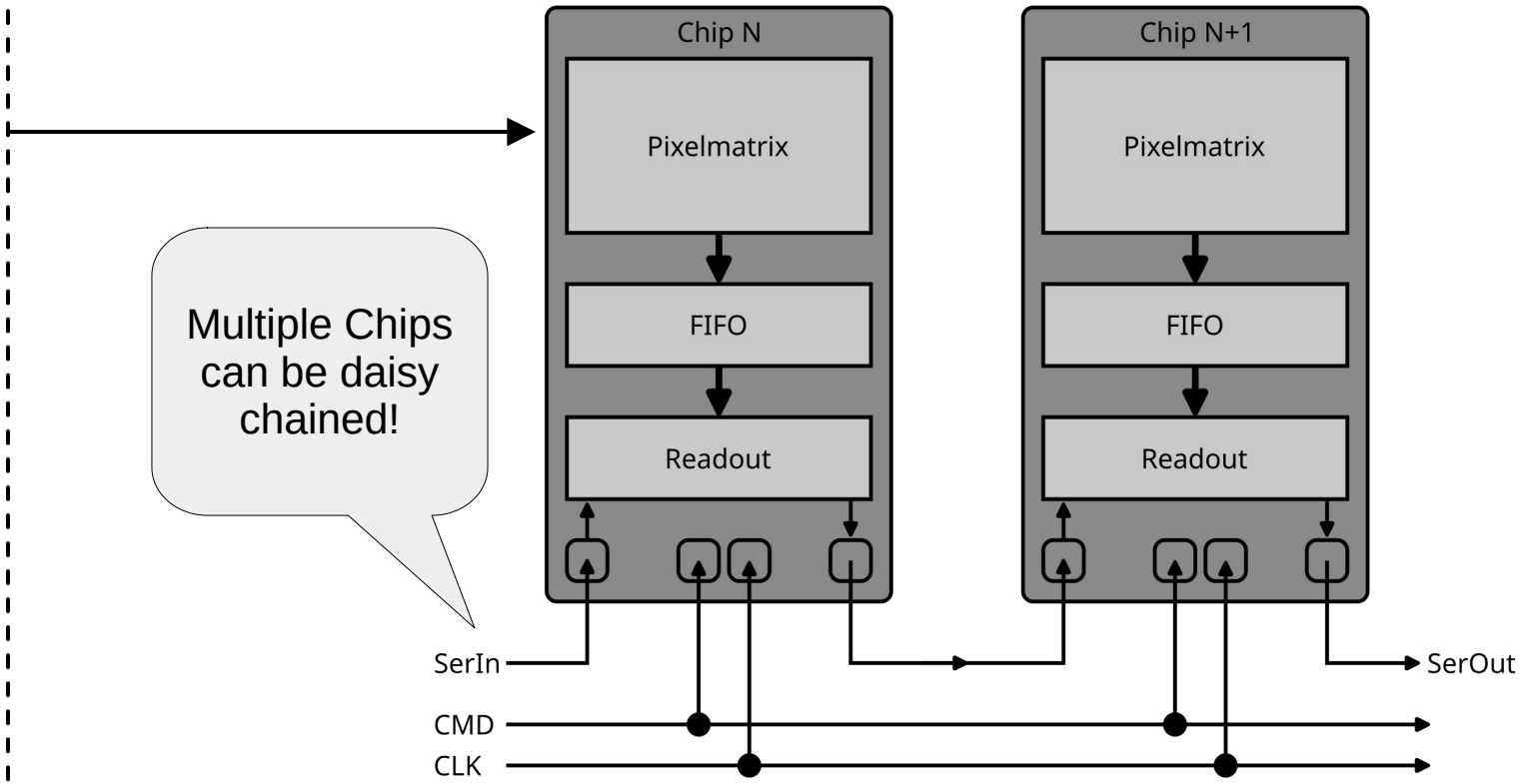


CMOS logic for 1 pixel

- 4 pixels form one unit, with common circuit in the center
- SPADs share one NWELL -> minimize distance

‘On demand’ digital Readout



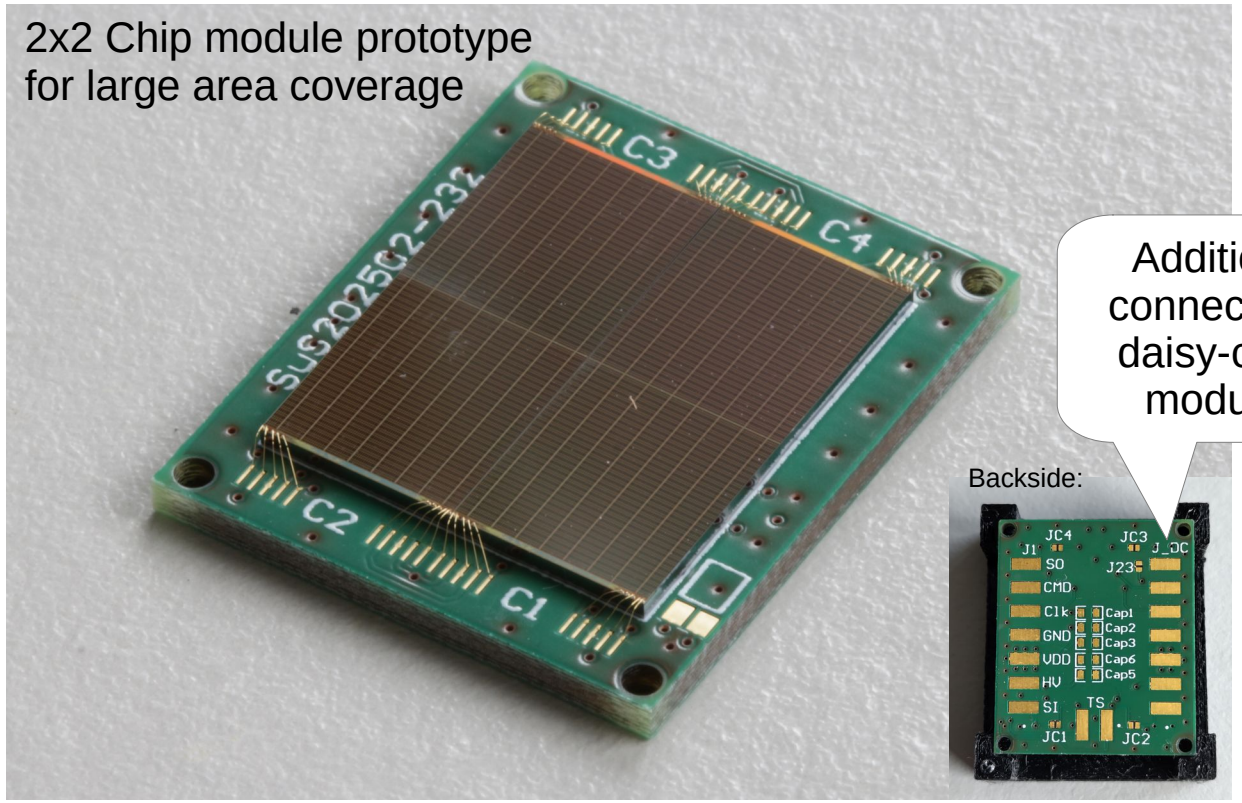


- Data driven approach to reduce power and data rate
- Pixel hit triggers Matrix Readout and time stamp latch (Δt ~10/20ns)
- Pixel x-y-address and time stamp is recorded into a FIFO

- Data in the FIFO is emptied over one serial line (slow ~ 520ns/Hit @ 50MHz)
- Data propagates through a daisy chain of chips
- Simple protocol (CMD + SerIn) for control of the chain

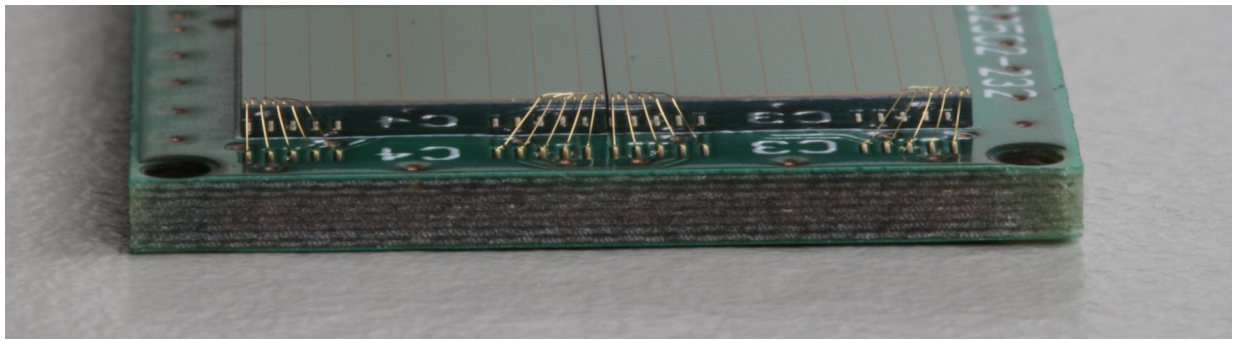
Module Prototype

2x2 Chip module prototype
for large area coverage

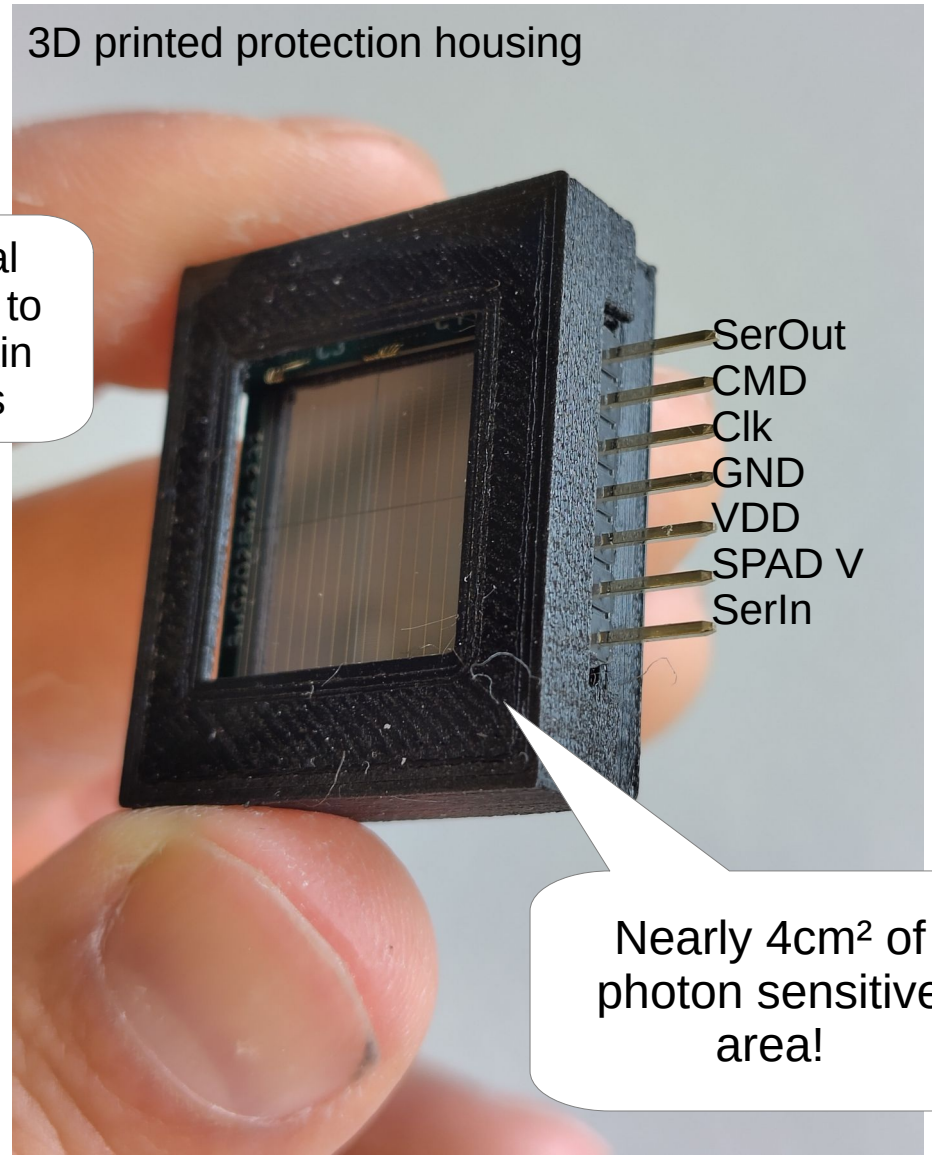


Backside:

Additional connector to daisy-chain modules



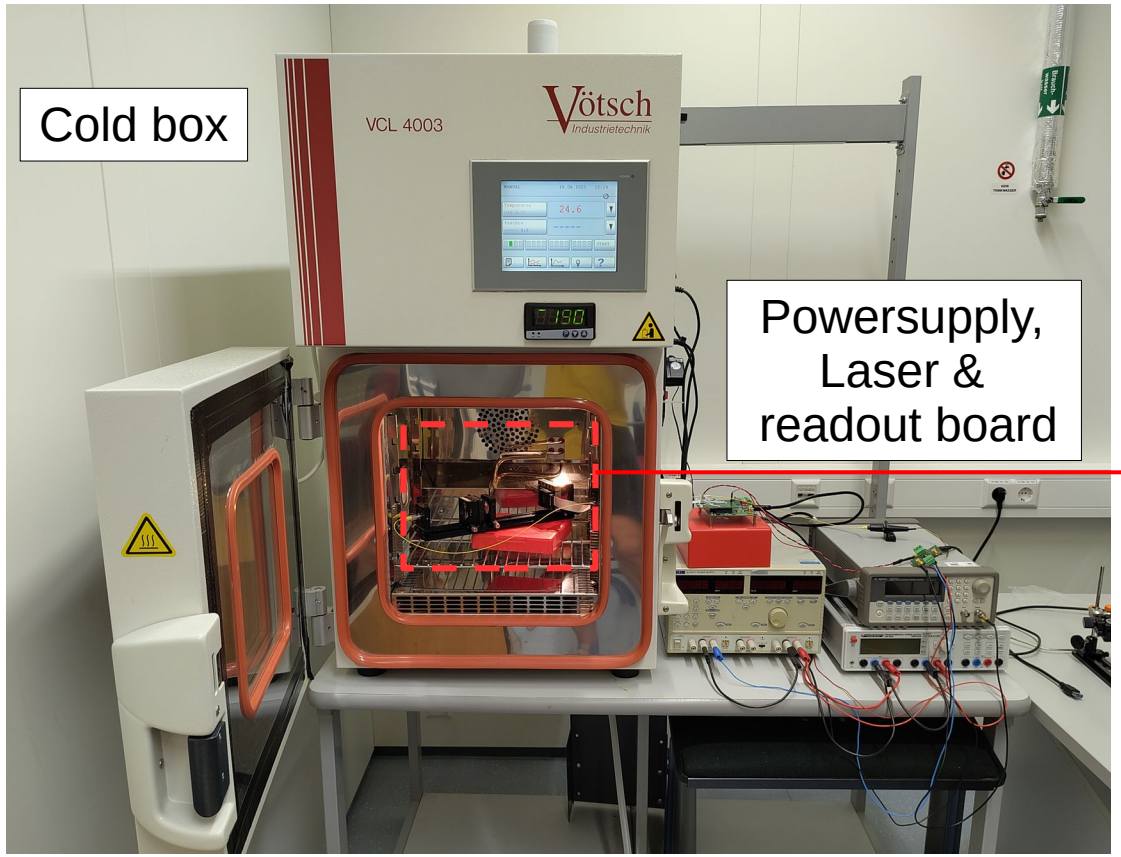
3D printed protection housing

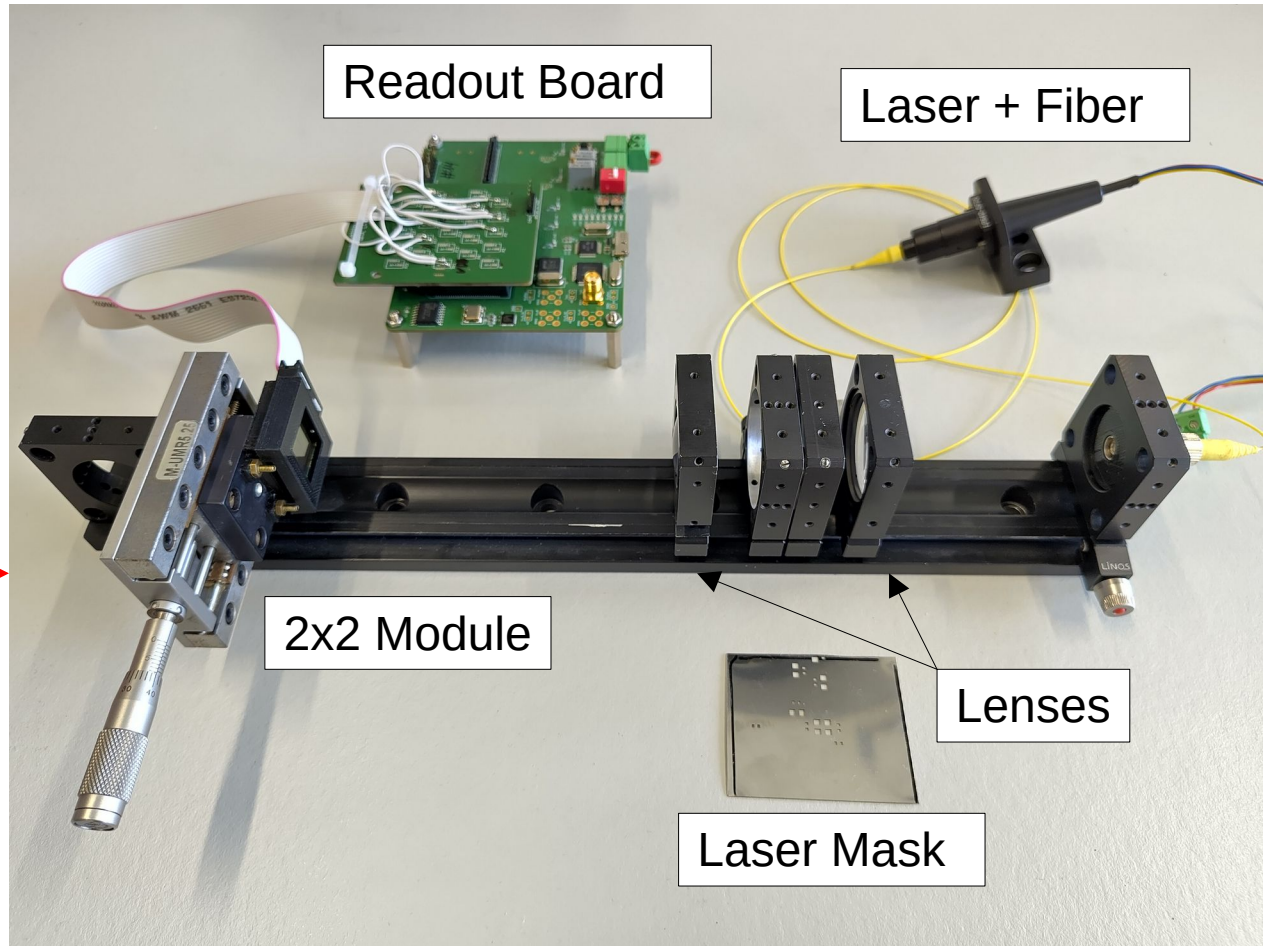


Nearly 4cm² of photon sensitive area!

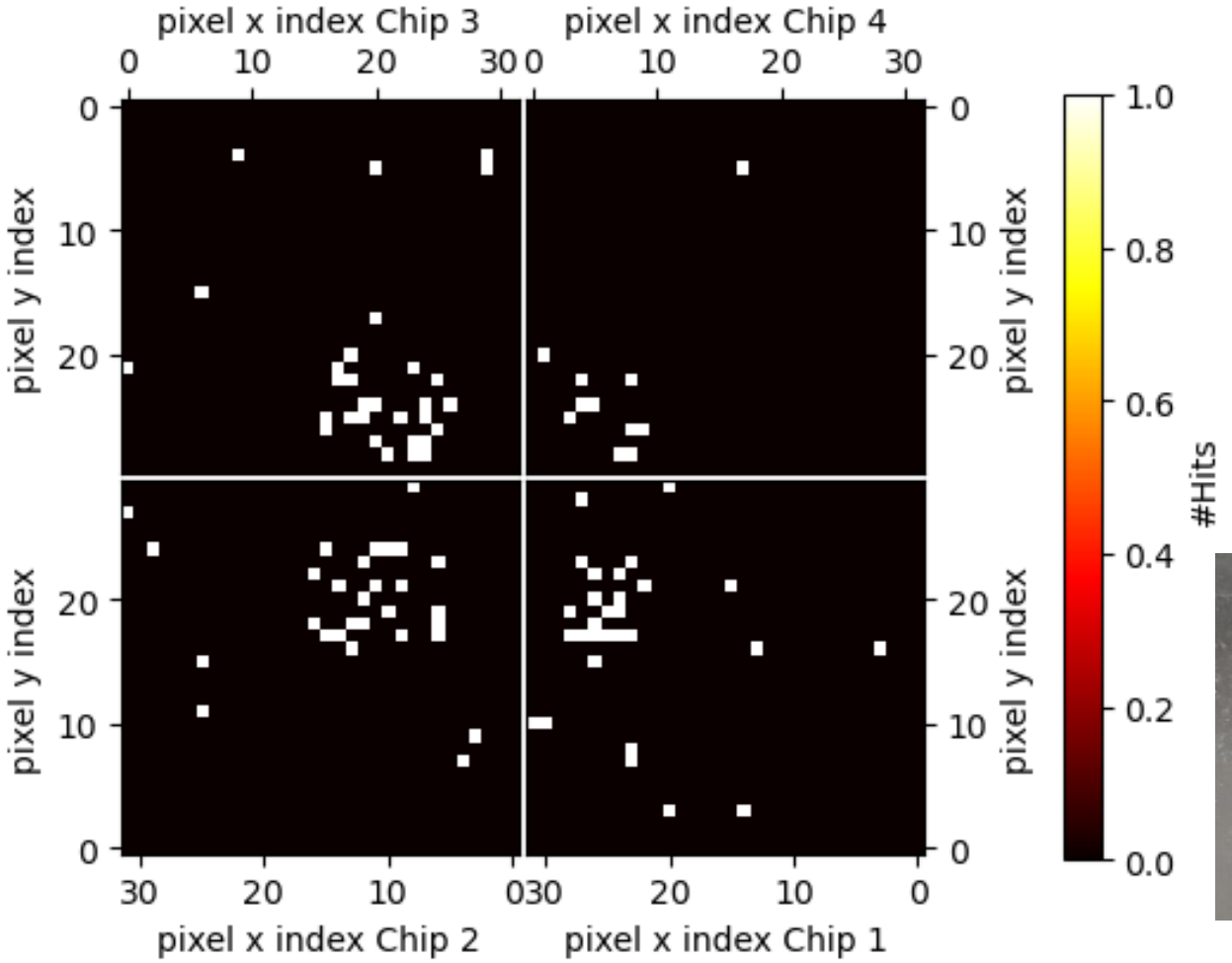
Module in Coldbox

- Module is read out by custom USB 3.0 board
- Preliminary we use a self made breakout adapter and a flat band cable to connect module and board
- Module is operated at T = -15°C to reduce dark count rate
- Simple optical setup to project a steel mask on the the sensitive area (~4cm²)



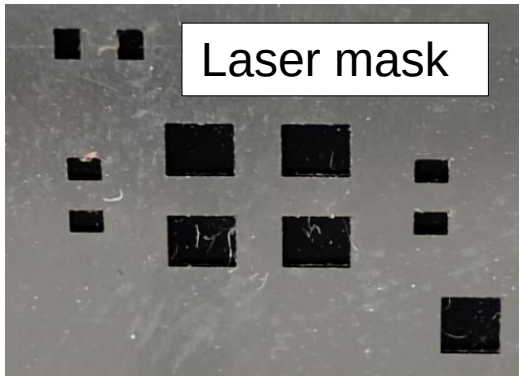


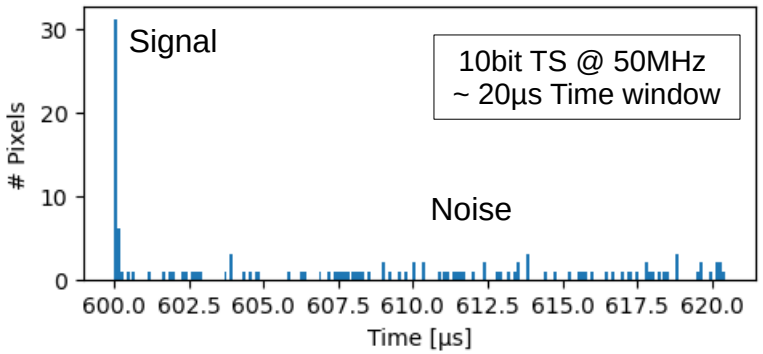
Laser imaging (single pulse)



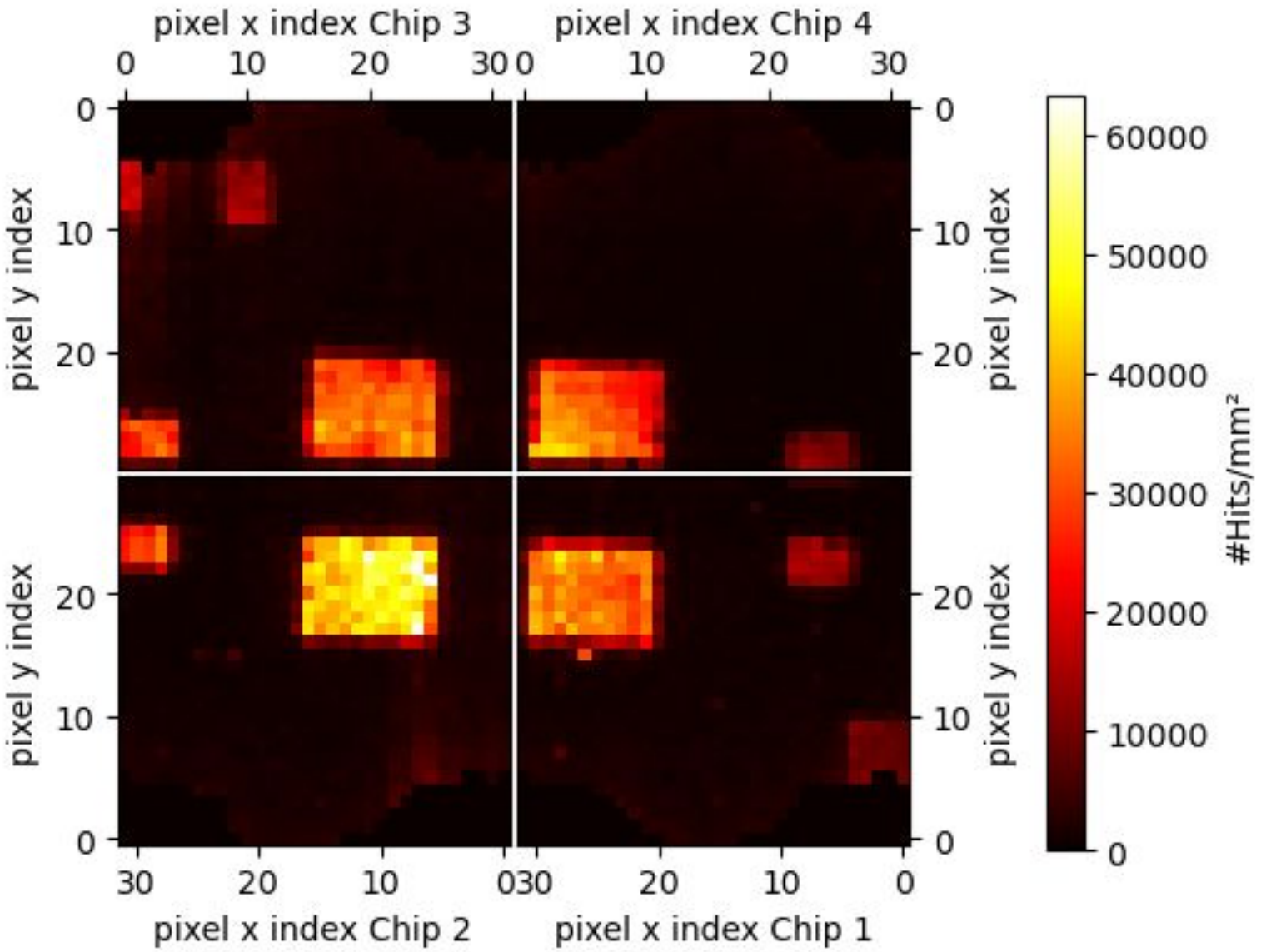
- Image of one laser pulse of 100ns on the module
- Noise discarded with time stamp (T > 100ns)
- Noisy SPADs are turned off
- Reminder: X-Y-T information of each photon hit in a pixel + Chip ID is provided by the module (26Bit per Hit)

  → very granular position reconstruction and good time resolution

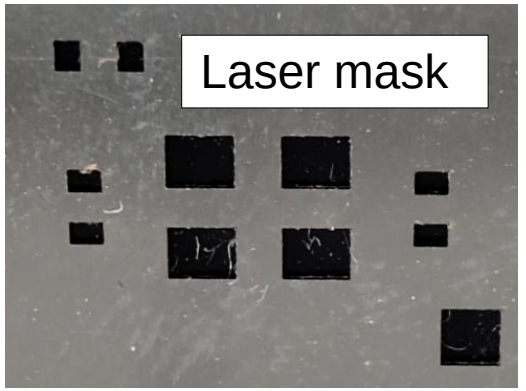




Accumulated Laser image



- Image accumulated from 7500 laser pulses of 100ns (Accumulation is done offline on the computer!)
- Number of hits per pixels normalized to active area to account for turned off noisy SPADs.



Module data rates

- At 50 MHz clock speed, ONE serial readout CHAIN can read 1.8 Mhits/s
  → at higher photon/dark count rates hits are trapped in matrix

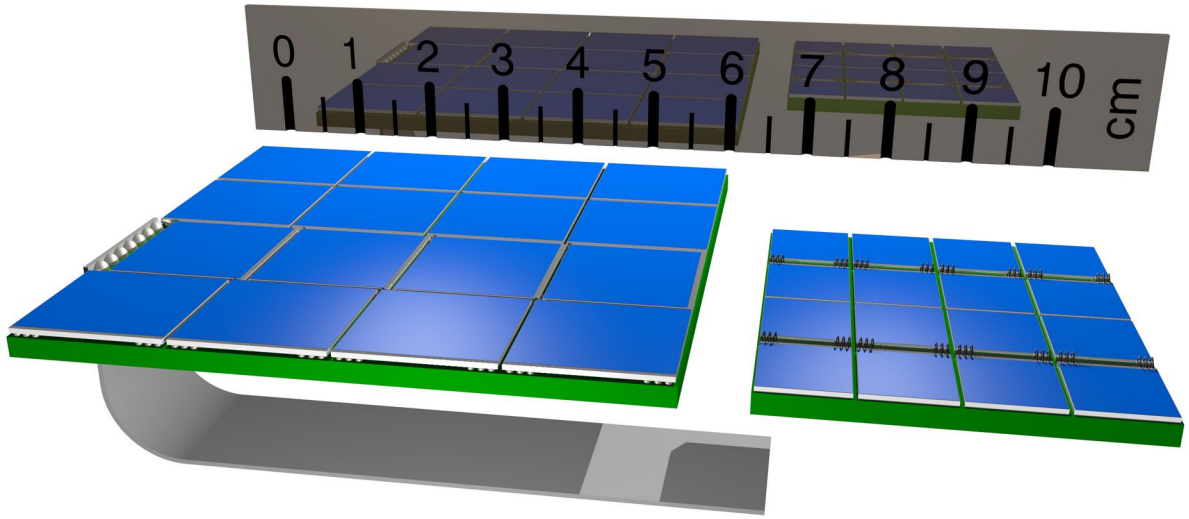
- For comparison: At a DCR of 0.1 Hz/mm² at LXe Temperatures a 1m² plane (=10000 Chips) produces only 100kHit/s. S1 photon rate is probably small.
  → We ‚COULD' read 1m² with only one (serial output) cable

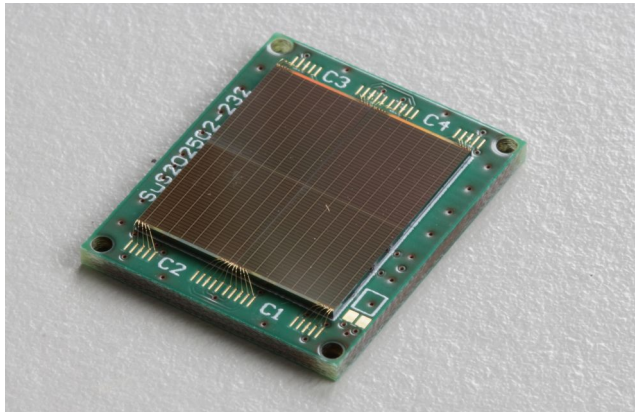
- S2 signal: If a larger number of photons hits a 'small' area (this depends on electrode geometry!):
  - NO SPAD hit gets lost
  - BUT: Readout can take long. For ex. 1000 hits require 600µs
  - Impact of this requires simulation!

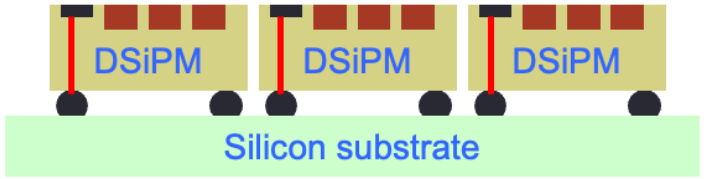
XLZD Modules

- First PCB module with 2x2 chips operational

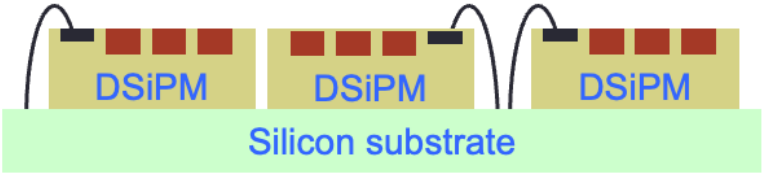
- Will next build a Silicon module to enhance radio purity and have a matching CTE for good low T mechanic stability
  - First version with wire bonds
  - Second version with Chips with Through Silicon Vias (TSV) for very compact module
- Final Chip can be as large as 2x2cm² and modules can be 10x10cm²







Version 2: Chip backside contacts (after postprocessing of wafers)

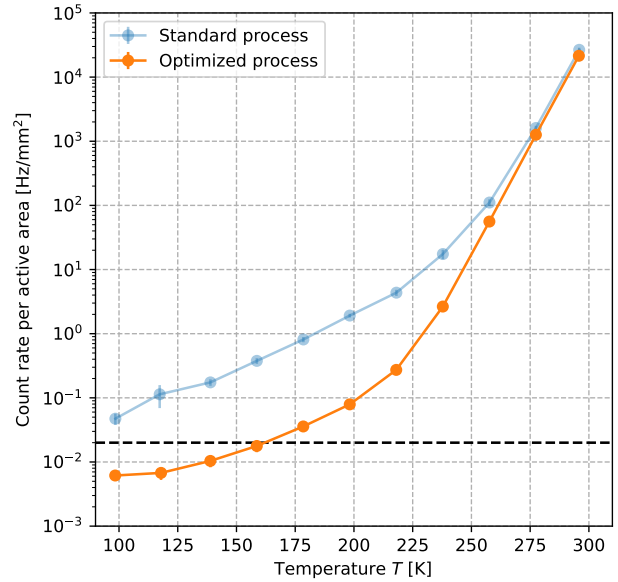


Version 1 : Wire bonds

Digital SiPMs for XLZD?

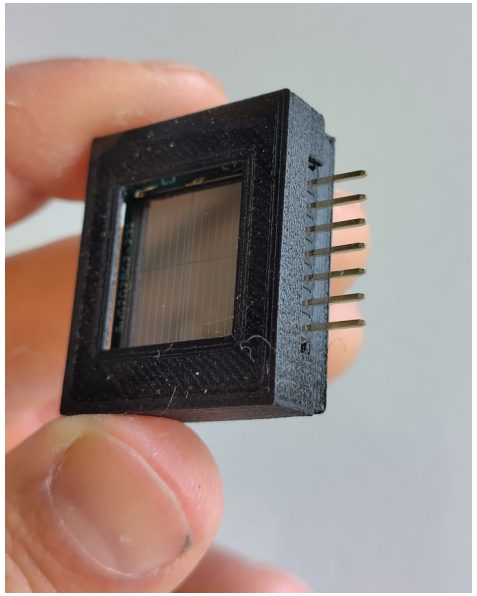
Digital SiPM prototype/demonstrator show

- Excellent dark count rate of 0.02 Hz/mm² at LXe temperature
- High fill factor of up to 72%



Advantages of Digital SiPMs:

- Very simple system (detection and readout on one piece of silicon)
- No amplifier chips needed (and Flash ADCs in warm)
- Serial Daisy chain readout allows modules with few cables (simpler mechanics, less feed-thoughs)
- High spatial resolution, Good time resolution
- Low Power dissipation (numbers needs to be investigated)
- Very Low intrinsic radioactivity ('all silicon')



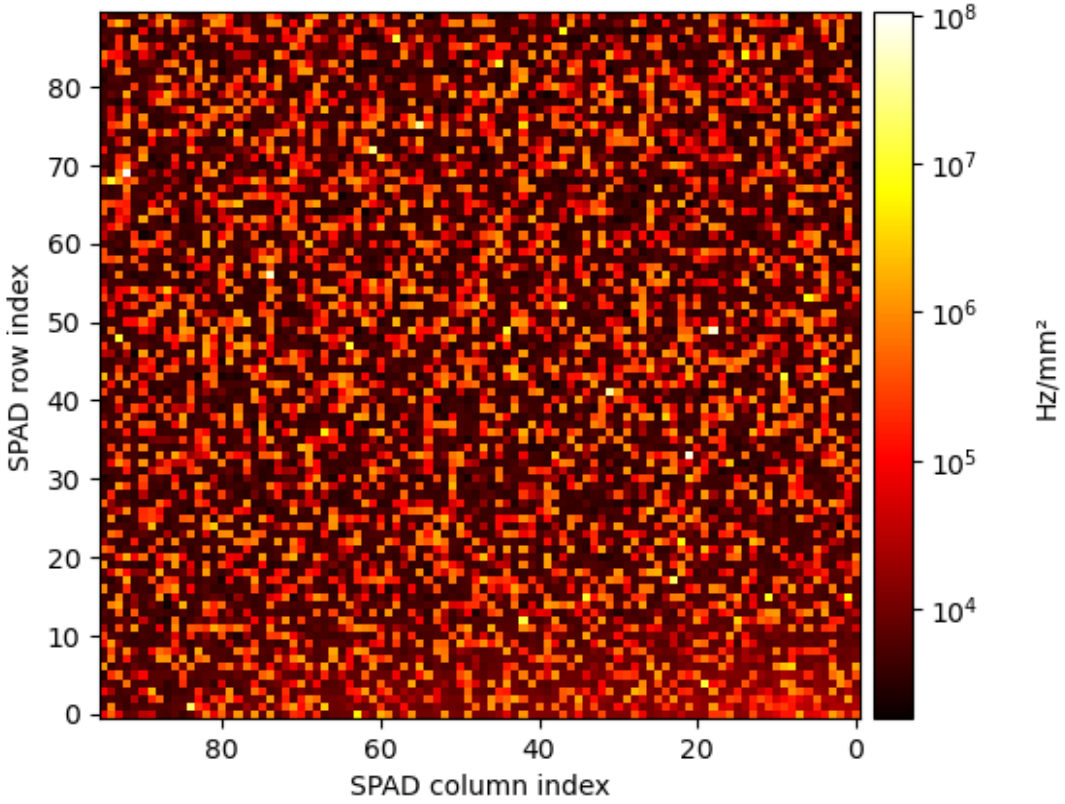
Open issues are (we believ can be fixed):

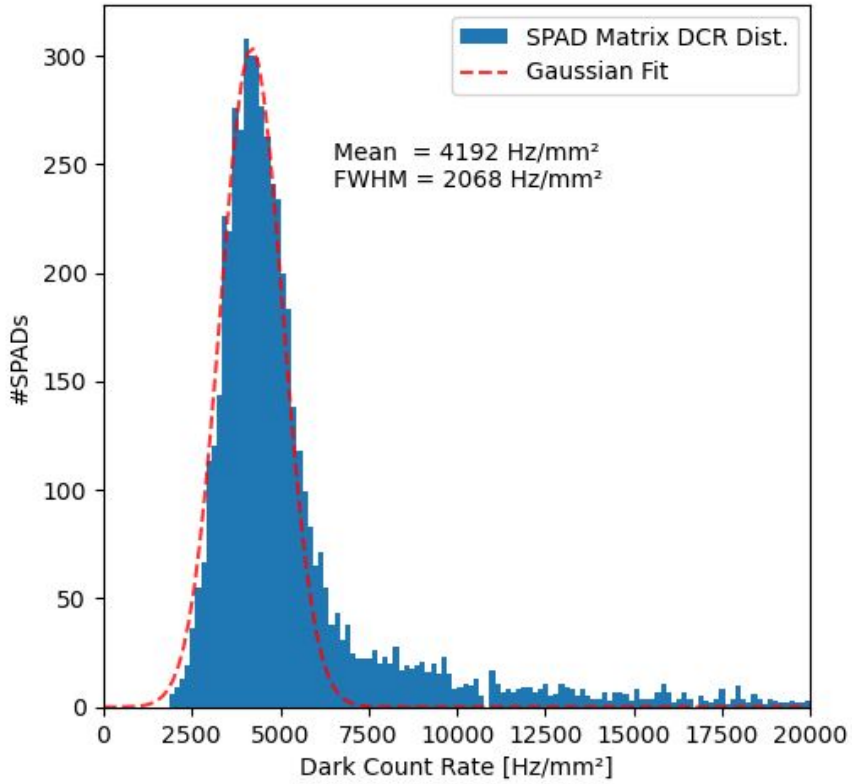
- UV sensitivity (→ use ‘PureB’ process) or use WLS
- Emission of photons from circuitry. Is that an issue in our data-driven design?

Note: This is where WE stand NOW. More groups and more R&D will lead to even better performance

Thank you!

‘DARWIN’ Chip Dark Count Rate at 5°C

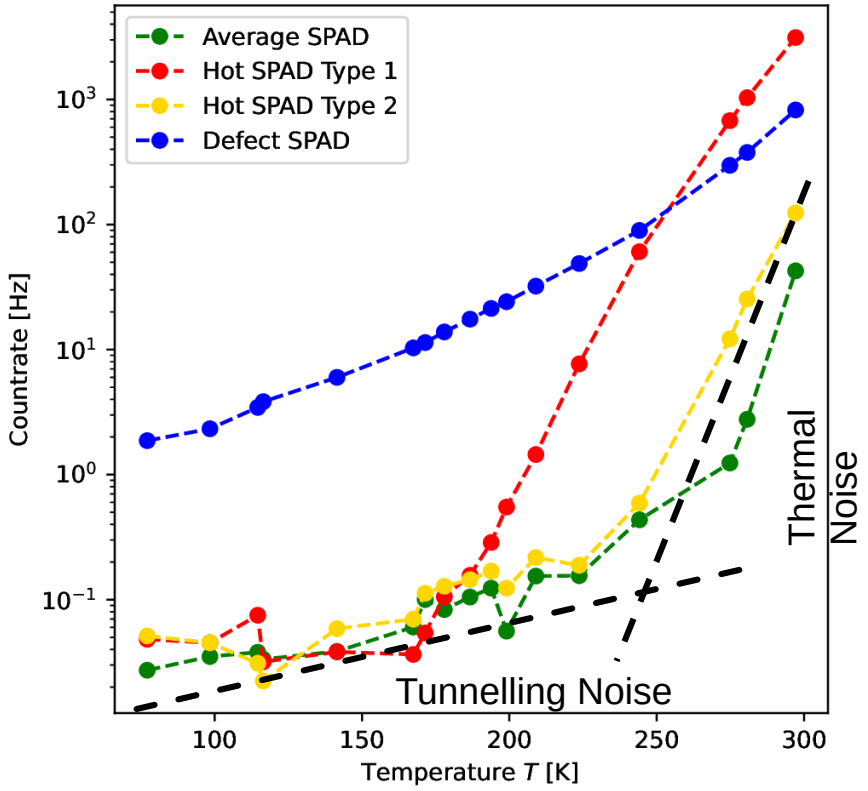


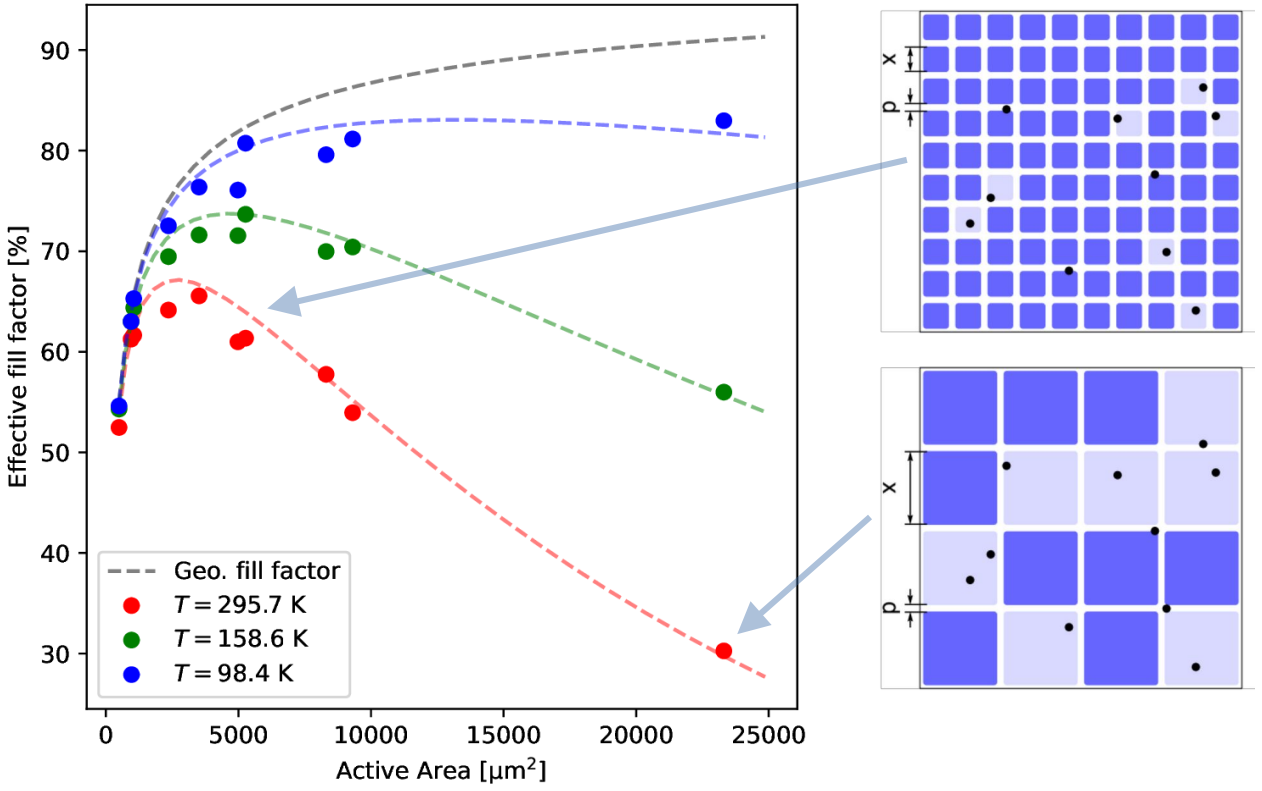


- During the measurement only one SPAD was active
- The main peak respresent the usable “avereage” SPADs
- Mean dark count rate is in agreement with prototype chip
- SPAD with rates > 3σ than mean are „noisy“ SPADs

- ~ 40% are noisy at 5°C, which is 10% higher than expected
- They are evenely distributed over the Chip → production variance
- Chip is designed for LXe temperatures: Noise and #noisy SPADs drop drasticaly! (>0.1Hz/mm² / ~10%)

Hot SPADs

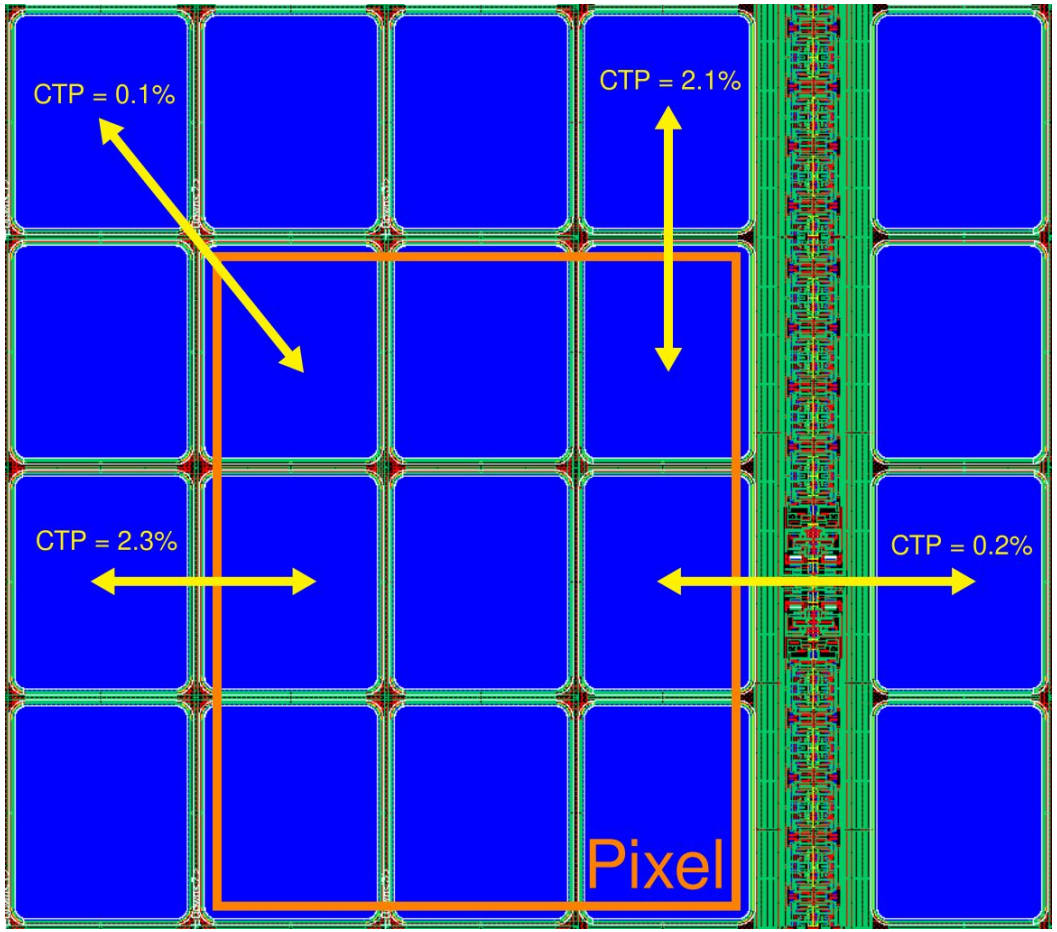




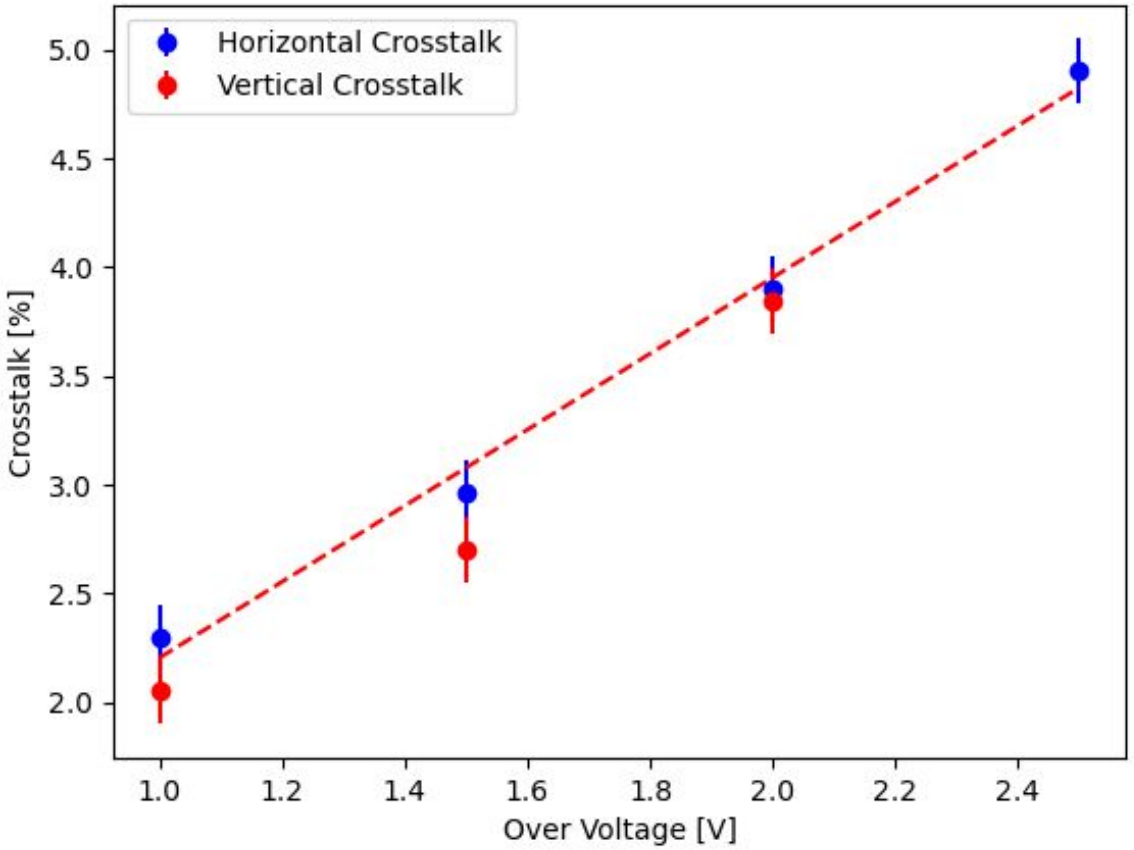
- Hot/noisy SPADs have enhanced thermal noise caused by defects in silicon (some SPADs are not functional).
- At low temperature tunnelling noise becomes dominant even for noisy SPADs. They behave like average ones → number of hot SPADs reduce (= defect freeze out)

- Hot SPADs have to be turned off to lower noise rate, which reduces active area and overall the fill factor (= active Area / total area).
- There is a best SPAD size leading to the highest ‘effective’ fill factor, which increases at lower T since the number of hot SPADs/defects decreases.

Crosstalk



- All pixels are read out and SPADs can be turned off
  → We can measure crosstalk by identifying coincidence hits in neighbouring SPADs.



- We measure 2% crosstalk for a 80x100 µm² SPAD at 1V OV.
- Crosstalk increases with over voltage ~1.8%/V
- We cannot distinguish between direct and indirect crosstalk. Requires finer time resolution (but we have a chip)