

The new Vertex project

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ara Rabaglia -

Summary

- Overview of MIMOSIS-2 characteristics
- Tests on communication with the chip (I²C and register settings)
- Tests on the data read-out and deserialization
- Tests with the full set-up and the radioactive source
- New Vertex design



MIMOSIS-28 VS MIMOSIS-2



MIMOSIS-28 VS MIMOSIS-2



I²C protocol

Experimental Setup



Power Supply:

- Positive pin: +5 V
- Negative pin: 0 V (ground)

Experimental Setup



Conversion of LVDS signals to single-ended signals

DAQ Board \Rightarrow NEW version soon

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Experimental Setup



 $\begin{array}{l} \mathsf{FPGA} \\ (\mathsf{DE10STD}) \end{array} \Rightarrow \mathsf{Final \ setup \ includes \ a \ \mathsf{DE10}} \mathsf{Nano} \end{array}$

Registers to configure the chip

are set through the **I**²**C**

communication protocol

 Communication frequency: 400 kHz

• Many tests of register Read

and Write operations.



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2 Working Configurations

PLL mode	Rescue Clock mode
Clock @40 MHz given by the FPGA	Clock @40 MHz given by the FPGA
Clock @320 MHz (for data read out) generated by the internal PLL	Clock @320 MHz given by an external generator (injected through a jumper on the proximity board)
Default Configuration	Configurable through register 27
Configurable Gain and Threshold to lock the PLL (implemented an automatic scan)	
Clock generated by the PLL very noisy	a - 27/05/25 11

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Data Read-Out

Data read-out

Clock-out @160 MHz

 \rightarrow Data on the rising and falling edge

 \rightarrow Data read-out @320 MHz

- 8 Data read out lines (DOUT)
- 128 bits words
 - \rightarrow 1 word/400 ns [1 lines]
 - \rightarrow 1 word/100 ns [4 lines]
- Trigger \rightarrow saved the frames arrived in the settable window [- Δt , + Δt ']

- 1, 2, 4, 8 DOUTs:
- 1 and 2 lines: widely tested
- 4 lines: tested, but output signals become very noisy
- 8 lines: never tested, odd lines seem

broken

Deserializer



Deserializer



- Alignment between the clock and the data \rightarrow PHASE
- (more than 1 DOUT) Build the word correctly

Deserializer



fcaafcaafcaafcaafcaafcaafcaa
fcaafcaafcaafcaafcaafcaafcaa
fe00fe00fe00fe00fe00fe9ffe7efee0
fcaafcaafcaafcaafcaafcaa <u>7075ff00</u>
fcaafcaafcaafcaafcaafcaafcaa

134	fcaafcaafcaafcaafcaafcaafcaafcaa
135	fcaafcaafcaafcaafcaafcaafcaafcaa
136	fe00fe00fe00fe00fe00fe0fe0ffe7efee1
137	fcaafcaafcaafcaafcaafcaa <u>7070ff00</u>
138	fcaafcaafcaafcaafcaafcaafcaafcaa
139	fcaafcaafcaafcaafcaafcaafcaafcaa
140	fcaafcaafcaafcaafcaafcaafcaafcaa

Data stream:

- Idle words
- Frames:
 - Header (yellow)
 - Frame counter (green)
 - Trail (pink)
 - Hits (FDXX)

NEW Experimental Setup

Radioactive Source: ²⁰⁷Bi [105 kBq, β -]

External Trigger: scintillator + PMT





- Random Trigger
- NO radioactive source
- Possible value for the threshold: 0 1.5 V, step 6 mV (0 to 255)
- ~2000 events (arrived trigger) per threshold value
- 4 sub-matrices

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- Fit with a Sigmoid function to find the Pedestal (P) and the Sigma (σ):

$$S = 0.5 \cdot (\tanh\left(\frac{(x-P)}{\sigma}\right) + 1)$$

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Sub-Matrix A

Sub-Matrix B

- Possible value for the threshold: 0 1.5 V, step 6 mV (0 to 255)
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80 100 Threshold (Decimal Value)

• 4 sub-matrices



-11.61 mm

-11.61 mm

→ - 3.87 mm - →

←3.87 mm→

Random Trigger ٠

4 sub-matrices

Sub-Matrix A

Sub-Matrix B

٠

- NO radioactive source ٠
- Possible value for the threshold: 0 1.5 V, step 6 ٠ mV (0 to 255)
- \sim 2000 events (arrived trigger) per threshold value ٠

0.8

0.2



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-11.61 mm-

→ ← 3.87 mm →

←3.87 mm→

Few runs over the night:



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 \rightarrow Good stability (no errors occur)



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- \rightarrow more than 3M hit collected



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- \rightarrow Good stability (no errors occur)
- \rightarrow more than 3M hit collected
- \rightarrow Analysis of the results: COMING SOON!





New Vertex

Proximity Board

2 MIMOSIS-2 chips per each proximity board

4 Proximity boards

2 DAQ board per proximity board (tot = 8)

1 DE10-nano per proximity board (tot = 4)



Target Holder: Conceptual Design

Conceptual target holder can be especially designed for specific target

 \Rightarrow 3D printer



Target Holder: Board disposition



New Vertex details





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- Tests on communication with the chip ______ Communication with the chip under (I²C and register settings)
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 \rightarrow Better performance than old Vertex

Communication with the chip under control

The data can be decoded, saved in binary files, and useful information can be extracted.

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Automatic threshold scan and run over the night

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- Communication with the chip under control
- The data can be decoded, saved in
 binary files, and useful information can be extracted.
- Automatic threshold scan and run over the night
- \longrightarrow Sketch of the future design

