ASPIDES
WP1- ASIC design and verification

ASPIDE prototype for Cherenkov detection

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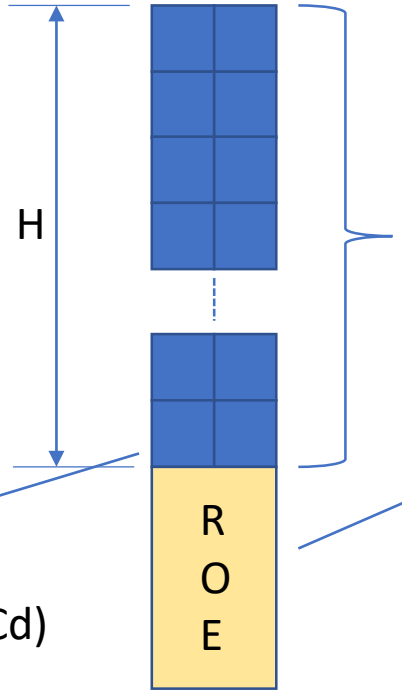
Macro-pixel architecture



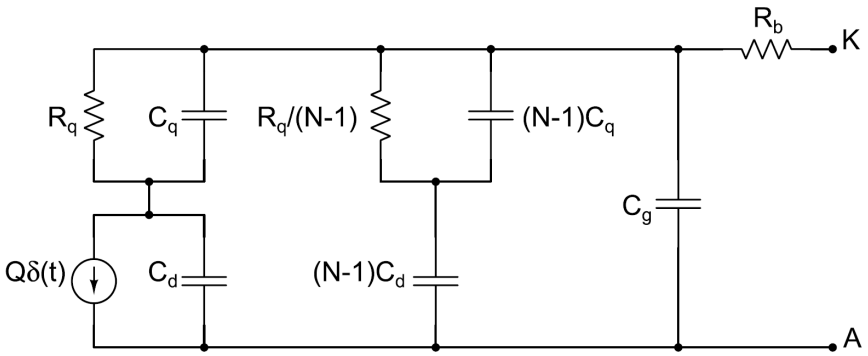
SiPM:

- Number of ucells (N) depends on the Cq/Cd and the required vertical height (H)

ReadOut Electronics: designed to measure the ToA and number of fired micro-cells by means of the ToT

Micro-cell:

- APD (current source and Cd)
- quenching resistor Rq
- Parasitic capacitance Cq



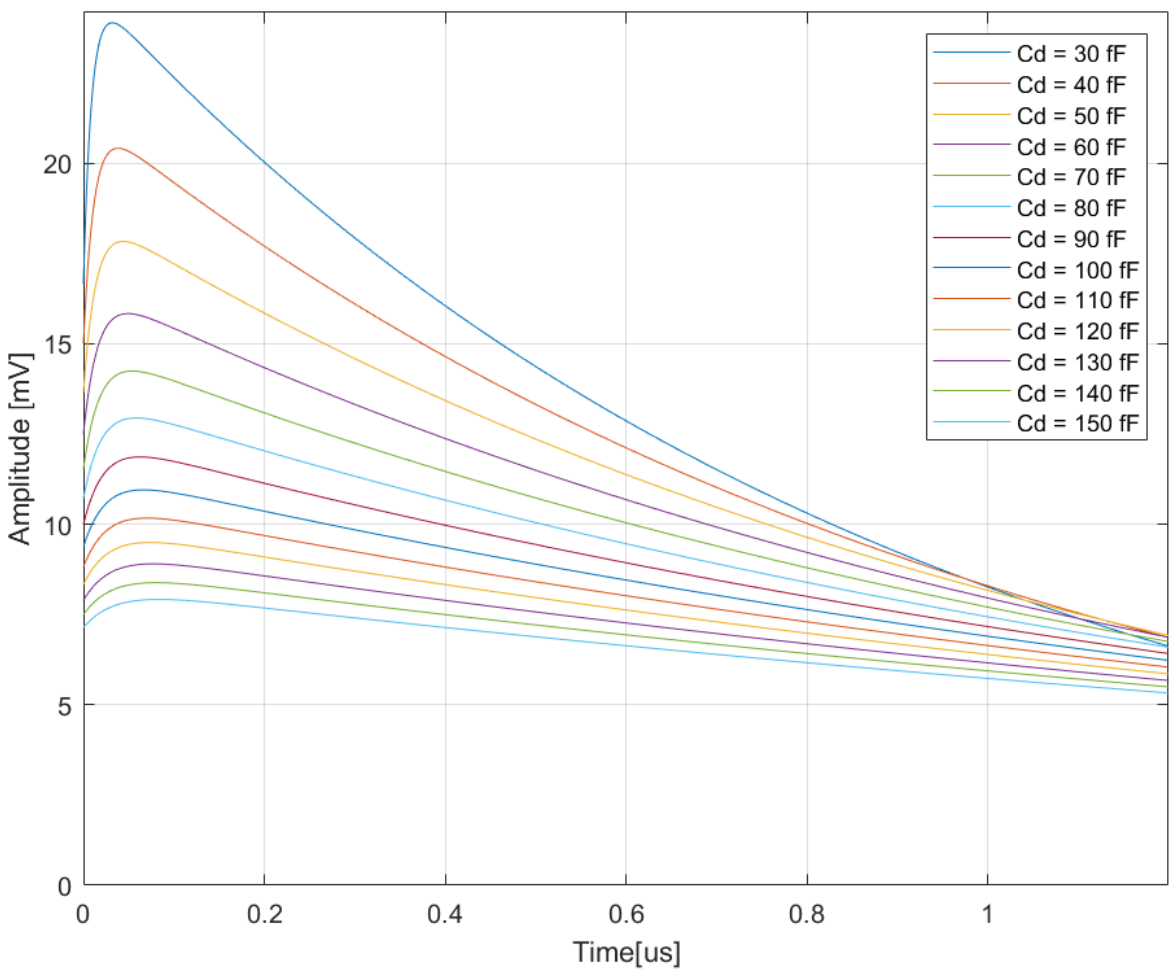
When a ucell fires it produces at the SiPM output a very fast voltage step followed by the recovery tail.
The step amplitude depends on:

- SiPM over-voltage
- Cq, Cd and Cg
- SiPM size

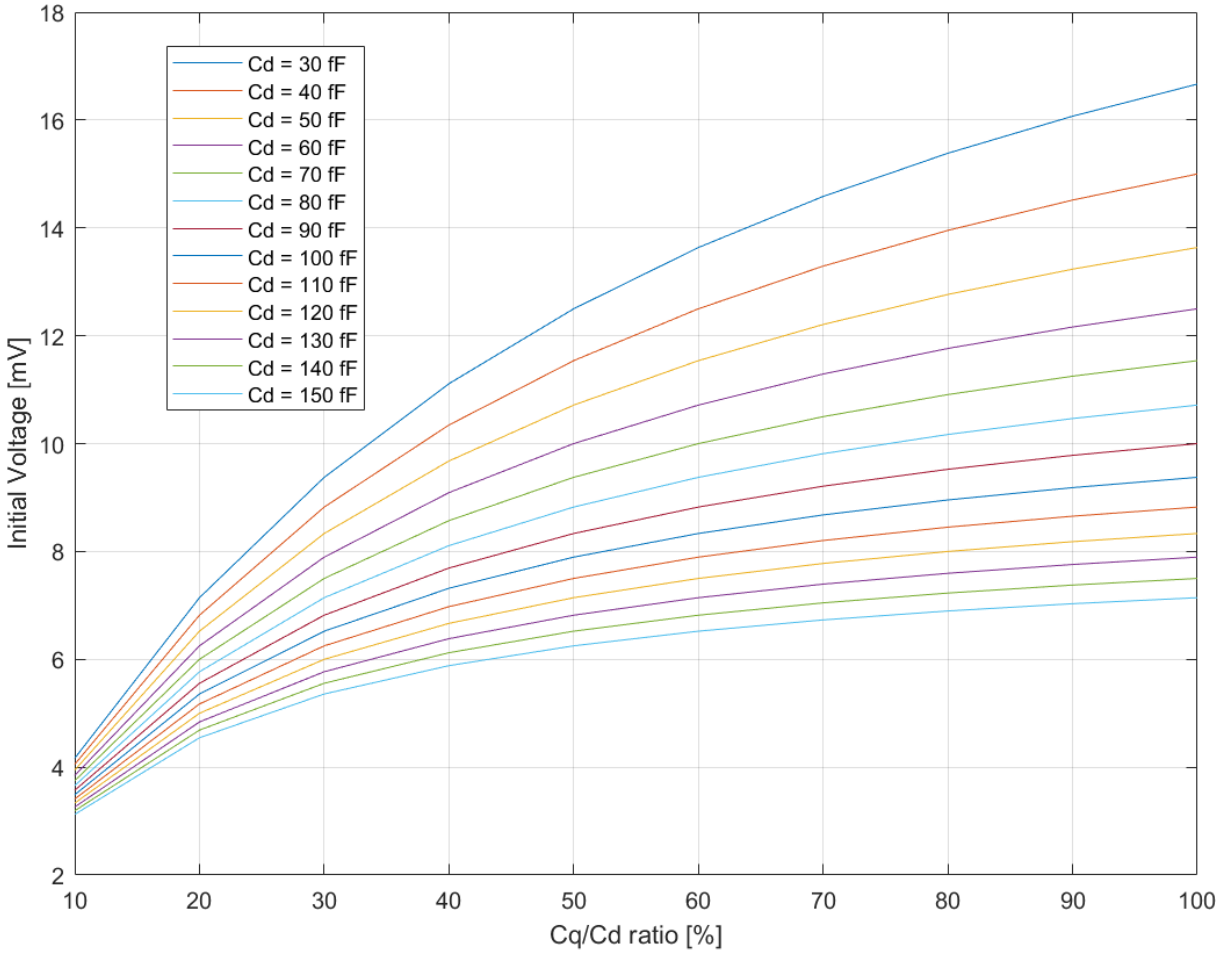
$$V_{step} \approx \frac{V_{OV}}{\frac{N}{1+{C_q}/{C_d}} + \frac{C_g}{C_q}}$$

The idea is to control the Cq/Cd ratio and the SiPM size (N, Cg) in order to have a step that can be directly used to mark the arrival time without using any amplifier.

Macro-pixel simulation with 1 micro-cell firing



SiPM response – zoom on the initial part

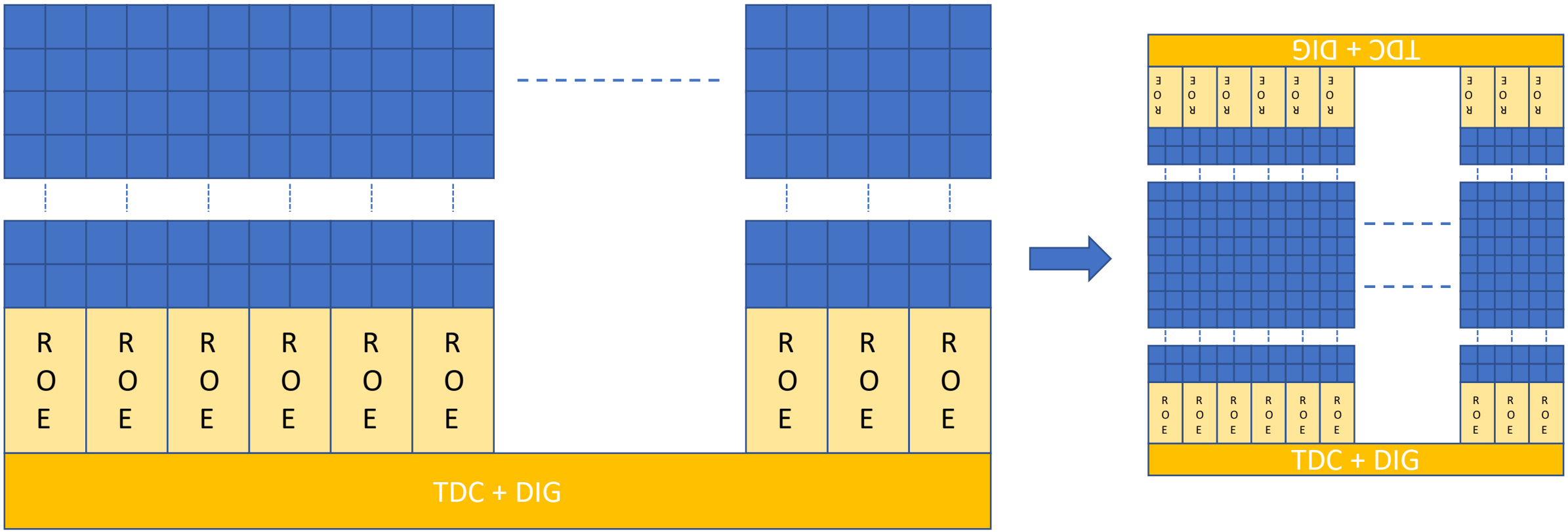


SiPM response initial value vs Cq/Cd ration

Simulation conditions: Cd = 100 fF, Rq = 200 kOhm, N = 100, Cg = 3 pF, Q0 = 150 fC, Ri = 150 kOhm

SiPM architecture

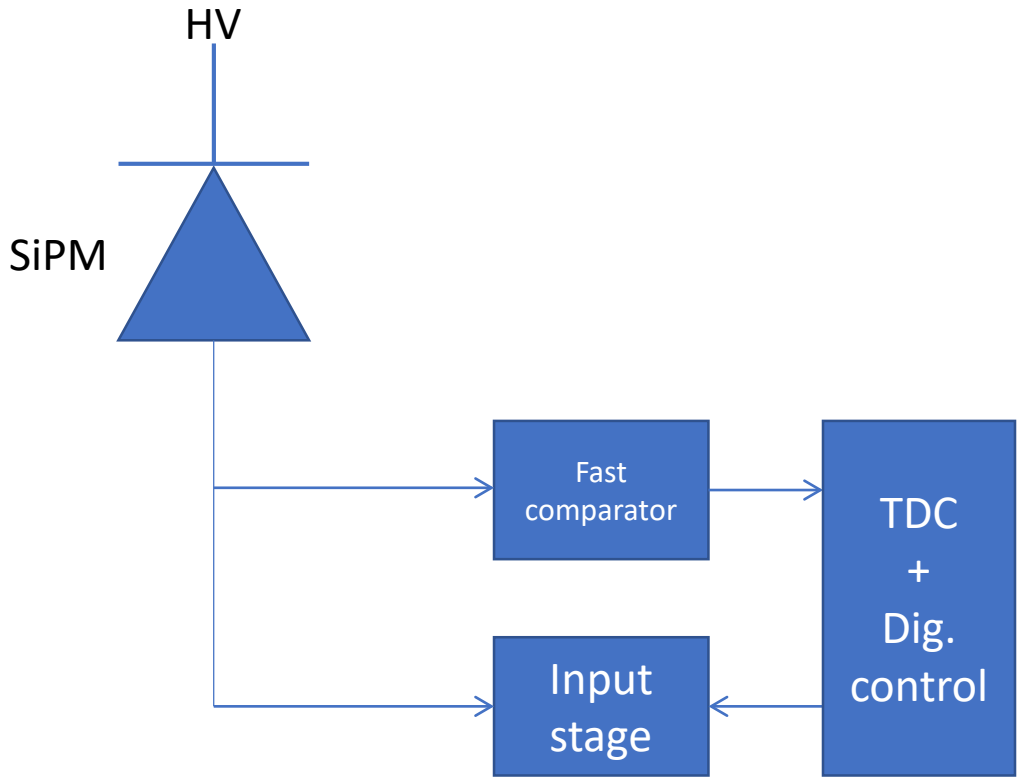
- HALF MODULE: macro-pixels can be horizontally abutted in order to realize an array of the required length, at the bottom of the ROE line the TDC + digital section can be placed.
- FULL MODULE: mirroring the HALF MODULE respect to the x – axis the whole SiPM is obtained



HALF MODULE

FULL MODULE

ReadOut Electronics



Input stage:

- Provides the equivalent small signal resistance to read the SiPM
- Controls the SiPM bias for a fine adjustment of the SiPM gain
- Performs the discharge at constant current of the input node (SiPM anode) in order to measure the number of detected photons (ToT)

Fast comparator:

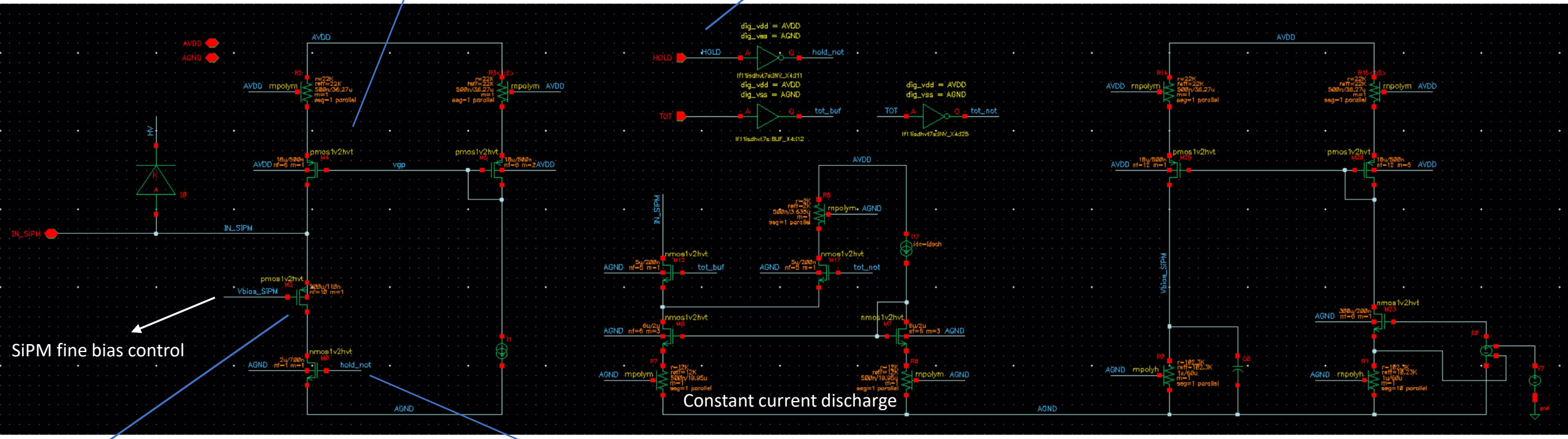
- Produces an output pulse whose rising edge marks the arrival time of the incoming event and whose duration is proportional to the number of detected photons.

Input Stage architecture

To be understood if also this branch must be switched off during the hold phase

Digital inputs:

- HOLD: when the rising edge is detected the input transistor branch is opened, charge is integrated at input node
- TOT: enables the discharge at constant current



SiPM fine bias control

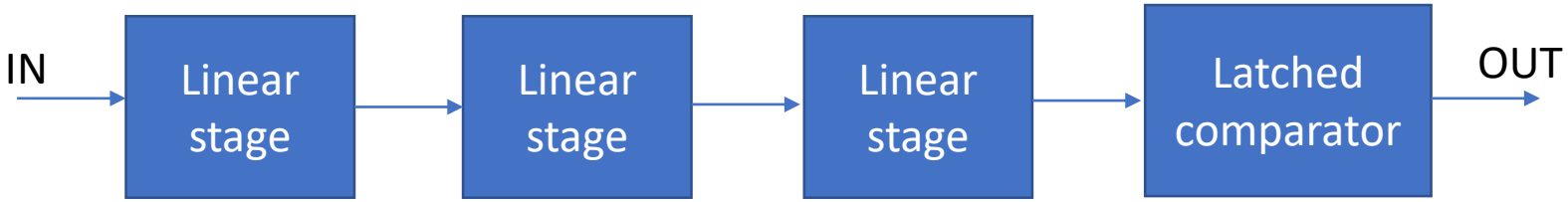
Input transistor:

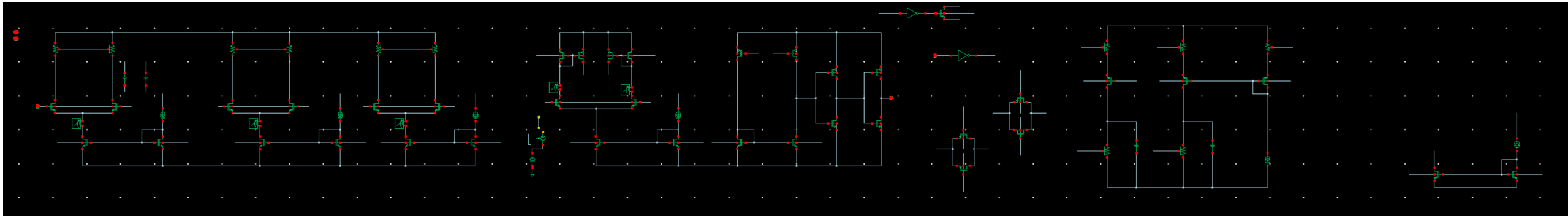
- Provides the equivalent input resistance
- Controls the SiPM bias

Switch:

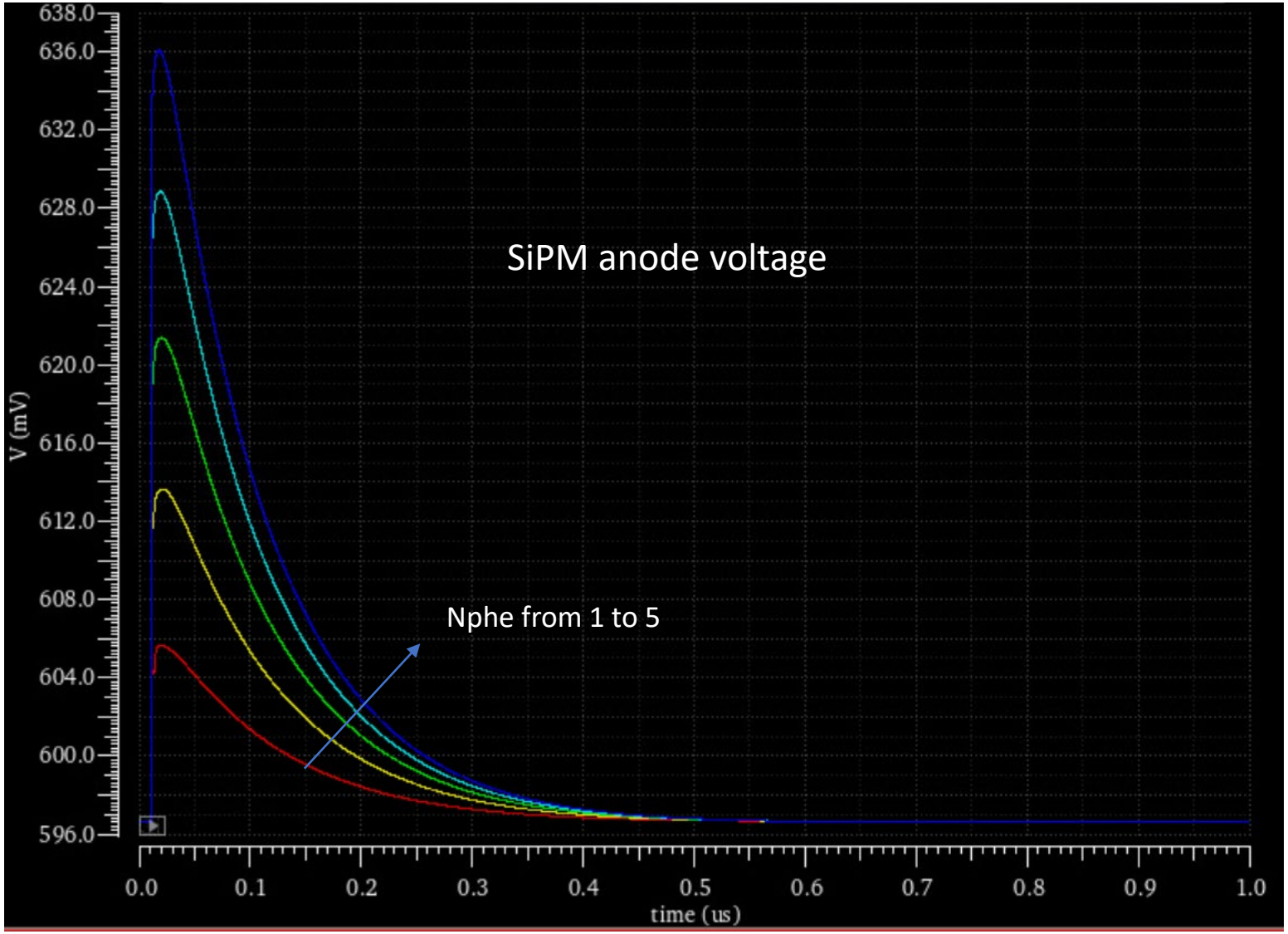
- ON: normal operation
- OFF: hold and constant current discharge

Fast comparator architecture





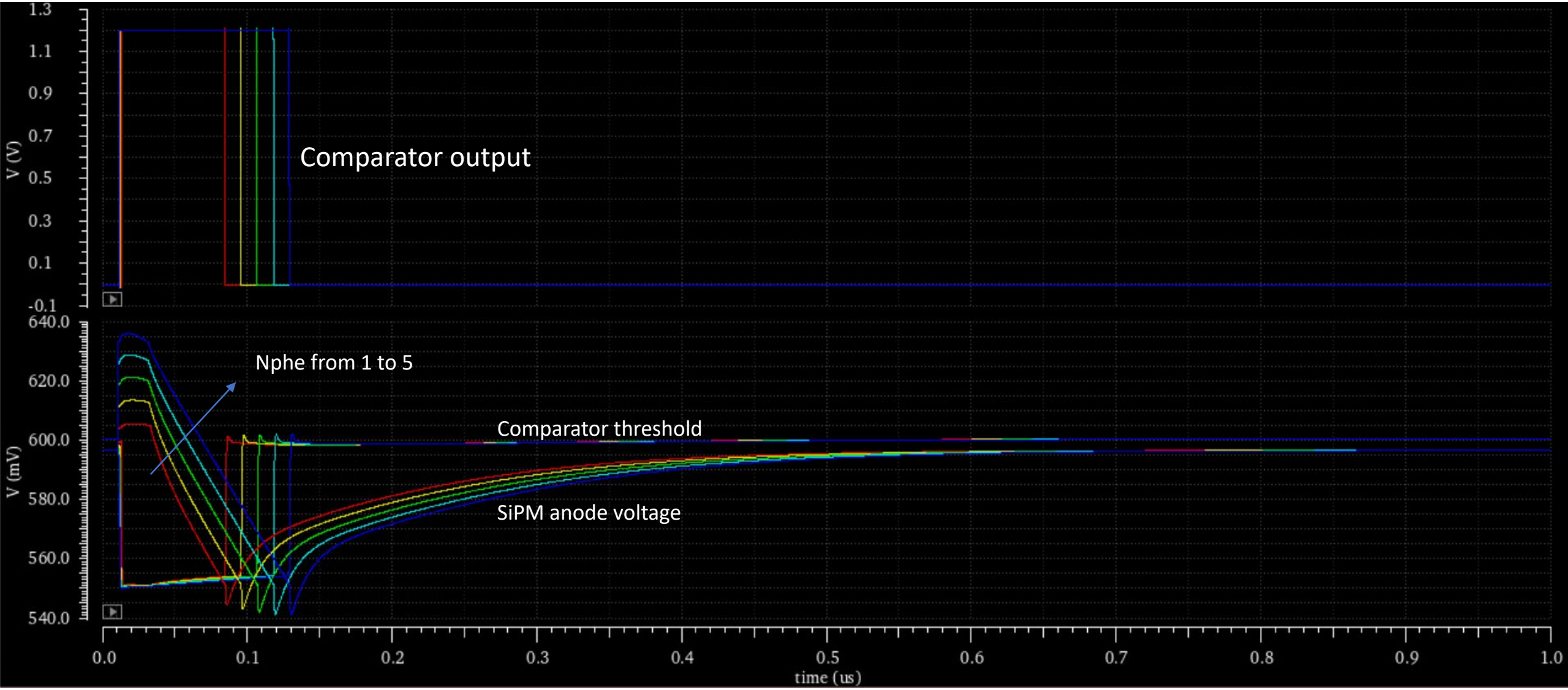
Simulation: transient time – no ToT



ToT not active - Equivalent input resistance has been chosen in order to recover in about 500 ns

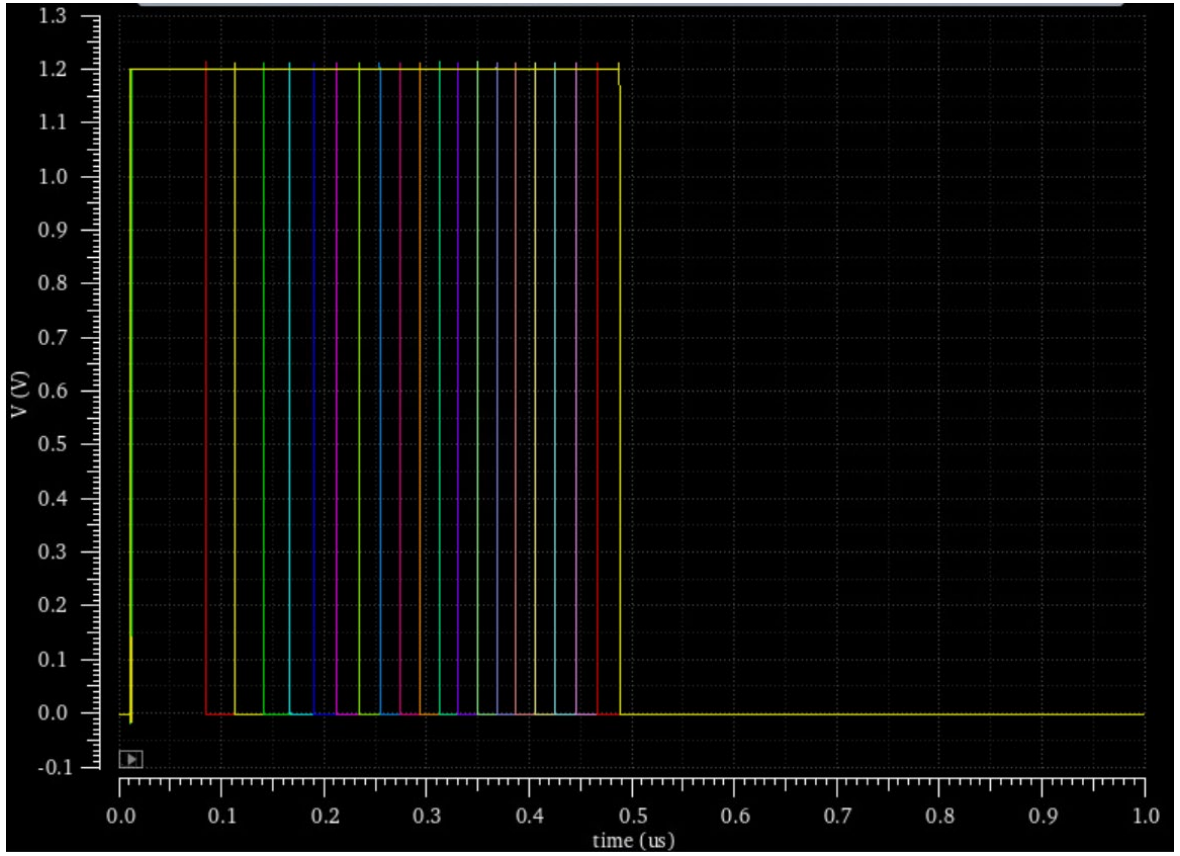
Simulation conditions: Cd = 100 fF, Cq = 40 fF, Rq = 200 kOhm, N = 90, Cg = 3 pF, Q0 = 150 fC, Ri = 150 kOhm

Simulation: transient time – ToT for 1 - 5 phe

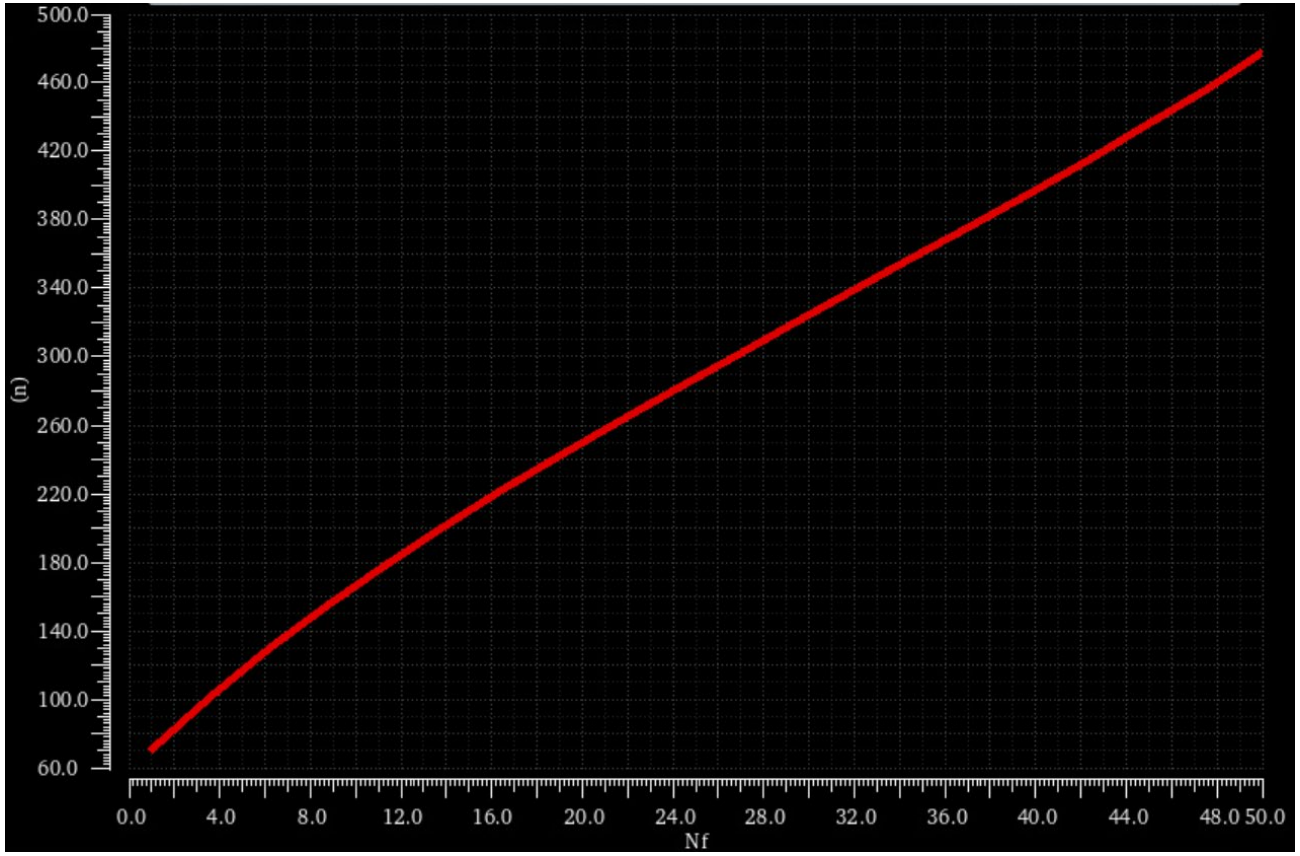


ToT active – measurement for input event from 1 to 5 photons

Simulation: transient time – ToT for 1 – 50 phe

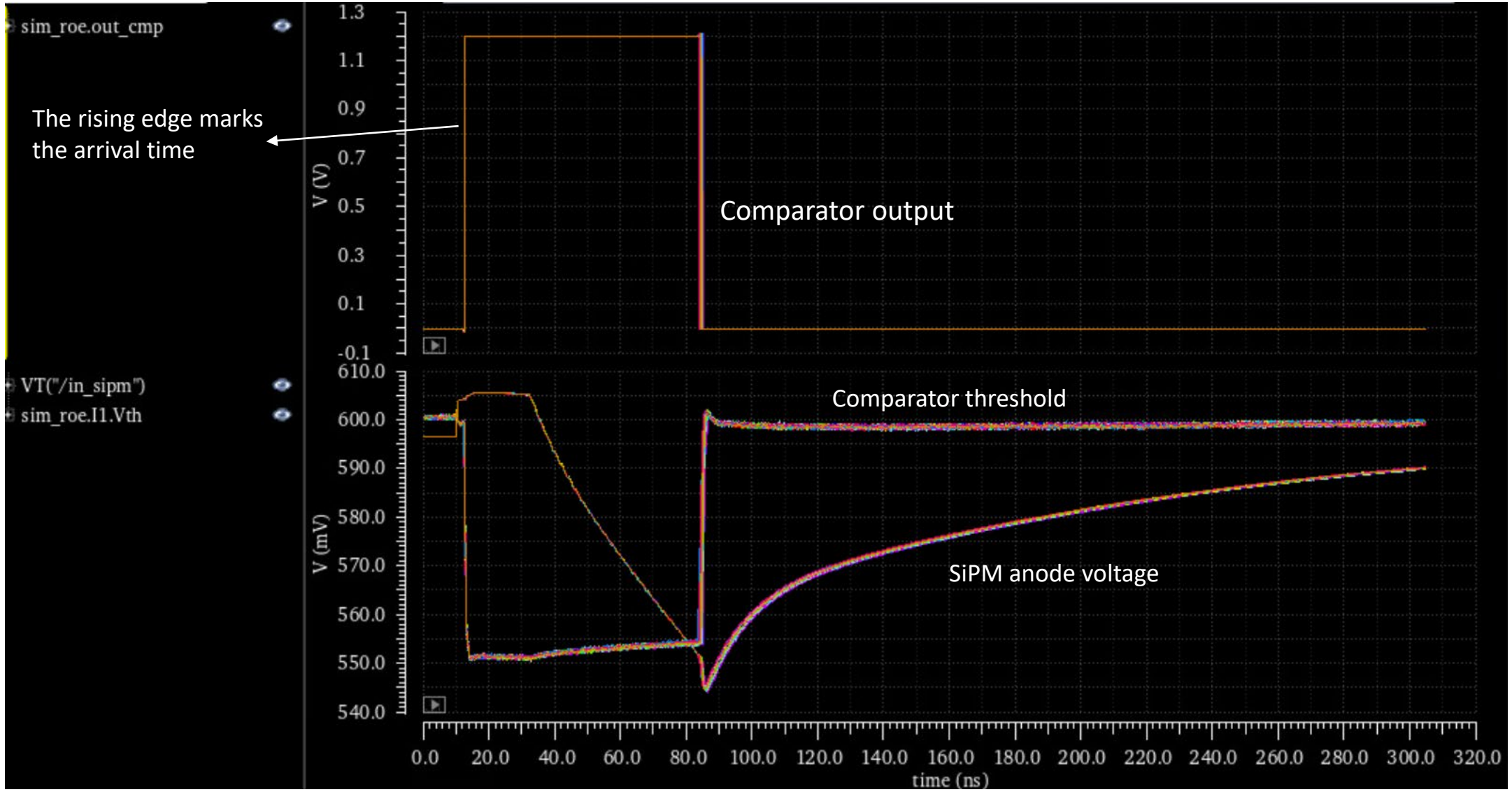


Comparator output for Nf from 1 to 50



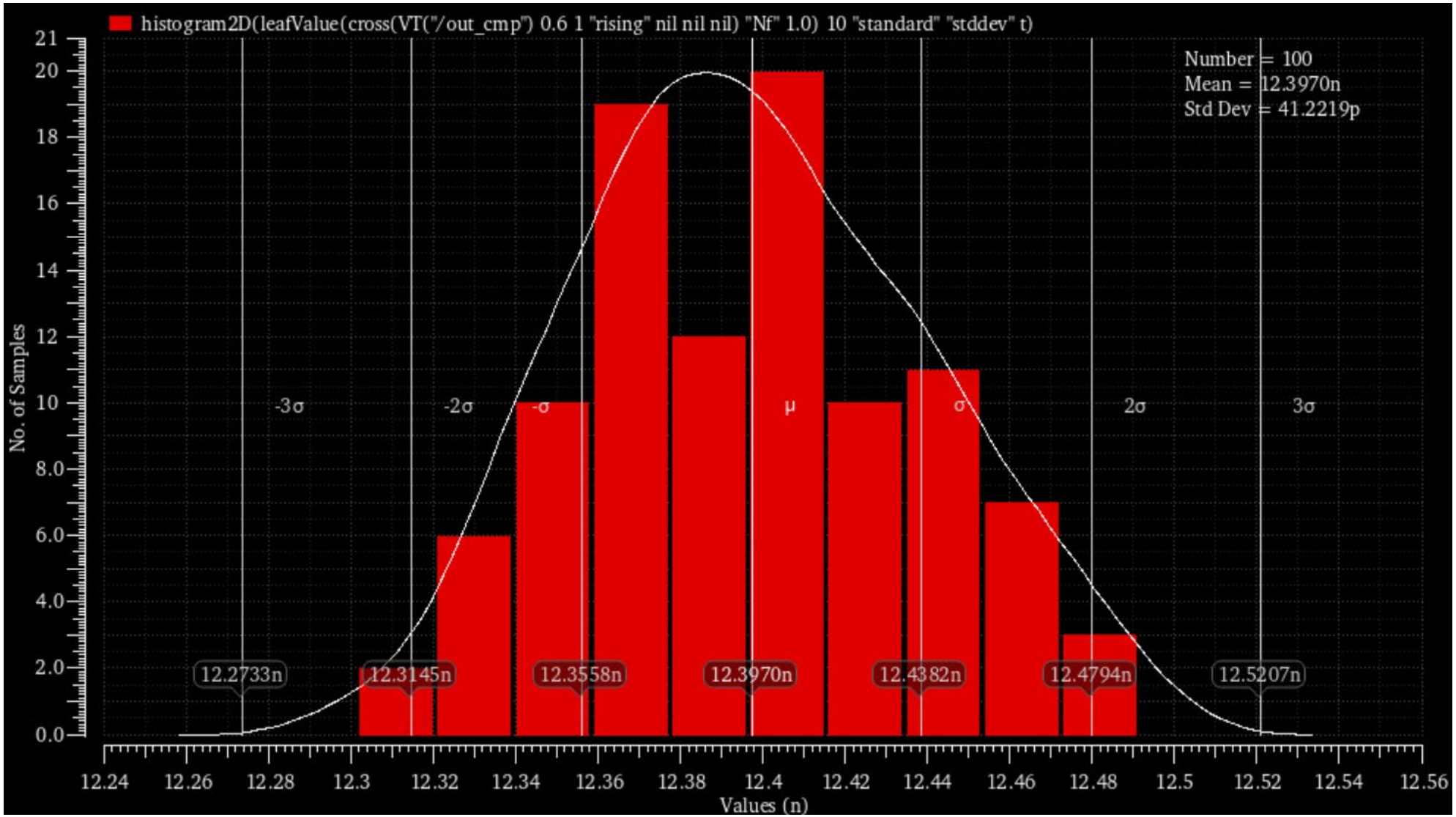
Comparator output duration for Nf from 1 to 50

Simulation: transient noise - 1 phe



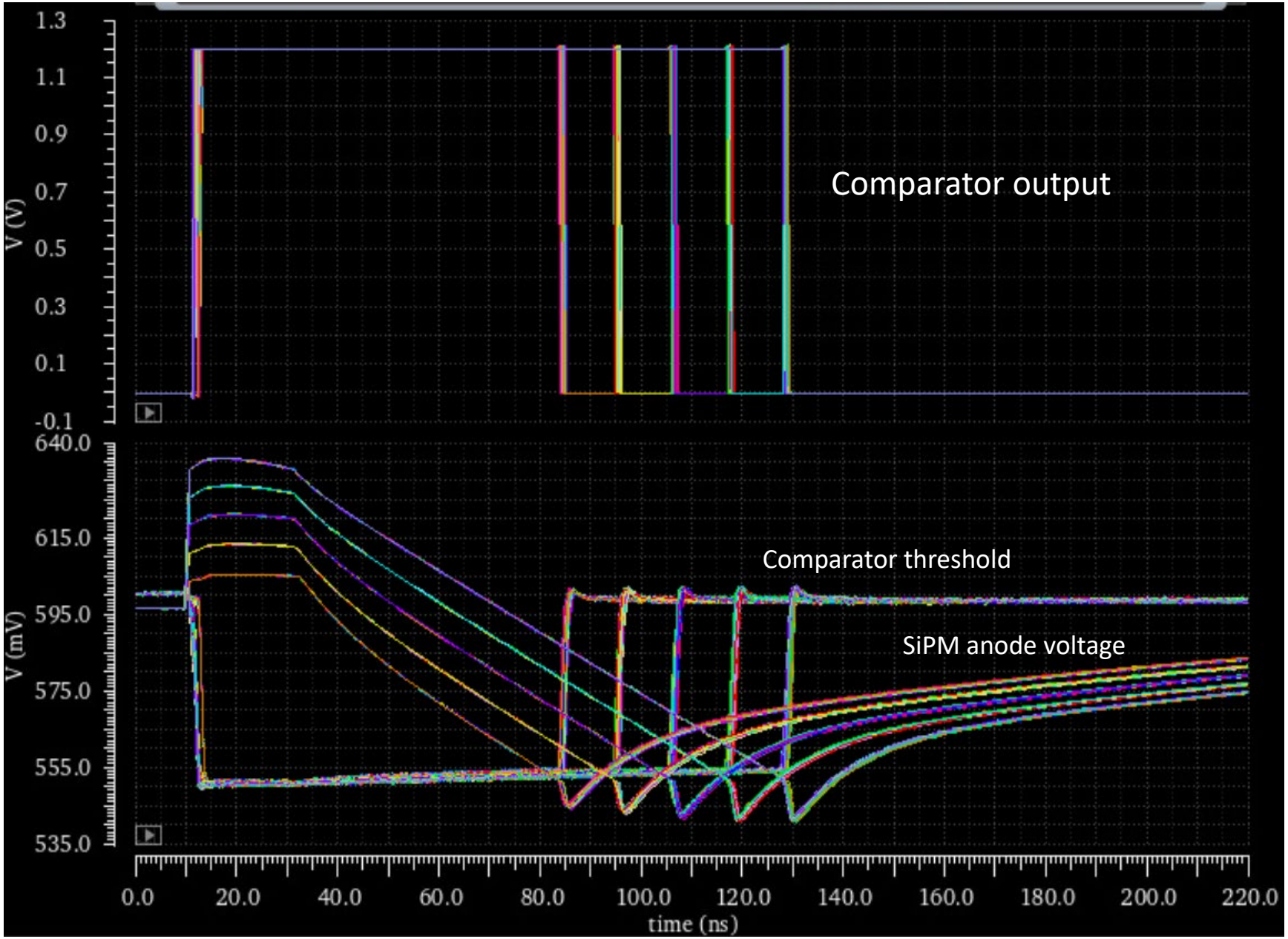
100 runs of transient noise

Simulation: transient noise - 1 phe – jitter ToA

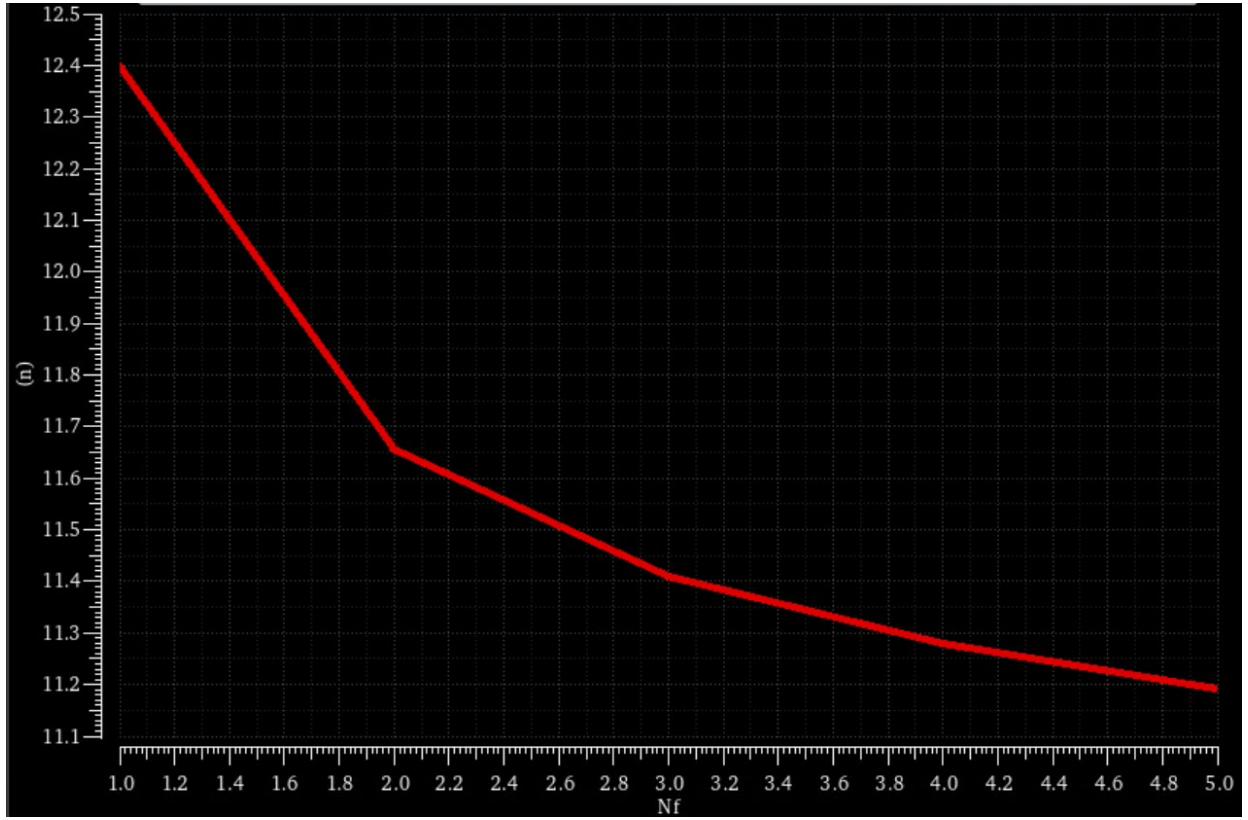


Time jitter measured on the rising edge of comparator output (50% transition point)

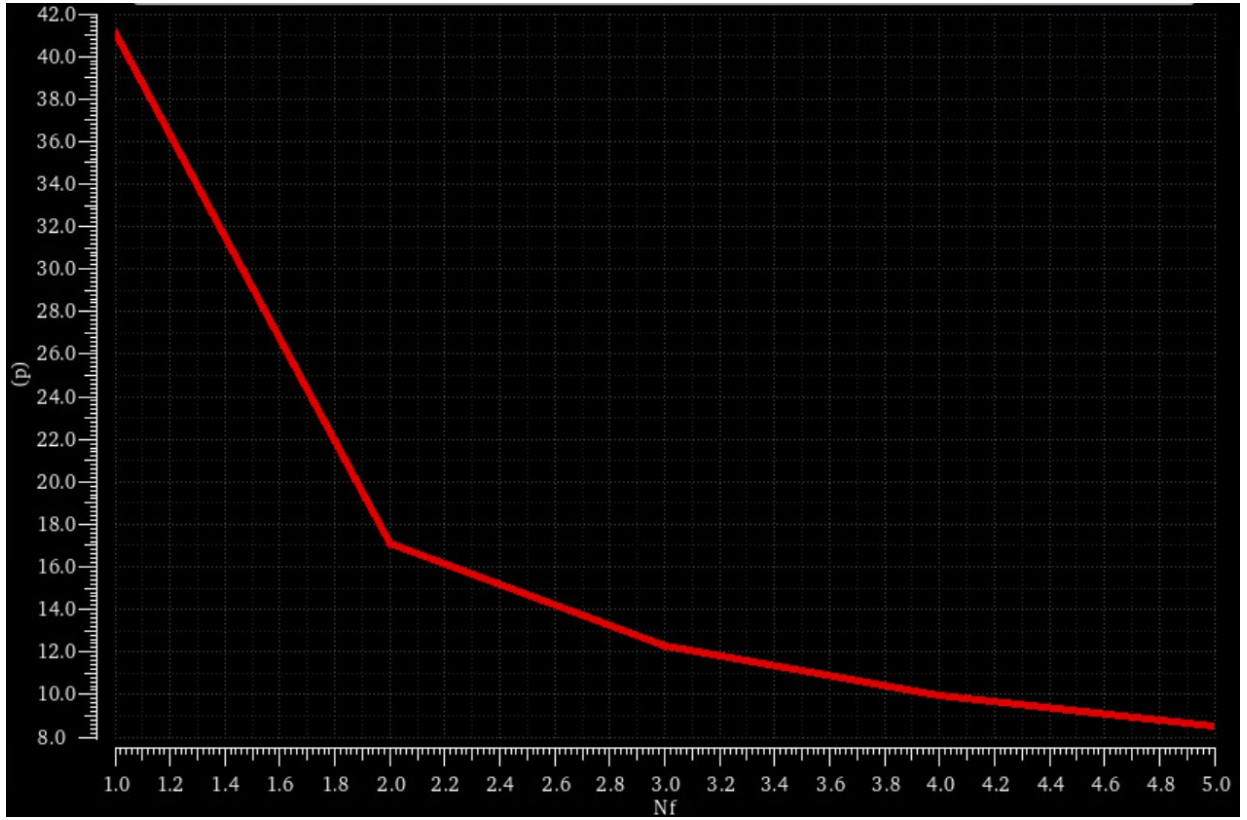
Simulation: transient noise – 1 to 5 phe



Simulation: transient noise – 1 to 5 phe - ToA



ToA – time walk



ToA – time jitter