Introductory course to VHDL and HLS FPGA programming

Contribution ID: 14

Type: not specified

UART receiver unit

Wednesday, 25 June 2025 11:30 (2 hours)

Implementation and simulation in VHDL of a UART receiver unit

Presenter: TRIOSSI, Andrea (Universita' degli Studi di Padova) **Session Classification:** Hands on