ALCOR bus and differential lines: FEE and RDO “for production”

Alcor bus: 1 Alcor64 + 1 Alcor64 → FEB TOP 14/02/2025

		1	2V5	2	GND		
F10		3	I2C_SDA	4			AB9
G10		5	I2C_SCL	6			AB10
		7	GND	8	GND		
W19		9	TP_2P	10	TP_1P		Y16
V19		11	TP_2N	12	TP_1N		W16
		13	GND	14	GND		
U20		15	SCLK_2P	16	SCLK_1P		AB15
T20		17	SCLK_2N	18	SCLK_1N		AB14
		19	GND	20	GND		
AA16		21	SDI_2	22	SDI_1		AA13
AB17		23		24			U18
		25	GND	26	GND		
W22		27	Q7_2P	28	Q7_1P		Y15
V22		29	Q7_2N	30	Q7_1N		Y14
		31	GND	32	GND		
U22		33	Q6_2P	34	Q6_1P		W14
T22		35	Q6_2N	36	Q6_1N		V14
		37	GND	38	GND		
R21		39	Q5_2P	40	Q5_1P		U15
T21		41	Q5_2N	42	Q5_1N		T15
		43	GND	44	GND		
R20		45	Q4_2P	46	Q4_1P		Y13
R19		47	Q4_2N	48	Q4_1N		W13
		49	GND	50	GND		
P22		51	Q3_2P	52	Q3_1P		T18
P21		53	Q3_2N	54	Q3_1N		T17
		55	GND	56	GND		
P18		57	Q2_2P	58	Q2_1P		V17
R18		59	Q2_2N	60	Q2_1N		U17
		61	GND	62	GND		
P16		63	Q1_2P	64	Q1_1P		W18
R16		65	Q1_2N	66	Q1_1N		W17
		67	GND	68	GND		
N19		69	Q0_2P	70	Q0_1P		Y19
P19		71	Q0_2N	72	Q0_1N		Y18
		73	GND	74	GND		
W21		75	NRES2_P	76	NRES1_P		AB19
V21		77	NRES2_N	78	NRES1_N		AA18
		79	GND	80	GND		
Y8		81	SS_N_2	82	SS_N_1		AB8
Y9		83		84			AA8
		85	GND	86	GND		
AB6		87	SDO_2P	88	SDO_1P		AB20
AB7		89	SDO_2N	90	SDO_1N		AA21
		91	GND	92	GND		
Y21		93	CLK_2P	94	CLK_1P		V15
Y20		95	CLK_2N	96	CLK_1N		U14
		97	CLK_OUT_2P	98	CLK_OUT_1P		
		99	CLK_OUT_2N	100	CLK_OUT_1N		

current scheme overcomes a limitation of ARTIX diff. pins (no diff. output from the point of view of FPGA allowed on certain pins)

we use as single ended the less critical: SDI and SS

however they are now placed close to “empty pins”

for final RDO and FEB we could then have the single-ended output on the FPGA → but s.e. to LVDS transl on RDO → ALCOR bus fully differential

this could be certainly an in-principle “desirable setup” for final RDO + FEB (so no dilemma in my view…)

In my view a final decision should be however evaluated based on:

- learning how it works current setup
- other modifications we might need to implement!