ALCOR DAY

Torino 25/02/2025

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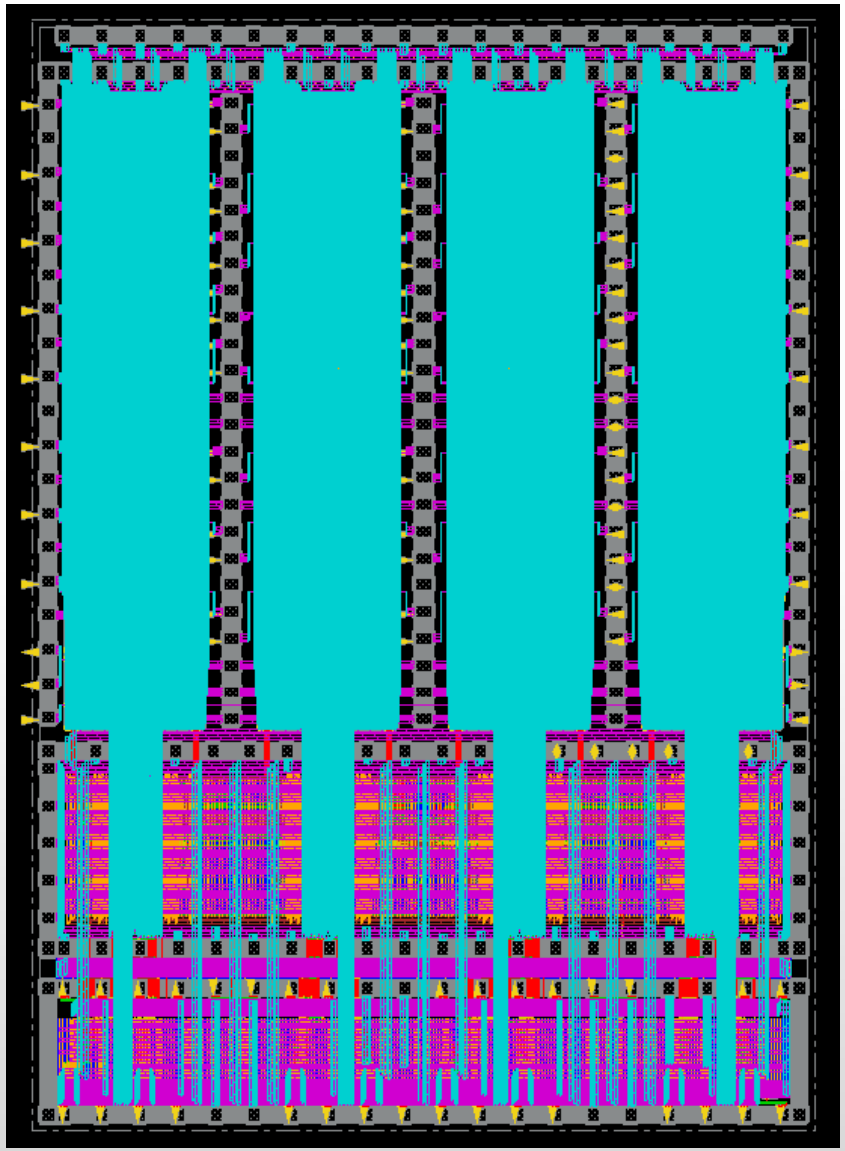
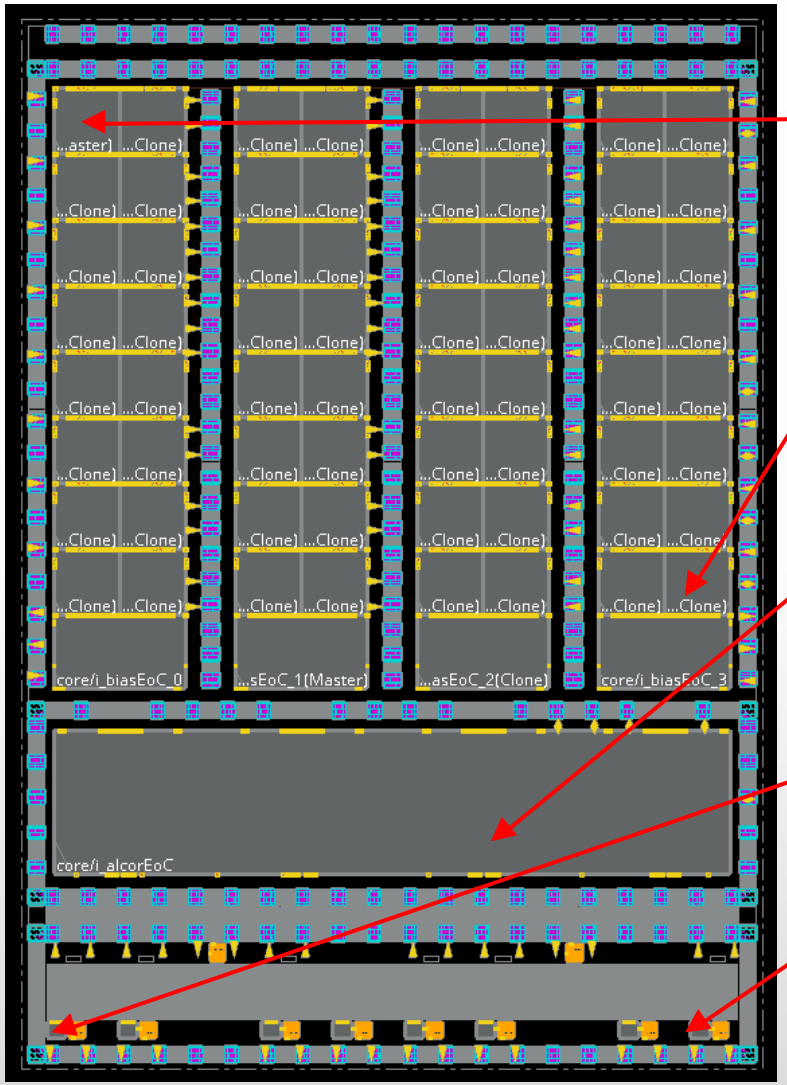
ALCOR 3



Digital blocks



Pixel x 64

End Of Column + SPI
(8 replicated readout circuits)

DDR x8

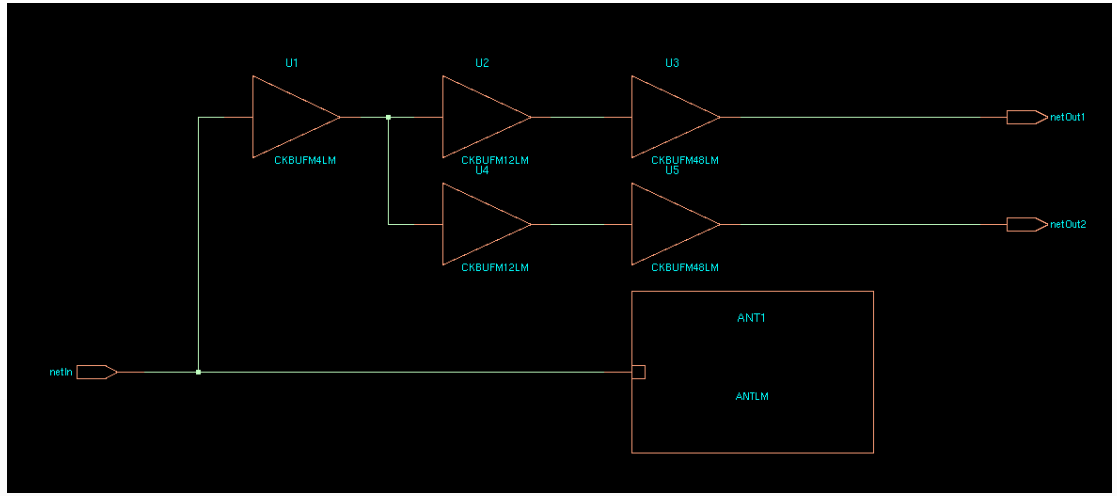
Status

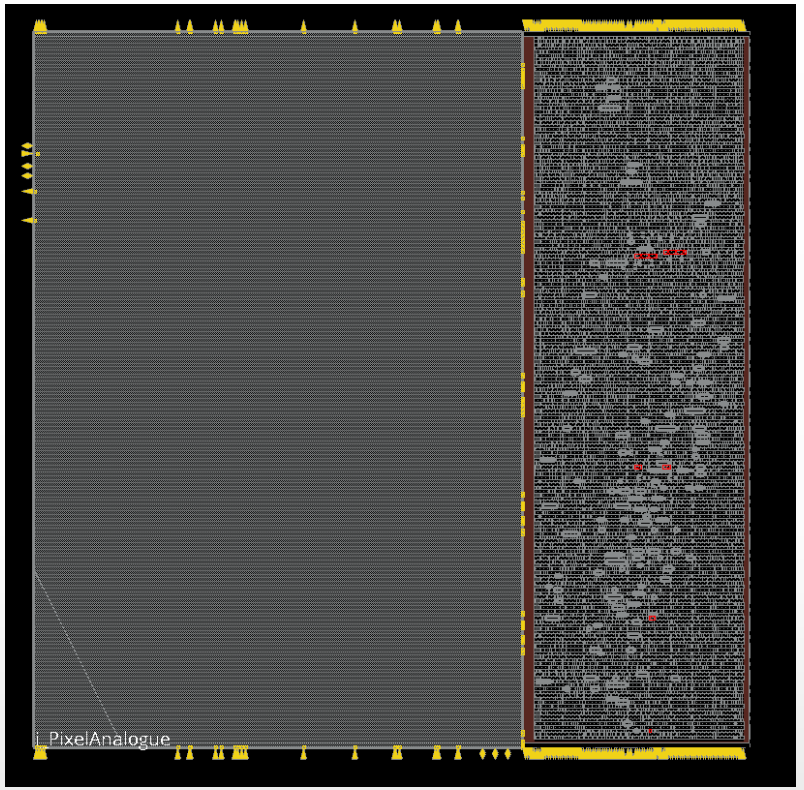
- Pixel digital: STA and DRC free, post pnr simulations ok
- EoC: STA few errors on configuration signals (maybe false path) and few transition errors to fix with ECO. Post pnr simulations done with assembled design
- DDR: STA and DRC free, post pnr simulations ok
- Assembled design done, full netlist available for simulations and power analysis
- Debug on timing and few DRC errors
- Full chip post pnr simulations done with delays without timing checks for now
- Power analysis done
- To do:
  - Reset counters TMR (to do for sure)
  - SPI logic TMR

Critical signals

- CLK 400 MHz
- DDR output 800 MHz
- Test Pulse, also used for fast shutter (Pixel Digital)
- Reset distribution with 3 different features depending on the signal width:
  - 24-31 xCLK: Hard Reset
  - 16-23 xCLK: Start (Frame Counter = 0 and Coarse Counter = 0)
  - 8-15 xCLK: New Orbit (Frame Counter +1 and Coarse Counter =0)
- Power distribution and analogue signals

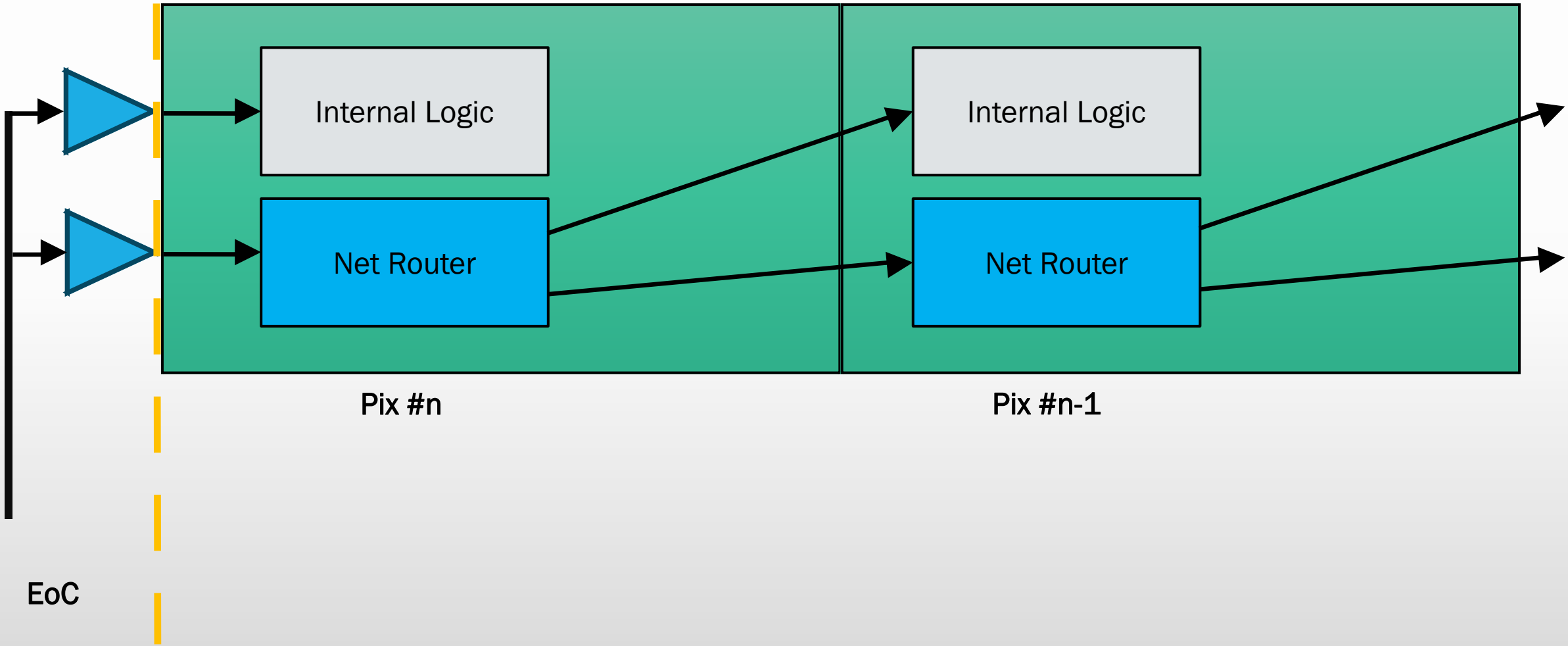
Pixel signals propagation





- Pixel to pixel signal propagation
  - Automatic tree for most of them
  - Dedicated routing for TP, Start, Reset and CLK (Net Router component)
- TDC triggers with “dont_touch” constraints require eco operations to fix transition errors

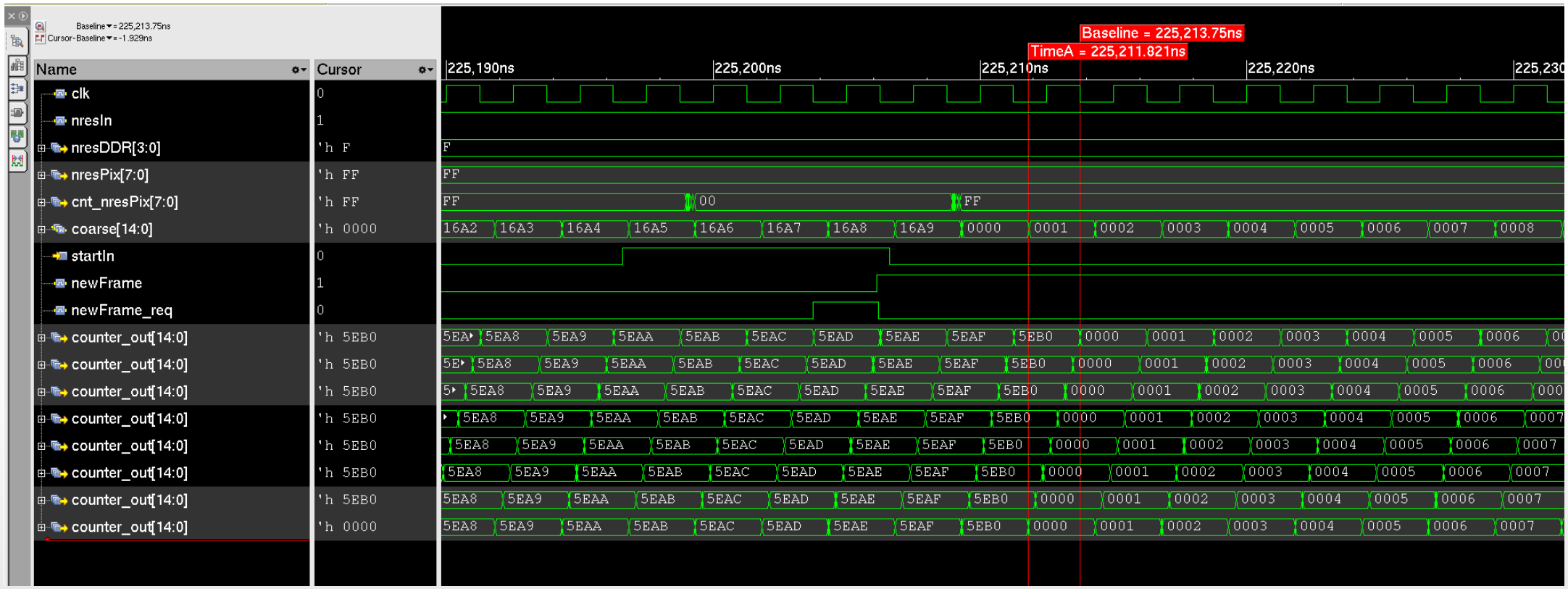
Net Router


Internal Logic
Net Router
Internal Logic
Net Router
Pix #n
Pix #n-1
EoC

Reset operations

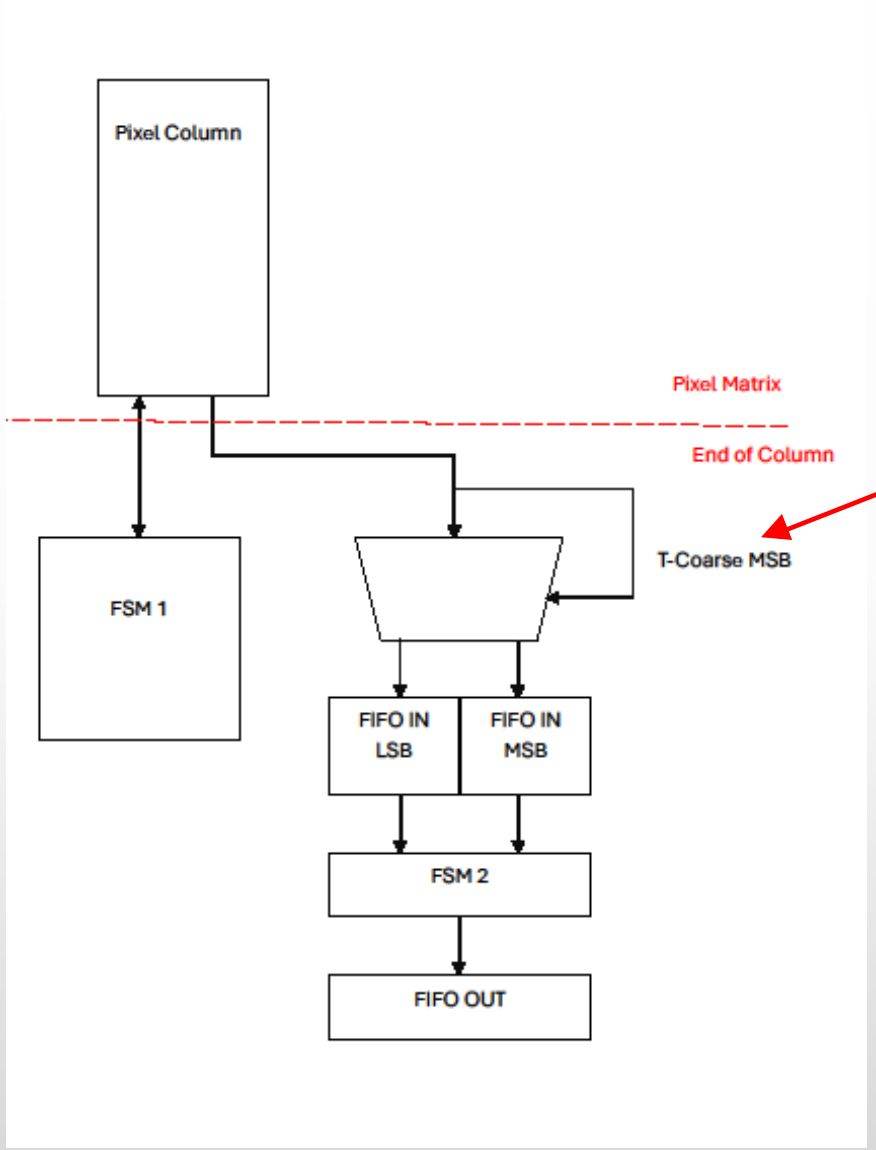
- Reset distribution with 3 different features depending on the signal width:
  - 24-31 xCLK: Hard Reset
  - 16-23 xCLK: Start (Frame Counter = 0 and Coarse Counter = 0)
  - 8-15 xCLK: New Orbit (Frame Counter +1 and Coarse Counter =0)
- A single FSM (TMR protected) manages the incoming reset signal
- First frame sent after EoC configuration
- New orbit forces a rollover condition (same behaviour)
- Reset latency. Reset command is decoded at the end of its cycle. Reset distribution inside the chip adds more latency because the are synchronizer circuits inside the EoC and Pixel logic. So, Coarse Counter reset is performed 12 clks after the reset signal is de-asserted (30 ns)

Reset distribution



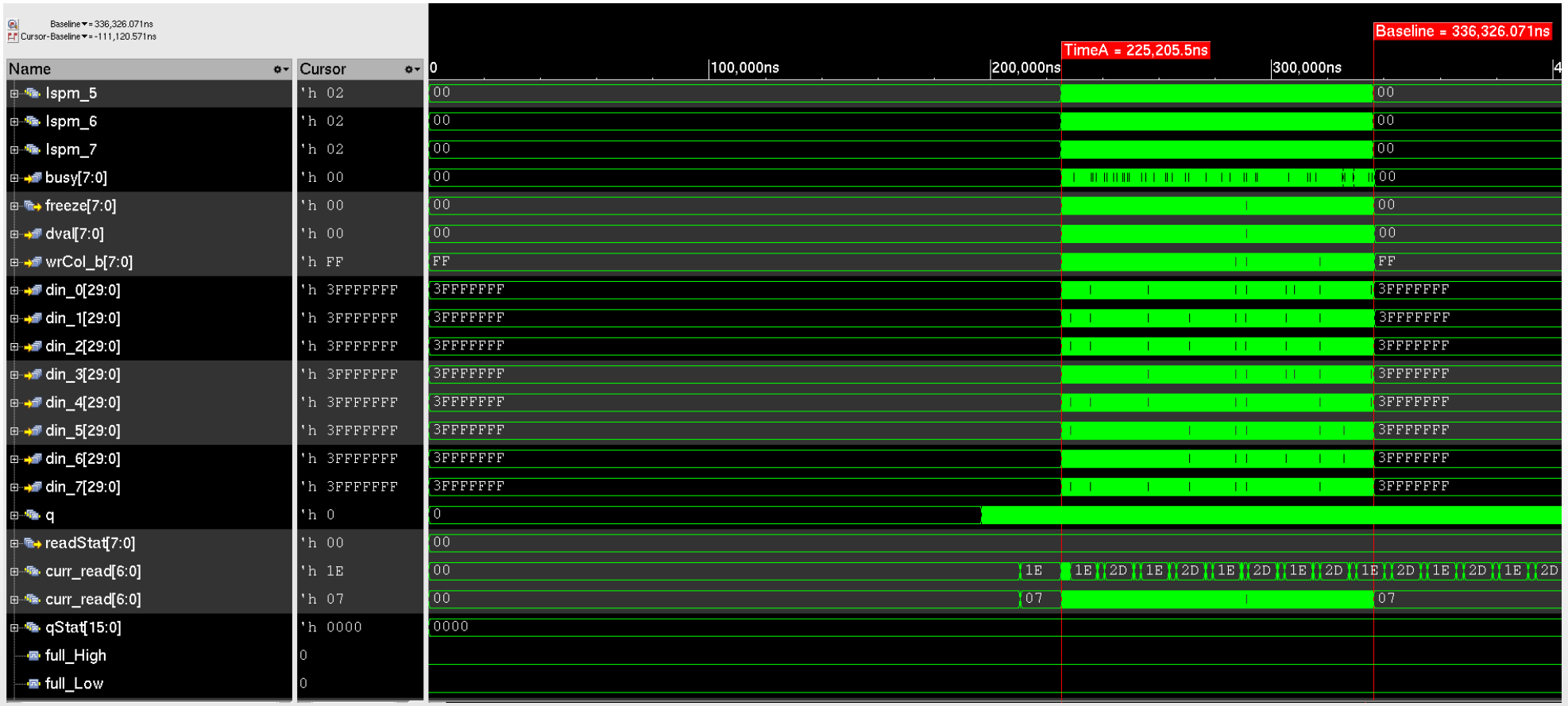
Less than 2 ns along the Pixel Column (post pnr simulation, TYP corner)

Start - New Orbit - Rollover



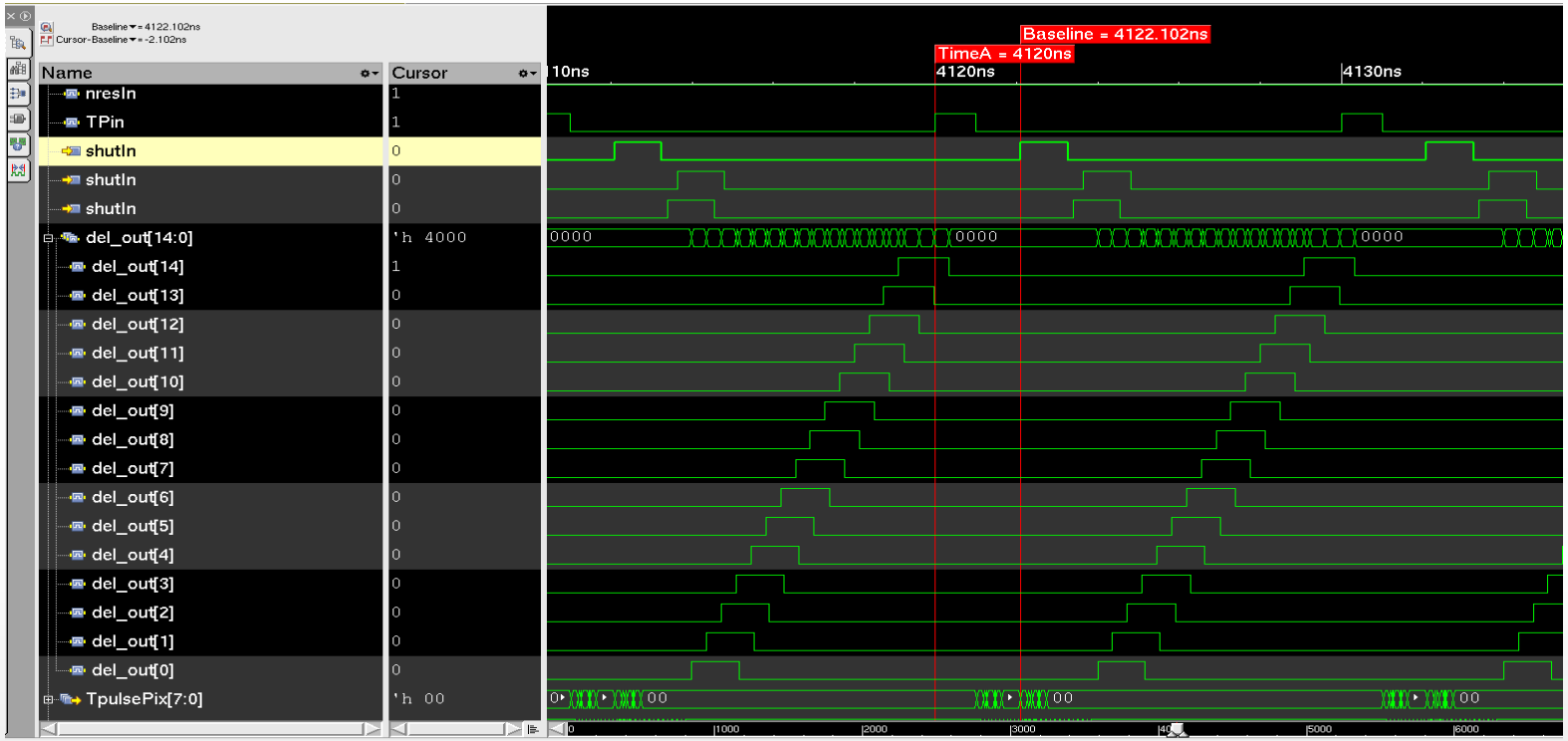
- After configuration:
  - Start Frame counter
  - Start State Machines
  - Write Header 0x1C1C1C1C
  - Write Frame Number
- Extra bit added here and forced by Rollover, Start or New Orbit request
- Read LSB FIFO until rollover or Start or New Orbit (MSB Coarse + 1 = 1) and FIFO LSB not Empty
- Wait for timeout (9-bit counter 2060 ns, it was 3200 ns in Alcor 0-1-2)
- Read MSB FIFO until rollover or Start or New Orbit (MSB Coarse + 1 = 1) and FIFO MSB not Empty
- Wait for timeout
- Each time writes Rollover code, Status (if enabled) CRC and Trailer

Data rates



- Data rates up to 16 MHz per column without loss
- Beware! The distribution is forced to cut off signals with width lower than 30 ns!

Test pulse distribution (TYP)



- External TP -> Shutter Pixel 7 Column 0 : 2.1 ns
- External TP -> Shutter Pixel 0 Column 0 : 3.67 ns
- External TP -> Shutter Pixel 0 Column 7 : 3.39 ns
- Row delta time : 1.53 ns
- Column delta time : 240 ps
- In pixel correction : 5.08 ns (360 ps each step)
- EoC correction (between columns) : 1.3 ns (each step 92 ps)

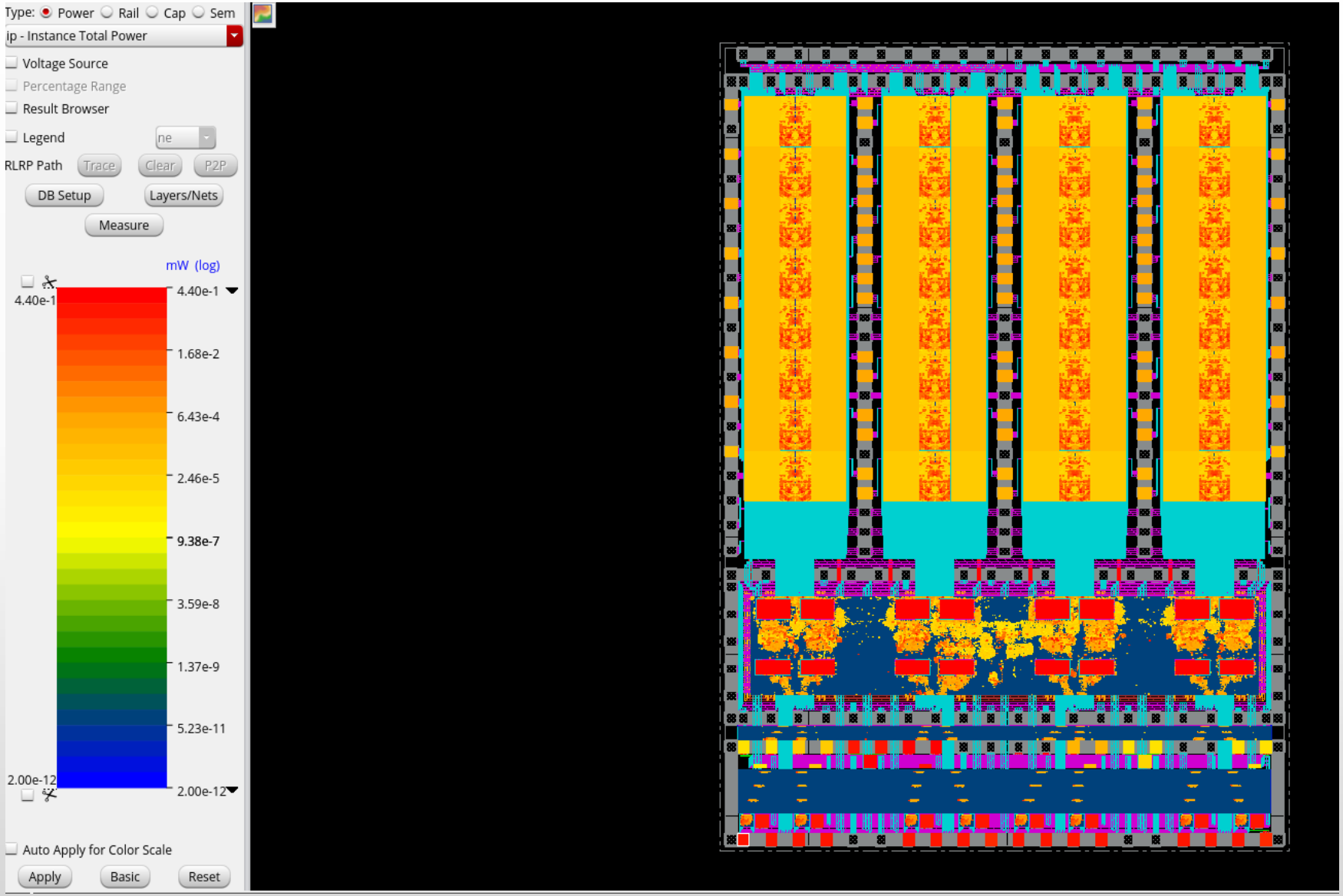
Radiation tolerance

- Pixel digital
  - Configuration registers: TMR with voting and self correction
  - FSMs: Hamming Code (Single Error Correction)
- EoC
  - Reset FSM: : TMR with voting and self correction (to add TMR at counters used by FSM)
  - Readout FSMs: Hamming Code (Single Error Correction)
- SPI:
  - Not yet!

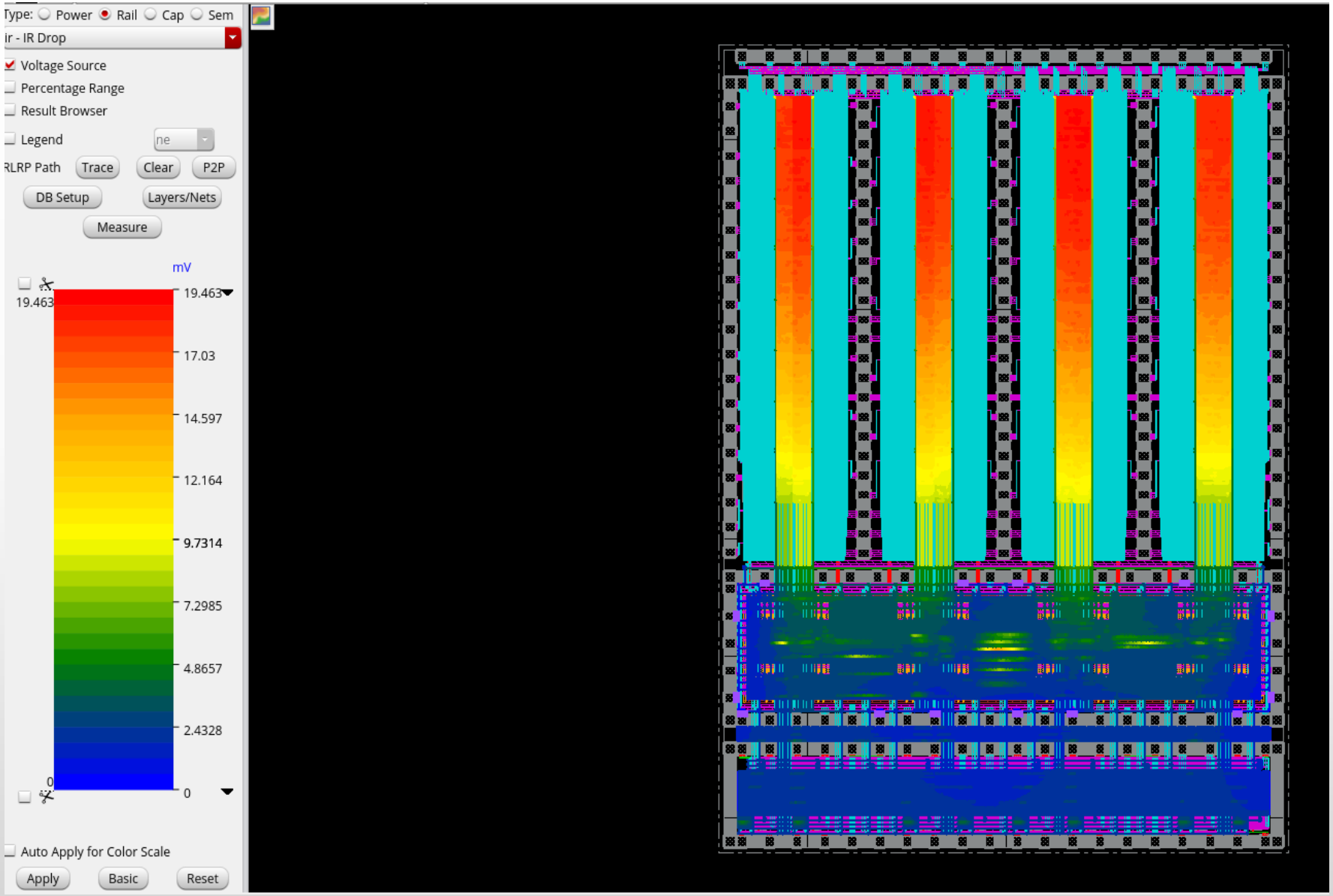
Power analysis

- Analysis done with VCD file form post pnr simulation
- DVDD/DGND (1.2 V core)
- Testbench with all pixels enabled and 10.84 MHz per column
- Total power consumption (core):
  - Total power 322 mW (200 mW internal 122 mW switching) (Alcor 0 : 87 mW, 63 +23, +270%)
  - EoC 31.6 mW (17.75 mW internal, 13.86 mW switching) (Alcor 0 : 9.71 mW +225%)
  - Pixel 4.37 mW (2.78 mW internal, 1.59 mW switching) (Alcor 0 : 2.31 mW +89%)
  - ddr_reg 1.14 mW (0.7 mW internal, 0.44 mW switching) (Alcor 0 : 0.74 mW +54%)
- Estimated power consumption full chip 1.2 W (with analogue and LVDS I/0)

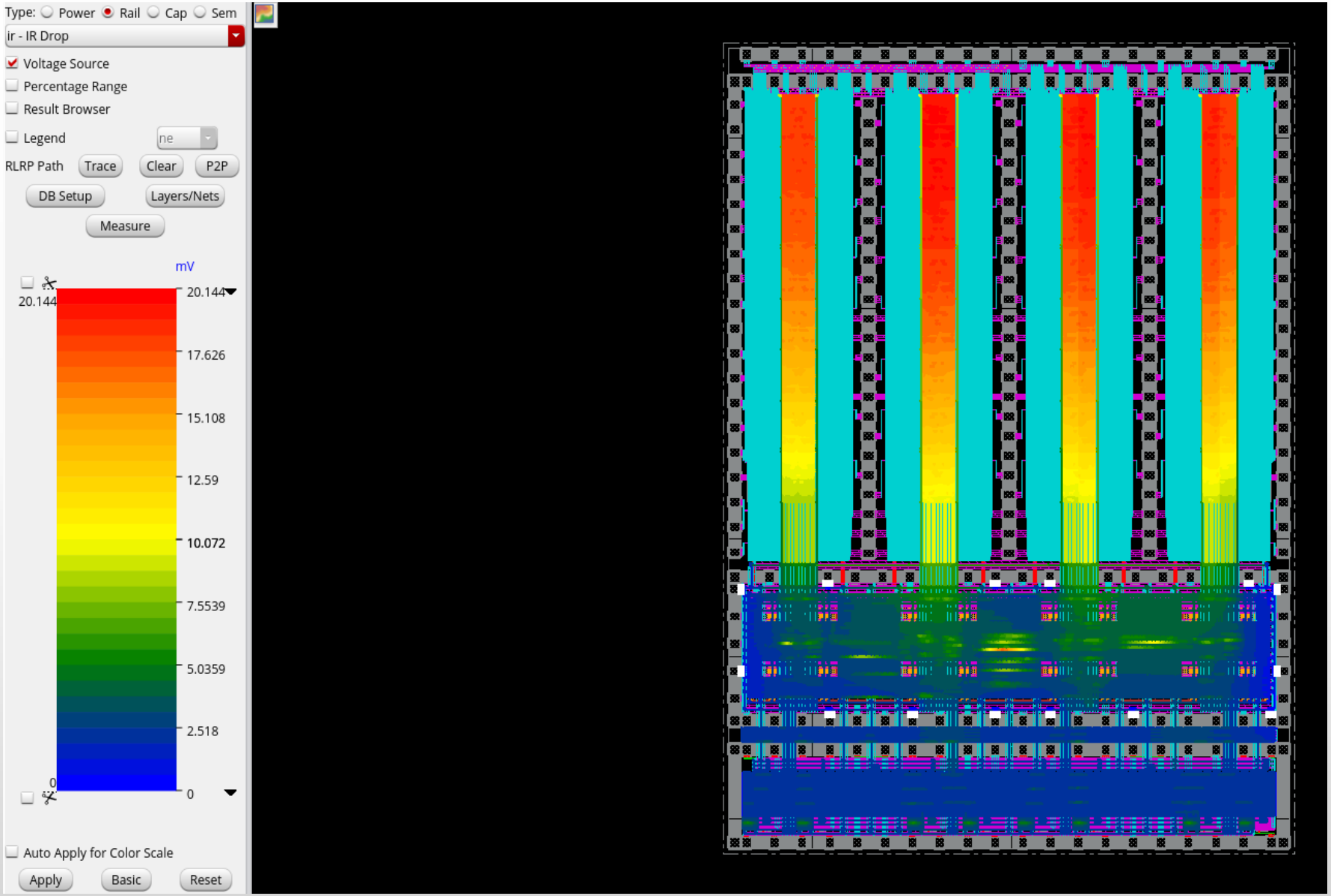
Instance power



DVDD IR drop


Type: Power Rail Cap Sem
ir - IR Drop
Voltage Source
Percentage Range
Result Browser
Legend
ne
RLRP Path
Trace
Clear
P2P
DB Setup
Layers/Nets
Measure
mV
19.463
19.463
17.03
14.597
12.164
9.7314
7.2985
4.8657
2.4328
0
0
Auto Apply for Color Scale
Apply
Basic
Reset

DGND drop


Type: Power Rail Cap Sem
ir - IR Drop
Voltage Source
Percentage Range
Result Browser
Legend
ne
RLRP Path
Trace
Clear
P2P
DB Setup
Layers/Nets
Measure
mV
20.144
20.144
17.626
15.108
12.59
10.072
7.5539
5.0359
2.518
0
0
Auto Apply for Color Scale
Apply
Basic
Reset

Thank you!