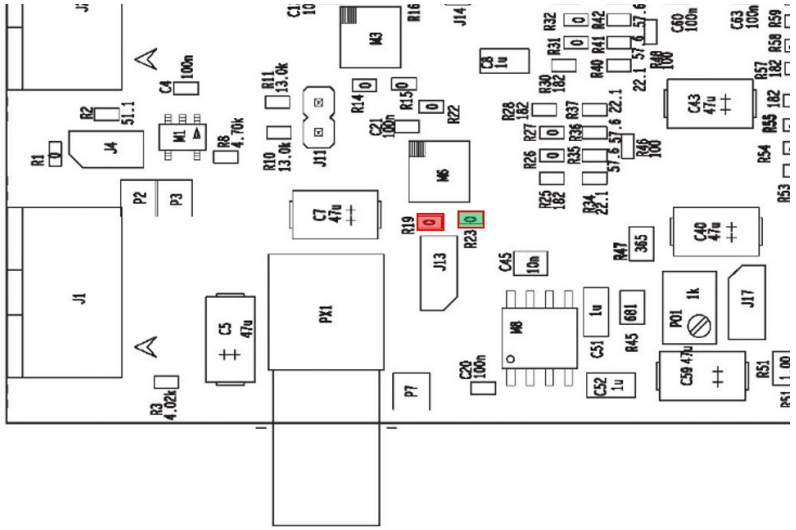
Recap

Switch R19 into R23



- Clock @40 MHz is sent to the chip from the FPGA
- Clock OUT not used for the deserializer
- Same configuration of the registers

1 OUTPUT LINES

```
20  fcaafcaafcaafcaafcaafcaafcaafcaa
21  fcaafcaafcaafcaafcaafcaafcaafcaa
22  fcaafcaafcaafcaafcaafcaafcaafcaa
23  fcaafcaafcaafcaafcaafcaafcaafcaa
24  fcaafcaafcaafcaafcaafcaafcaafcaa
25  fcaafcaafcaafcaafcaafcaafcaafcaa
26  fcaafcaafcaafcaafcaafcaafcaafcaa
27  fcaafcaafcaafcaafcaafcaafcaafcaa
28  fcaafcaafcaafcaafcaafcaafcaafcaa
29  fcaafcaafcaafcaafcaafcaafcaafcaa
30  fcaafcaafcaafcaafcaafcaafcaafcaa
```

2 OUTPUT LINES

```
20  21  fcaafcaafcaafcaafcaafcaafcaafcaa
21  22  fcaafcaafcaafcaafcaafcaafcaafcaa
22  23  fcaafcaafcaafcaafcaafcaafcaafcaa
23  24  fcaafcaafcaafcaafcaafcaafcaafcaa
24  25  fcaafcaafcaafcaafcaafcaafcaafcaa
25  26  fcaafcaafcaafcaafcaafcaafcaafcaa
26  27  fcaafcaafcaafcaafcaafcaafcaafcaa
27  28  fcaafcaafcaafcaafcaafcaafcaafcaa
28  29  fcaafcaafcaafcaafcaafcaafcaafcaa
29  30  fcaafcaafcaafcaafcaafcaafcaafcaa
30  31  fcaafcaafcaafcaafcaafcaafcaafcaa
31  32  fcaafcaafcaafcaafcaafcaafcaafcaa
32  33  fcaafcaafcaafcaafcaafcaafcaafcaa
33  34  fcaafcaafcaafcaafcaafcaafcaafcaa
```

```
fcaafcaafeacfe84fe84fe58fe58fe0d
fe05fe05fe00fe00fe00fe00fe00fe00
fe00fe00fe00fe00fe00fe00ff38fd38
fd38b300b3001ea05ea05ea0ab70ab70
a270e270e270fcaafcaafd39fd39fd39
70087008509840904090ac18ac182c68
3c603c60b268b26892b880b080b08570
8570bd3afd3afd3a15a815a8b6b8a6b0
a6b0fcaafcaafd3bfd3bfd3b72007200
5b505950595053d853d85fb84fb04fb0
```

Frame: 050d5884

```
caafcaafcaa
caafcaafcaa
```

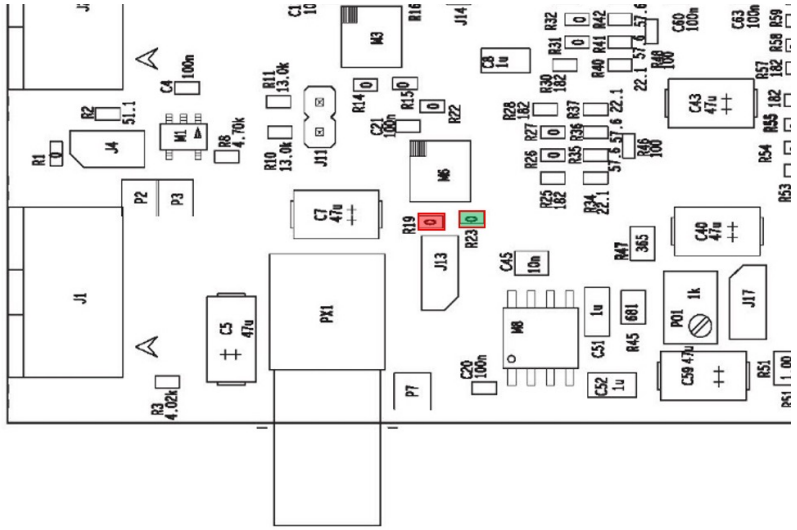
…About ten lines of IDLE words…

Frame: 050d5885

```
caafcaafcaa
caafcaafcaa
fcaafcaafd3cfd3cfd3c6b906b907358
335833585fe05fe07ea83ea83ea81b70
1b703ab878b878b8fcaafcaafd3dfd3d
fd3d35603560bf20ff00ff00054b054b
acaafcaafcaafcaafcaafcaafcaafcaa
fcaafcaafeadfe85fe85fe58fe58fe0d
fe05fe05fe00fe00fe00fe00fe00fe00
fe00fe00fe00fe00fe00fe00ff38fd38
fd384e404e40eb40b940b94086888688
8798879087904c984c98696829682968
3228322897e885e885e830b030b03330
73307330fcaafcaafd39fd39fd395388
```

New Configuration: rescue mode with R23

- Clock @40 MHz is sent to the chip from the FPGA
- Clock @320 MHz from outside (J11)
- Register configuration equal to the one for Rescue Mode



1 OUTPUT LINE

```
17    fcaafcaafcaafcaafcaafcaafcaafcaa
18    fcaafcaafcaafcaafcaafcaafcaafcaa
19    fcaafcaafcaafcaafcaafcaafcaafcaa
20    fcaafcaafcaafcaafcaafcaafcaafcaa
21    fcaafcaafcaafcaafcaafcaafcaafcaa
22    fcaafcaafcaafcaafcaafcaafcaafcaa
23    fcaafcaafcaafcaafcaafcaafcaafcaa
24    fcaafcaafcaafcaafcaafcaafcaafcaa
25    fcaafcaafcaafcaafcaafcaafcaafcaa
26    fcaafcaafcaafcaafcaafcaafcaafcaa
27    fcaafcaafcaafcaafcaafcaafcaafcaa
28    fcaafcaafcaafcaafcaafcaafcaafcaa
29    fcaafcaafcaafcaafcaafcaafcaafcaa
30    fcaafcaafcaafcaafcaafcaafcaafcaa
31    fcaafcaafcaafcaafcaafcaafcaafcaa
32    fcaafcaafcaafcaafcaafcaafcaafcaa
33    fcaafcaafcaafcaafcaafcaafcaafcaa
34    fcaafcaafcaafcaafcaafcaafcaafcaa
35    fcaafcaafcaafcaafcaafcaafcaafcaa
```

2 OUTPUT LINES

```
35    fcaafcaafcaafcaafcaafcaafcaafcaa
36    fcaafcaafcaafcaafcaafcaafcaafcaa
37    fcaafcaafcaafcaafcaafcaafcaafcaa
38    fcaafcaafcaafcaafcaafcaafcaafcaa
39    fcaafcaafcaafcaafcaafcaafcaafcaa
40    fcaafcaafcaafcaafcaafcaafcaafcaa
41    fcaafcaafcaafcaafcaafcaafcaafcaa
42    fcaafcaafcaafcaafcaafcaafcaafcaa
43    fcaafcaafcaafcaafcaafcaafcaafcaa
44    fcaafcaafcaafcaafcaafcaafcaafcaa
45    fcaafcaafcaafcaafcaafcaafcaafcaa
46    fcaafcaafcaafcaafcaafcaafcaafcaa
47    fcaafcaafcaafcaafcaafcaafcaafcaa
48    fcaafcaafcaafcaafcaafcaafcaafcaa
49    fcaafcaafcaafcaafcaafcaafcaafcaa
50    fcaafcaafcaafcaafcaafcaafcaafcaa
51    fcaafcaafcaafcaafcaafcaafcaafcaa
52    fcaafcaafcaafcaafcaafcaafcaafcaa
53    fcaafcaafcaafcaafcaafcaafcaafcaa
```

1 OUTPUT LINE

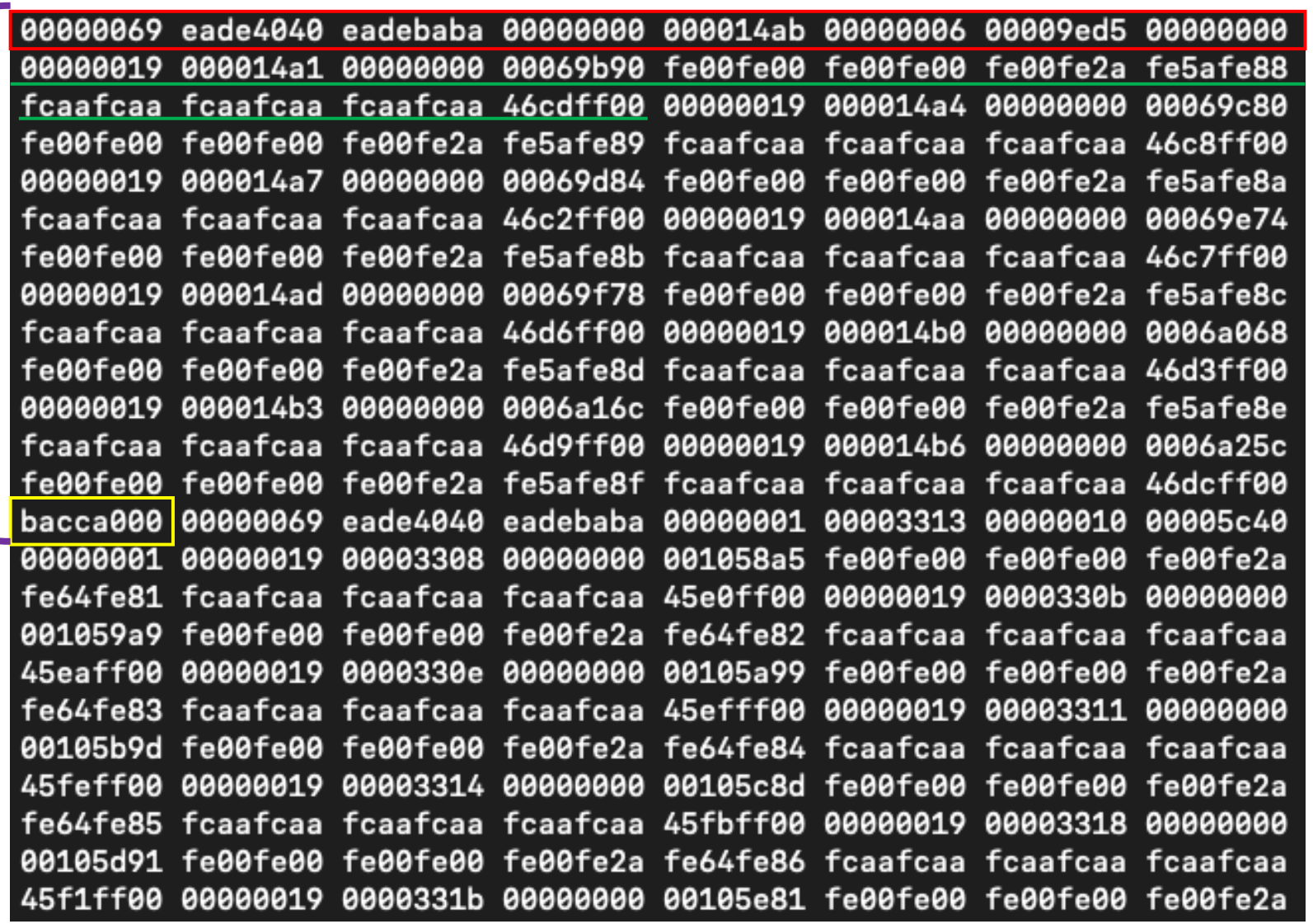
```
122    fcaafcaafcaafcaafcaafcaafcaafcaa
123    fcaafcaafcaafcaafcaafcaafcaafcaa
124    fe00fe00fe00fe00fe00fe9ffe7efee0
125    fcaafcaafcaafcaafcaafcaa7075ff00
126    fcaafcaafcaafcaafcaafcaafcaafcaa
127    fcaafcaafcaafcaafcaafcaafcaafcaa
128    fcaafcaafcaafcaafcaafcaafcaafcaa
129    fcaafcaafcaafcaafcaafcaafcaafcaa
130    fcaafcaafcaafcaafcaafcaafcaafcaa
131    fcaafcaafcaafcaafcaafcaafcaafcaa
132    fcaafcaafcaafcaafcaafcaafcaafcaa
133    fcaafcaafcaafcaafcaafcaafcaafcaa
134    fcaafcaafcaafcaafcaafcaafcaafcaa
135    fcaafcaafcaafcaafcaafcaafcaafcaa
136    fe00fe00fe00fe00fe00fe9ffe7efee1
137    fcaafcaafcaafcaafcaafcaa7070ff00
138    fcaafcaafcaafcaafcaafcaafcaafcaa
139    fcaafcaafcaafcaafcaafcaafcaafcaa
140    fcaafcaafcaafcaafcaafcaafcaafcaa
```

2 OUTPUT LINES

```
267    fcaafcaafcaafcaafcaafcaafcaafcaa
268    fe00fe35feeefe6cfe00fe00fe00fe00
269    fcaafcaa482eff00fcaafcaafcaafcaa
270    fcaafcaafcaafcaafcaafcaafcaafcaa
271    fcaafcaafcaafcaafcaafcaafcaafcaa
272    fcaafcaafcaafcaafcaafcaafcaafcaa
273    fcaafcaafcaafcaafcaafcaafcaafcaa
274    fcaafcaafcaafcaafcaafcaafcaafcaa
275    fcaafcaafcaafcaafcaafcaafcaafcaa
276    fcaafcaafcaafcaafcaafcaafcaafcaa
287    fcaafcaafcaafcaafcaafcaafcaafcaa
288    fcaafcaafcaafcaafcaafcaafcaafcaa
289    fcaafcaafcaafcaafcaafcaafcaafcaa
290    fcaafcaafcaafcaafcaafcaafcaafcaa
291    fcaafcaafcaafcaafcaafcaafcaafcaa
292    fcaafcaafcaafcaafcaafcaafcaafcaa
293    fe00fe35feeefe6dfe00fe00fe00fe00
294    fcaafcaa482bff00fcaafcaafcaafcaa
295    fcaafcaafcaafcaafcaafcaafcaafcaa
```

Readout of the Events

- Move to a configuration more like the final one
- Spy Buffer used only for debug
- Readout of the events
  - an event correspond to a trigger
  - Each event can be formed by more than one frame



1 Event
Start of the event
Frame
End of the event

Next step

- Implementation of a Firmware that can handle 2 chip (seems to work)
- Decoding the data ⟶ move to hits
- Work on pixels threshold
- Re-design of the DAQ board