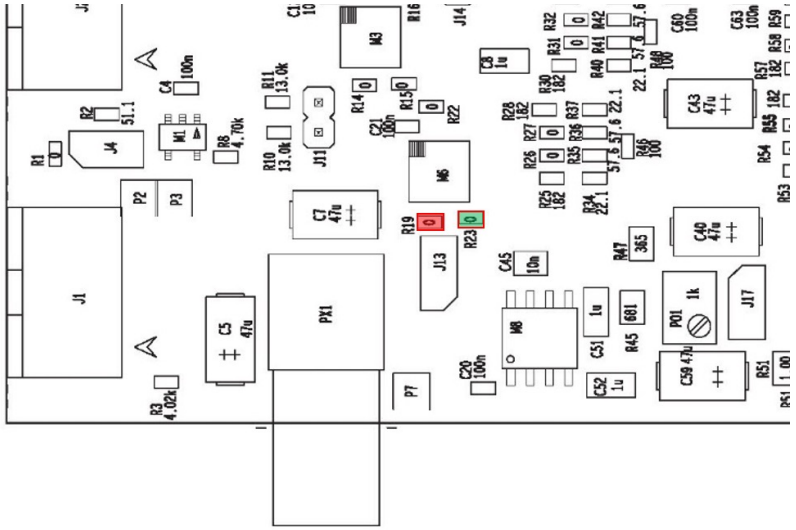
Recap

Switch R19 into R23



- Clock @40 MHz is sent to the chip from the FPGA
- Clock OUT not used for the deserializer
- Same configuration of the registers

1 OUTPUT LINES

```
20  fcaafcaafcaafcaafcaafcaafcaafcaa
21  fcaafcaafcaafcaafcaafcaafcaafcaa
22  fcaafcaafcaafcaafcaafcaafcaafcaa
23  fcaafcaafcaafcaafcaafcaafcaafcaa
24  fcaafcaafcaafcaafcaafcaafcaafcaa
25  fcaafcaafcaafcaafcaafcaafcaafcaa
26  fcaafcaafcaafcaafcaafcaafcaafcaa
27  fcaafcaafcaafcaafcaafcaafcaafcaa
28  fcaafcaafcaafcaafcaafcaafcaafcaa
29  fcaafcaafcaafcaafcaafcaafcaafcaa
30  fcaafcaafcaafcaafcaafcaafcaafcaa
```

2 OUTPUT LINES

```
20  21  fcaafcaafcaafcaafcaafcaafcaafcaa
21  22  fcaafcaafcaafcaafcaafcaafcaafcaa
22  23  fcaafcaafcaafcaafcaafcaafcaafcaa
23  24  fcaafcaafcaafcaafcaafcaafcaafcaa
24  25  fcaafcaafcaafcaafcaafcaafcaafcaa
25  26  fcaafcaafcaafcaafcaafcaafcaafcaa
26  27  fcaafcaafcaafcaafcaafcaafcaafcaa
27  28  fcaafcaafcaafcaafcaafcaafcaafcaa
28  29  fcaafcaafcaafcaafcaafcaafcaafcaa
29  30  fcaafcaafcaafcaafcaafcaafcaafcaa
30  31  fcaafcaafcaafcaafcaafcaafcaafcaa
31  32  fcaafcaafcaafcaafcaafcaafcaafcaa
32  33  fcaafcaafcaafcaafcaafcaafcaafcaa
33  34  fcaafcaafcaafcaafcaafcaafcaafcaa
```

```
fcaafcaafeacfe84fe84fe58fe58fe0d
fe05fe05fe00fe00fe00fe00fe00fe00
fe00fe00fe00fe00fe00fe00ff38fd38
fd38b300b3001ea05ea05ea0ab70ab70
a270e270e270fcaafcaafd39fd39fd39
70087008509840904090ac18ac182c68
3c603c60b268b26892b880b080b08570
8570bd3afd3afd3a15a815a8b6b8a6b0
a6b0fcaafcaafd3bfd3bfd3b72007200
5b505950595053d853d85fb84fb04fb0
```

Frame: 050d5884

```
caafcaafcaa
caafcaafcaa
```

…About ten lines of IDLE words…

Frame: 050d5885

```
caafcaafcaa
caafcaafcaa
fcaafcaafd3cfd3cfd3c6b906b907358
335833585fe05fe07ea83ea83ea81b70
1b703ab878b878b8fcaafcaafd3dfd3d
fd3d35603560bf20ff00ff00054b054b
acaafcaafcaafcaafcaafcaafcaafcaa
fcaafcaafeadfe85fe85fe58fe58fe0d
fe05fe05fe00fe00fe00fe00fe00fe00
fe00fe00fe00fe00fe00fe00ff38fd38
fd384e404e40eb40b940b94086888688
8798879087904c984c98696829682968
3228322897e885e885e830b030b03330
73307330fcaafcaafd39fd39fd395388
```

Deserializer update

Implementation of a phase for each output line:

- The register that monitors the output line never counts the expected number of idle words
- When we set the right phase ⟶ Output file without errors in the decodification of the idle word

```
36    fcaafcaafcaafcaafcaafcaafcaafcaa
37    fcaafcaafcaafcaafcaafcaafcaafcaa
38    fcaafcaafcaafcaafcaafcaafcaafcaa
39    fcaafcaafcaafcaafcaafcaafcaafcaa
40    fcaafcaafcaafcaafcaafcaafcaafcaa
41    fcaafcaafcaafcaafcaafcaafcaafcaa
42    fcaafcaafcaafcaafcaafcaafcaafcaa
43    fcaafcaafcaafcaafcaafcaafcaafcaa
44    fcaafcaafcaafcaafcaafcaafcaafcaa
45    fcaafcaafcaafcaafcaafcaafcaafcaa
46    fcaafcaafcaafcaafcaafcaafcaafcaa
47    fcaafcaafcaafcaafcaafcaafcaafcaa
48    fcaafcaafcaafcaafcaafcaafcaafcaa
49    fcaafcaafcaafcaafcaafcaafcaafcaa
50    fcaafcaafcaafcaafcaafcaafcaafcaa
```

Some examples of outputs

1 OUTPUT LINE

```
 39    fcaafcaafcaafcaafcaafcaafcaafcaa
 40    fe00fe00fe00fe00fe00fe1bfea2fec4
 41    fcaafcaafcaafcaafcaafcaafcaafcaa
 42    fe00fe00fe00fe00fe1bfea2fec4fcaa
 43    fcaa43feff0052a8fd3d6580fd3bfe00
 44    fe00fe00fe00fe00fe1bfea2fec5fcaa
 45    fea2fec5fcaafcaa43feff0052a8fd3d
 46    3d88fd39fe00fe00fe00fe00fe00fe1b
 47    fe00fe00fe00fe00fe1bfcaafcaa2e20
 48    fd3bfcaa5d282e2075083d88fd39fe00
 49    fe00fcaafcaafcaafcaafcaafcaa8fc8
 50    fcaa8fc8fd3bfcaa5d282e2075083d88
 51    fcaafcaafcaafcaafcaafcaafcaafcaa
```

```
129    fcaafcaafcaafcaafcaafcaafcaafcaa
130    4db044585e88fd3b3b386f604090fd39
131    fd3b3b386f60fcaafcaa19821b70fd3c
132    fcaa1982ff001b70fd3c4db044585e88
133    fe00fe00fe1bfea2fec8fcaafcaafcaa
134    fcaafcaafcaa1982ff001b704db0fe00
135    fe00fe00fe00fe00fe1bfea2fec8fcaa
136    fd39fcaac5b07868fd38a838fd0cfe00
137    fcaac5b07868fd38fe00fe1bfea29420
138    fcaafcaafcaafcaafcaafcaa9420fd39
139    9420fd39fcaac5b07868fd38a838fd0c
140    fcaafcaafcaafcaafcaafcaafcaafcaa
141    fcaafcaafcaafcaafcaafcaafcaafcaa
```

2 OUTPUT LINES

```
72    fcaafcaafcaafcaafeaffcaafeaffcaa
73    fcaafcaafcaafcaafeaefcaafeaffcaa
74    fcaafcaafe9bfcaafe00fcaafe00fcaa
75    fe9bfcaafcaafcaafcaafeaefcaafcaa
76    fcaafcaa583bfe46fcaafeaffcaafeaf
77    ff00feb9fcaafcaafeaafeaefcaafeaf
78    fcaafcaafcaafcaafeaefe00feaefe00
79    fcaafcaafcaafcaafeaafcaafeaefcaa
80    fcaafcaafcaafcaafcaafcaafcaafcaa
81    fcaafcaafcaafcaafcaafeaafcaafcaa
```

```
448    fcaafcaafcaafcaafeaefcaafeaffcaa
449    fcaafcaafcaafcaafe00fcaafe00fcaa
450    fe46fcaafcaafcaafcaafeaefcaafcaa
451    fcaafcaa589efd38fcaafeaffcaafeaf
452    ff00fe00feb9fcaafcaafeaefcaafeaf
453    fcaafcaafcaafcaafcaafe00feaafe00
454    fcaa589efcaafcaafcaafcaafcaafcaa
455    fcaafcaafcaafcaafcaafcaafcaafcaa
456    fcaafcaafcaafcaafeaffcaafeaefcaa
```