### Data readout: rescue clock mode

Last check point: IDLE words read with ONE output line and saved in the spy buffer.

#### Now...:

- We are able to control the "START" and the "STOP" of the chip
- We find the Header word and the Frame Counter into the data saved into spy buffer
- We introduce the re-alignment of the PHASE
- Readout work "well" only with ONE output line
- Odd Output lines do not work (we don't know why)

70 fcaafcaafcaafcaafcaafcaa 71 fcaafcaafcaafcaafcaafcaa 72 fcaafcaafcaafcaafcaafcaa 73 fcaafcaafcaafcaafcaafcaa 74 fcaafcaafefefe12fe38fe01fe01fc01 75 fc01fc01fa743c01fa76f81c6ac0fcab 76 fc02cc0bf2abf2abf2abf3ffe577e557 77 e557e557e557e557fcaafcaafcaa 78 fcaafcaafcaafcaafcaafcaa 79 fcaafcaafcaafcaafcaafcaa 80 fcaafcaafcaafcaafcaafcaa 81 fcaafcaafcaafcaafcaafcaafcaa 82 fcaafcaafcaafcaafcaafcaafcaa 83 fcaafcaafcaafcaafcaafcaafcaa 84 fcaafcaafcaafcaafcaafcaafcaa 85 fcaafcaafcaafcaafcaafcaafeff 86 fe12fe71fe01fe00fe00fe00fe00fd3a 87 3d2cfe9e0fc8fd3f30b9ff005987fd55 88 fcd5f955fe55fc4bfe57f95bfc6bf8ab 89 f157f95fcb5f8abf357e557caafcaafc 90 aafcaafcaafcfcaafcaafcaafeff 91 7e557e557e557e557e57ff2abf2abf2a 92 bf2afcaafcaafcaafcaafcaafcaa 93 fcaafcaafcaafcaafcaafcaa 94 fcaafcaafcaafcaafcaafcaa 95 fcaafcaafcaafcaafcaafcaa 96 fcaafcaafcaafcaafcaafcaa 97 fcaafcaafcaafcaafcaafcaa 98 fcaafcaafcaafcaafcaafe00fe13 99 fe71fe01fe00fe00fe00fe00fd3b3b48 100 fe9e0db9ff00b769f9abe357fc03f84f 101 fb8ff00ff007e00fe00fe00fd388180c 8489d8cfba8fcaafd3942bc7eaafcaaf 102 caafcaafcaafcaafcaaffcaafcaa 103

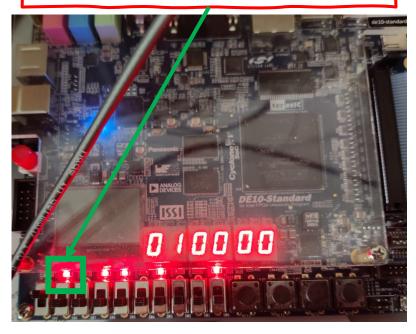
## Data readout: PLL mode

|                 |      |       | SYNC_IN_N SLVS pags   |
|-----------------|------|-------|---|
| SEL_START       | 2-1  | 0     | Start mode selection: Automatic: 0 (by default after PLL locked) Software: 1 (by sending 03 to INSTR CMDID see section 2 page 10) External: 2 or 3 (via START_IN_P and START_IN N SLVS pad) |
| SEL_CLOCK       | 0    | 0     | Clock selection:  Main @ 40 MHz (CLK_P and CLK_N SLVS pad): 0  Rescue @ 320 MHz <sup>4</sup> (CLKRESCUE_P CLKRESCUE_N SLVS pad): 1  |
| Name            | Bits | Reset | Description   |
| Not Used        | 7    | 0     |   |
| EN_ LOCKPLL     | 6    | 0     | Enable LOCKPLL pad  |
| EN_CLKPLL       | 5    | 0     | Enable CLKPLL_P CLKPLL_N SLVS pad   |
| TRIM_ REFCURPLL | 4-2  | 4     | Trimming bits for PLL current reference   |
| DIS_PLL_LDO     | 1    | 0     | Disable low-dropout PLL regulator (when disable VCO powered through AVDD and AVSS)  |
| EN_PLL_VCO      | 0    | 1     | Enable VCO  |
| Name            | Bits | Reset | Description   |
| Not Used        | 7    | 0     |   |
| GAIN            | 6-3  | 7     | Gain of current comparator to detect PLL lock from phase comparator   |
| THRESHOLD       | 2-0  | 0     | Threshold of current comparator to detect PLL lock from phase   |

| Name              | Bits | Reset | Description  |
|-------------------|------|-------|--|
| EN_CLKRESCUE_TERM | 7    | 0     | Enable rescue clock (320 MHz) SLVS 100 Ω termination       |
| EN_CLKSER         | 6    | 0     | Enable output clock serializer (160 MHz) test option       |
| EN_CUSTOM_FLV     | 5    | 0     | Enable custom fill level for elastic buffer test option    |
| EN_CUSTOM_BW      | 4    | 0     | Enable custom bandwidth for frame generator test option    |
| EN_PATTERN        | 3    | 0     | Enable pattern for serializer test mode                    |
| EN_PULSEINJ       | 2    | 0     | Enable external pulse injection test option                |
| EN_PIXELMASK      | 1    | 1     | Enable Pixel Masked (1) or Pulsed (0) mode for pixel array |
| EN_MFE            | 0    | 0     | Enable Multi Frame Emulator test mode                      |

comparator

## Now the PLL is locked !!!



Scan to find the right value

## Data readout: PLL mode

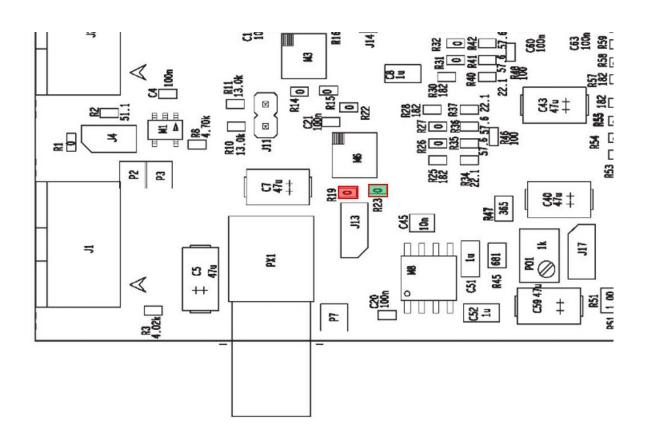
#### Same results as with the rescue clock:

- Only IDLE words when the chip is in STOP
- Frame when it is in START

```
47
      fcaafcaafcaafcaafcaafcaafcaa
48
      fcaafe2afe7ffe77fe7ffe2afe2afe2a
49
     fe2afeaafcaafcaafcaafcaafcaa
50
     fec6fe06fe5cfe03fe00fe00fe00fe00
51
     ff007ffdfc7dfceefceafcaafcaa
52
     fcaafcaafcaafcaafceafcfffcea
53
     fcaafcaafcaafcaafcaafcaafcaa
54
     fcaafcaafcaafcaafcaafcaafcaa
     fcaafcaafcaafcaafcaafcaafcaa
55
56
     fcaafcaafcaafcaafcaafcaafcaa
57
     fcaafcaafcaafcaafcaafcaafcaa
58
     fcaafcaafcaafcaafcaafcaafcaa
59
     fcaafcaafcaafcaafcaafcaafcaa
60
     fcaafcaafcaafcaafeaafe2afe3a
     fe2afe2afeaafeaafeaafeaafcaa
61
62
     fec7fe06fe5cfe03fe00fe00fe00fe00
     ff00577ffcaafceffcfffc55fcfffcaa
63
64
     fcaafcaafcaafcaafceafcfffcff
65
      fcfffc55fc7ffceafcaafcaafcaafcaa
     fcaafcaafcaafcaafcaafcaafcaa
67
     fcaafcaafcaafcaafcaafcaafcaa
68
     fcaafcaafcaafceffcaafcaafcaa
      fcaafcaafcaafcaafcaafcaafcaa
     fcaafcaafcaafcaafcaafcaafcaa
71
     fcaafcaafcaafcaafcaafcaafcaa
     fcaafcaafcaafcaafcaafcaafcaa
73
      fcaafcaafeaafe2afe2afeaafe2afe2a
74
     fe2afe2afeaafcaafcaafcaafcaa
     fec8fe06fe5cfe03fe00fe00fe00fe00
75
     ff00775dfcaafcaafcaafcaafcaa
      fcaafcaafceefcfffcfffceafcaa
      fcaafcaafcaafcaafcaafcaafcaa
```

# Next Step...

Switch R19 into R23 to remove the external clock and try again to lock the PLL



- Clock @40 MHz is sent to the chip from the FPGA
- Clock OUT not used for the deserializer
- Same configuration of the registers

# First attempt

Clock IN @320 MHz → it is wrong! But the PLL is locked. No IDLE words in the Spy Buffer

# Second attempt

**Clock IN @40 MHz** → Right configuration

**IDLE word decoded correctly** → with 1 and 2 output lines

→ with 4, 2 or 3 output lines stop decoding the IDLE word

**Chip in START** 

- → words seem duplicated but it's recognizable the frame
- → with 2 output lines, some problems in the deserializer, but it's still recognizable the frame

# Some examples of outputs

#### fcaafcaafcaafcaa 1 OUTPUT LINES fcaafcaafcaafcaa rcaarcaarcaarcaa<mark>fcaafcaafcaafcaa</mark> 20 fcaafcaafcaafcaafcaafcaafcaa fcaafcaafcaafcaafcaafcaafcaa 21 22 fcaafcaafcaafcaafcaafcaafcaa 23 fcaafcaafcaafcaafcaafcaa 24 fcaafcaafcaafcaafcaafcaa 25 fcaafcaafcaafcaafcaafcaa 26 fcaafcaafcaafcaafcaafcaa 27 fcaafcaafcaafcaafcaafcaa 28 fcaafcaafcaafcaafcaafcaa 29 fcaafcaafcaafcaafcaafcaafcaa 30 fcaafcaafcaafcaafcaafcaa

| fcaafcaafeacfe84fe84fe58fe58fe0d |  |
|----------------------------------|--|
| fe05fe05fe00fe00fe00fe00fe00     |  |
| fe00fe00fe00fe00fe00fe00         |  |
| fd38b300b3001ea05ea05ea0ab70ab70 |  |
| a270e270e270fcaafcaafd39fd39fd39 |  |
| 70087008509840904090ac18ac182c68 |  |
| 3c603c60b268b26892b880b080b08570 |  |
| 8570bd3afd3afd3a15a815a8b6b8a6b0 |  |
| a6b0fcaafcaafd3bfd3bfd3b72007200 |  |
| 5b505950595053d853d85fb84fb04fb0 |  |
| Cromo: OFOdFOO4 caafcaafcaa      |  |
| Frame: 050d5884 caafcaafcaa      |  |

55 fcaafcaafcaafcaafcaafcaafcaa 56 fcaafcaafcaafcaafcaafcaa 57 fcaafe00fe00fe00fcaafcbefe9efe9e 58 fe00fe00fe00fe00fe51fe51fe17fe37 59 fe00fe00fe00fcaafe37fe00fe00ff00 60 fcaafcaafcaaff00ff0043fd43fd 61 fcaafcaafcaaeeaefcaafcaafcaa 62 fcaafcaafcaafcaafcaafcaafcaa 63 fcaafcaafcaafcaafcaafcaafcaa 64 fcaafcaafcaafcaafcaafcaafcaa fcaafcaafcaafcaa Frame:3717519e fcaafcaafcaafcaa

#### afcaafcaafcaafcaa 2 OUTPUT LINES

afcaafcaafcaa tcaatcaatcaatcaafcaafcaafcaa 21 fcaafcaafcaafcaafcaafcaafcaa 22 fcaafcaafcaafcaafcaafcaa 23 fcaafcaafcaafcaafcaafcaa 24 fcaafcaafcaafcaafcaafcaafcaa 25 fcaafcaafcaafcaafcaafcaafcaa 26 fcaafcaafcaafcaafcaafcaafcaa 27 fcaafcaafcaafcaafcaafcaafcaa 28 fcaafcaafcaafcaafcaafcaa 29 fcaafcaafcaafcaafcaafcaa 30 fcaafcaafcaafcaafcaafcaafcaa 31 fcaafcaafcaafcaafcaafcaa 32 fcaafcaafcaafcaafcaafcaa 33 fcaafcaafcaafcaafcaafcaa

...About ten lines of IDLE words...

...Many lines of IDLE words...

caafcaafcaa Frame: 050d5885 caafcaafcaa rcaarcaaruscruscrusco<mark>b906b907358</mark> 335833585fe05fe07ea83ea83ea81b70 1b703ab878b878b8fcaafcaafd3dfd3d fd3d35603560bf20ff00ff00054b054b acaafcaafcaafcaafcaafcaafcaa fcaafcaafeadfe85fe85fe58fe58fe0d fe05fe05fe00fe00fe00fe00fe00 fe00fe00fe00fe00fe00fe00ff38fd38 fd384e404e40eb40b940b94086888688 8798879087904c984c98696829682968 3228322897e885e885e830b030b03330 73307330fcaafcaafd39fd39fd395388

aafcaafcaafcaa Frame: 3717519f aafcaafcaafcaafcaa тсаатсаатсаатсааfcaafcaafcaa 114 fcaafcaafcaafcaafcaafcaafcaa 115 116 fcaafcaafcaafcaafcaafcaafcaa 117 fcaafcaafcaafcaafcaafcaafcaa 118 fcaafcaafcaafcaafcaafcaafcaa 119 fcaafcaafcaafe00fcaafcaafcaafcbf 120 fe00fe00fe00fe00fe9ffe9ffe51fe51 121 fe00fe00fe00fe00fe17fe37fe37fe00 122 fe00fcaafcaafcaafe00ff00ff00ff00 123 fcaafcaafcaa43f843f8eeaafcaa 124 fcaafcaafcaafcaafcaafcaafcaa 125 fcaafcaafcaafcaafcaafcaafcaa