MIMOSIS1 I²C controller

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1 Introduction

The purpose of this document is the description of the operation of the I²C controller of MIMOSIS1 which is used to read or write internal registers, instructions, configuration, monitors, and memories. The MIMOSIS1 has an I²C slave unit with the following features:

- Data transfer rates less than 1Mbits/s (Fast plus mode also called Fm+)
- 7-bits addressing scheme
- Single or multi-byte bus transactions

1.1 General description

MIMOSIS1 uses a subset of the 7-bits I²C address to initiate 9 different types of transactions. Consequently, the I²C address is divided in two parts:

- 3-bits chip identification called CHIPID (MSBs)
- 4-bits command identification called CMDID (LSBs)

The CHIPID is configured through 3 pull-down pads (CHIPID[2:0]) and allows to address several chips with one master. Each CMDID takes one 8-bits word as parameter. CMDID could be divided in four flavours:

- An instruction
- Set the 16-bits address of the internal registers, configuration, monitors, or memories
- Read or write the selected internal registers, configuration, monitors, or memories. The read or write operations could be direct or indirect
- Read or write the offset used for the indirect addressing

The Table 1 gives the purpose of the CMDID used in MIMOSIS1 controller. All the other variants are unused.

Table 1: Description of the CMDID used in MIMOSIS1 controller

Name	Value	Purpose
INSTR	1	Instruction (write only command)
ADD_MSB	2	MSB of the internal address mapping
ADD_LSB	3	LSB of the internal address mapping
WR	4	Data written at the address given by the concatenation of ADD_MSB and ADD_LSB registers
RD	5	Data read at the address given by the concatenation of ADD_MSB and ADD_LSB registers
WR_IND	6	Data written at the address given by the combination of the OFFSET with the concatenation of ADD_MSB and ADD_LSB registers. OFFSET register is also incremented at the end of the operation
RD_IND	7	Data read at the address given by the combination of the OFFSET with the concatenation of ADD_MSB and ADD_LSB registers. OFFSET register is also incremented at the end of the operation
WR_OFF	8	Write the value of the OFFSET register
RD_OFF	9	Read the value of the OFFSET register

1.2 Single and multi-byte transactions

MIMOSIS1 I²C slave unit is compatible with single or multi-byte transactions.

1.2.1 Single byte transactions

In single byte transactions, each command takes one 8-bits word as parameter in write or read mode. The INSTR command is in write only. When the INSTR command is read, MIMOSIS1 return 0. A typical I²C transaction for MIMOSIS1 is given by Figure 1.

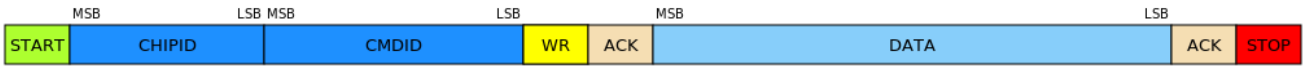

Figure 1: Typical I²C write transaction for MIMOSIS1

1.2.2 Multi-byte transactions

Two modes exist in multi-byte transactions, the non-incremental and the incremental mode. These modes are set by the pad ENINCR. The non-incremental mode (default mode) is selected by setting ENINCR to 0. The incremental mode is selected by setting ENINCR to 1.

1.2.2.1 Non-incremental mode

In non-incremental mode, multi-byte transactions operates as executing the same command with different parameters. For example, this mode could be used to read continuously a monitor register. This example is given by Figure 2.

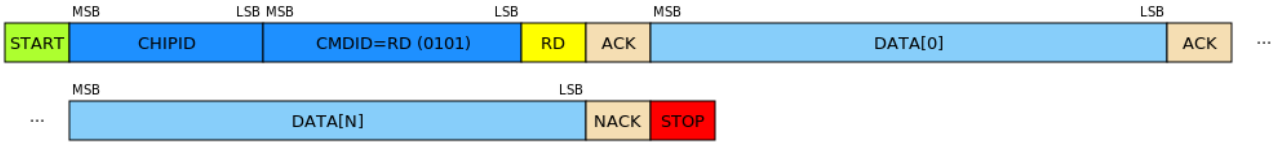

Figure 2: Multi-byte I²C transaction in non-incremental mode for MIMOSIS1

The equivalent transaction for this example in multi-byte with repetitive start is given by Figure 3.

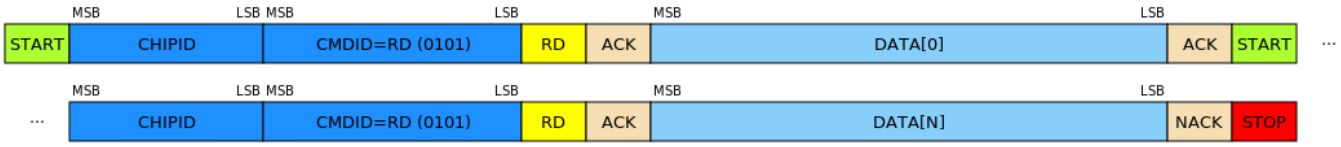

Figure 3: Equivalent multi-byte with repetitive start I²C transaction for the non incremental mode for MIMOSIS1

1.2.2.2 Incremental mode

In incremental mode, multi-byte transactions operates as executing the next command (i.e. the incremented CMDID) with each different parameters. For example, this mode could be used to set the address of the internal register and write a value to this register. This example is given by Figure 4.

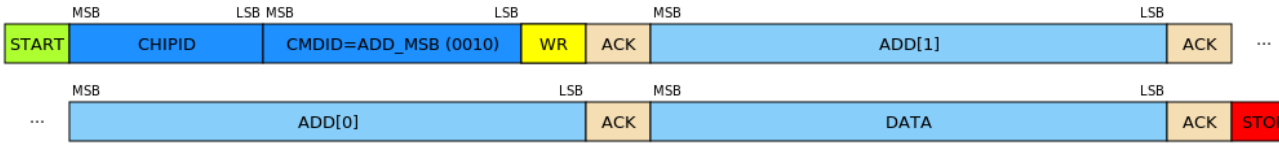

Figure 4: Multi-byte I²C transaction in incremental mode for MIMOSIS1

The equivalent transaction for this example in multi-byte with repetitive start is given by Figure 5.

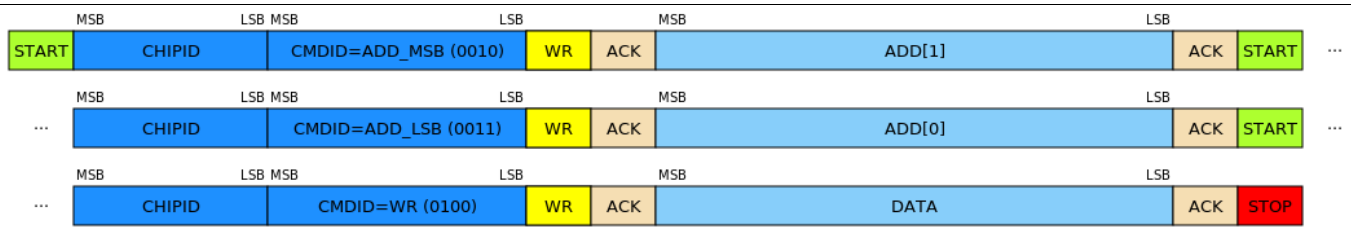

Figure 5: Equivalent multi-byte with repetitive start I²C transaction for the incremental mode for MIMOSIS1

1.3 Access to the internal registers

MIMOSIS1 has several internal registers and memories to configure, monitor, and test the chip. These internal registers and memories are accessible through a 16-bits address mapping. The 16-bits address mapping is set by the ADD_MSB CMDID for the 8 MSBs and by ADD_LSB CMDID for the 8 LSBs.

The selected internal register or memory could be read or write through the direct access or indirect access mode.

1.3.1 Direct access

The read direct access is done with the RD CMDID, and the write direct access is done with the WR CMDID. If the address mapping is not change the read or write operation is done on the same internal register.

1.3.2 Indirect access

The read indirect access is done with the RD_IND CMDID, and the write indirect access is done with the WR_IND CMDID. The address of the selected internal register is obtained by combining the address set through ADD_MSB and ADD_LSB CMDID, and the value of the OFFSET register. The combination of the address and the OFFSET register is given in section **Error! Reference source not found.**. The OFFSET register is accessible through the RD_OFF and WR_OFF CMDID. After each RD_IND or WR_IND CMDID, the value of the OFFSET register is incremented by 1. This mode could be used, for example, to configure all the DACs with one non-incremental transaction shown in Figure 6.

The combination of the incremental mode and indirect access could lead to unpredictable results.

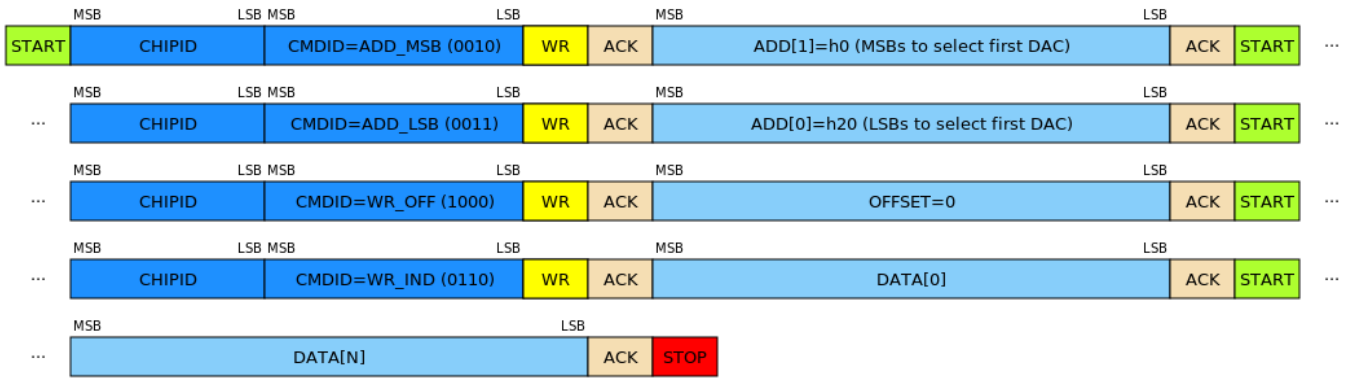

Figure 6: Full example of an I²C transaction to configure all DACs in indirect access mode

Figure 7 shows the equivalent I²C transaction to configure all the DACs with one non-incremental transaction in direct mode. In indirect access mode the transaction is 227-bits wide and in indirect mode the transaction is 628-bits wide.

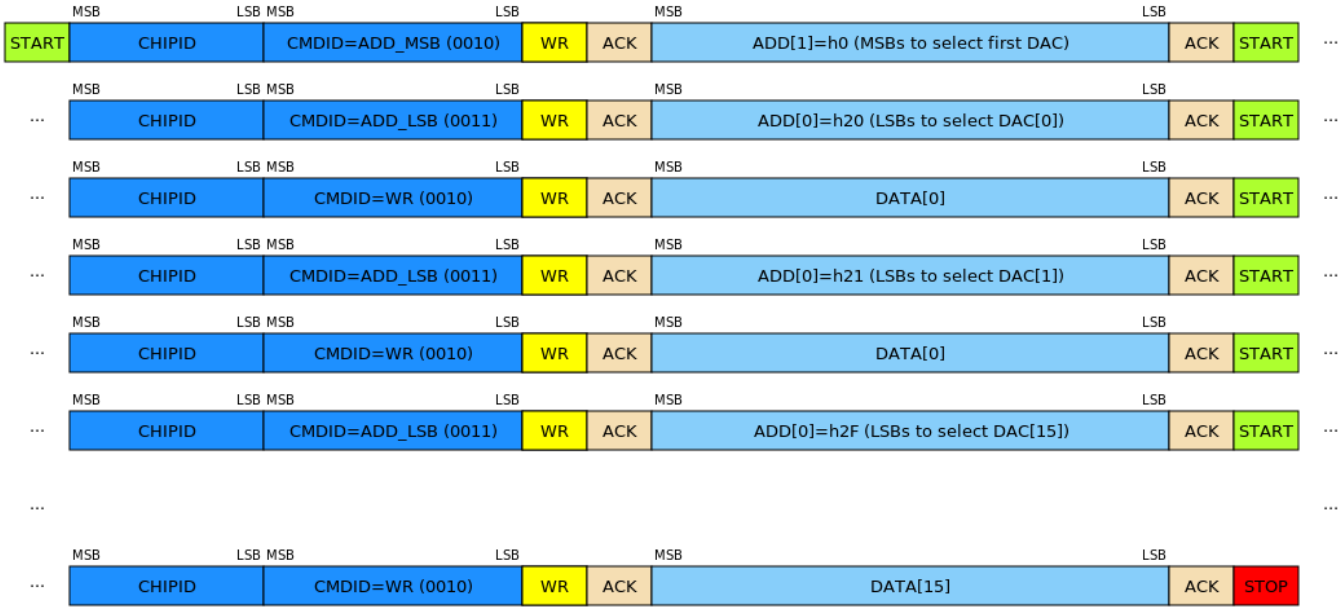

Figure 7: Full example of an equivalent I²C transaction to configure all DACs in direct access mode

The multi-byte I²C transaction is optional. All the multi-byte I²C transactions shown in this section could be replace by several single byte I²C transactions.

2 INSTR command identification

2.1 Introduction

The INSTR CMDID is used to send a command to MIMOSIS1. Two kinds of commands are available: set or reset one or several flags, to assert and deassert one or several reset.

2.2 Detailed description

Table 2 describes the available commands depending of the parameter given to INSTR CMDID.

Table 2: INSTR CMDID parameter decoding

Command	Code Hex	7	6	5	4	3	2	1	0
Set/Reset Flag Part 1	0-1F	0	0	0	X	X	X	X	X
Reset Start Chip (stop chip)	02	0	0	0	-	-	-	1	0
Set Start Chip (start chip)	03	0	0	0	-	-	-	1	1
Reset MASK_PULSE_DATA	04	0	0	0	-	-	1	-	0
Set MASK_PULSE_DATA	05	0	0	0	-	-	1	-	1
Set/Reset Flag Part 2	20-3F	0	0	1	X	X	X	X	X
Unselect Left Columns	22	0	0	1	-	-	-	1	0
Select Left Columns	23	0	0	1	-	-	-	1	1
Unselect Right Columns	24	0	0	1	-	-	1	-	0
Select Right Columns	25	0	0	1	-	-	1	-	1
Unselect Top Rows	28	0	0	1	-	1	-	-	0
Select Top Rows	29	0	0	1	-	1	-	-	1
Unselect Bottom Rows	30	0	0	1	1	-	-	-	0
Select Bottom Rows	31	0	0	1	1	-	-	-	1
Reset Register Part 1	80-9F	1	0	0	X	X	X	X	X
Reset General Configuration[1]	81	1	0	0	-	-	-	-	1
Reset DAC[1]	82	1	0	0	-	-	-	1	-
Reset Sequencer Configuration[1]	84	1	0	0	-	-	1	-	-
Reset Monitoring[2]	88	1	0	0	-	1	-	-	-
Reset Pixel Control[1]	90	1	0	0	1	-	-	-	-
Reset Register Part 2	A0-BF	1	0	1	X	X	X	X	X
Reset Analogue Pixel Selection[1]	A1	1	0	1	-	-	-	-	1
Reset Readout Test Configuration[1]	A2	1	0	1	-	-	-	1	-
Reset Flags[1]	B0	1	0	1	1	-	-	-	-
Reset Unit	C0-DF	1	1	0	X	X	X	X	X
Reset Readout[1]	C1	1	1	0	-	-	-	-	1
Reset PLL[2]	C2	1	1	0	-	-	-	1	-
Reset PLL Bandgap[2]	C4	1	1	0	-	-	1	-	-
Reset Bandgap[2]	C8	1	1	0	-	1	-	-	-
Reset Clock Divider[1]	D0	1	1	0	1	-	-	-	-
Reset Register and Unit	E0-FF	1	1	1	X	X	X	X	X
Reset Global	E0	1	1	1	-	-	-	-	-

[1] The reset is also done by Reset Global (hE0 command), Power On Reset (POR), and RTSB pad

[2] The reset is not affected by Reset Global (hE0 command), and RTSB pad. The only ways to send a reset are with INSTR CMDID, or with the Power On Reset (POR) after a power shutdown.

2.3 INSTR CMDID parameter decoding

The parameter given to the INSTR CMDID is decoded as follows. Bit 7 control the kind of command, set or reset one or more flags (value equal to 0) or to assert and deassert reset (value equal to 1). Bits 6 and 5 are used to group by section. Bits 4 to 0 depend of the command type.

2.3.1 Set or reset flags

When set or reset flags command is selected (with bit 7 equal to 0). Bits 4 to 0 are used as follows. Bits 4 to 1 are used to mask on which flags the written value is applied. If the mask is set to 1 the value is written otherwise the previous value is kept. Several flags of the same section could be written at once. Bit 0 gives the value to write to the flags selected with bits 4 to 1. Table 3 gives the 6 different flags used in MIMOSIS1.

For example to select all the left part of the pixel matrix, the user needs to select the left columns, the top, and the bottom rows. Consequently, the parameter given to the INSTR CMDID is b00111011 or h3B. Explanation: bit 7 set to 0 to select flag modification function, bits 6-5 set to 01 to select pixel array selection section, bits 4-1 set to 1101 to select bottom rows, top rows, and left columns, bit 0 to set the flags to 1.

Table 3: INSTR CMDID Flags description

Flag	Section (bits 6-5)	Mask bit	Function
Start Chip	0	1	To Start (1) or Stop (1) the sequencer
MASK_PULSE_DATA	0	2	Value written to the pixel in mask or pulse mode (see section 7 page 27)
Left Columns	1	1	Select (1) or Unselect (0) half of the matrix columns (left part) (see section 7 page 27)
Right Columns	1	2	Select (1) or Unselect (0) half of the matrix columns (right part) (see section 7 page 27)
Top Rows	1	3	Select (1) or Unselect (0) half of the matrix rows (top part) (see section 7 page 27)
Bottom Rows	1	4	Select (1) or Unselect (0) half of the matrix rows (bottom part) (see section 7 page 27)

2.3.2 Reset function

There is three ways to reset MIMOSIS1. First, a Power On reset which is asserted at the power up of the chip and deasserted after few milliseconds and reset all the registers and all the finite state machine in the units. Then a RSTB pad which is active low which reset all the registers and all the finite state machine in the units except the monitoring register, the two bandgaps (one for the DACs and one for the PLL), and the PLL. Finally, a soft reset send through the INSTR CMDID which could be global or selective. The global reset is equivalent to the reset through the RSTB pad. The global reset didn't reset the monitoring register, the two bandgaps, and the PLL. When a soft reset is send the reset is asserted and after 2 periods of main clock (frequency of 40 MHz) it is deasserted.

When reset command is selected (with bit 7 equal to 1). Bits 4 to 0 are used to mask on which blocs the reset is applied. Several reset of the same section could be written at once. In case of global reset the mask bits are not used. Table 4 gives the 14 different resets used in MIMOSIS1.

For example, to reset the PLL and the PLL Bandgap without resetting all the other blocs, the parameter given to the INSTR CMDID is b11000110 or hC6. Explanation: bit 7 set to 1 to select reset function, bits 6-5 set to 10 to select reset unit section, bits 4-0 set to 001100 to select PLL and PLL bandgap.

Table 4: INSTR CMDID Resets description

Reset	Section (bits 6-5)	Mask bit	Function
General Configuration	0	0	Reset internal register used for main configuration of MIMOSIS1 (see section 3 p 13)
DAC	0	1	
Sequencer Configuration	0	2	
Monitoring	0	3	
Pixel Control	0	4	
Analogue Pixel Selection	1	0	Reset internal register used for test configuration of MIMOSIS1 (see section 3 p 13), and Flag accessible through INSTR CMDID
Readout Test Configuration	1	1	
Flags	1	4	
Readout	2	0	Reset units of MIMOSIS1
PLL	2	1	
PLL Bandgap	2	2	
Bandgap	2	3	
Clock Divider	2	4	
Global	3	-	Global reset equivalent to RSTB pad

3 Address mapping

3.1 Introduction

The address mapping used in MIMOSIS1 works with a 16-bits address word. The address is set with ADD_MSB and ADD_LSB CMDID. It selects the internal registers which will be written or read using the direct or indirect access mode (see section 1.3 page 8).

3.2 Banks

In order to have an efficient selection of registers and to limit the number or the size of I²C transactions, the internal register are grouped by function. This groups are selectable with a 4-bits word inside the address mapping called bank (BANK[3:0]). The MSB is located on bit 15 of the address. The 3 LSBs are located on bits 7 to 5 of the address. Consequently, BANK[3] is writable with ADD_MSB CMDID, and BANK[2:0] is writable with ADD_LSB CMDID.

The function mapping is organized to minimize the I²C transactions to configure MIMOSIS1 in standard modes (i.e. non-test modes). The major configuration of MIMOSIS1 could be done with the 8 MSBs of the address set to 0. Consequently to configure the most important registers of MIMOSIS1 it is only necessary to use the ADD_LSB CMDID, after having configured only once the ADD_MSB CMDID with 0 (except for pixel control).

Height different banks are used to group different functions and are shown in Table 5.

Table 5: MIMOSIS1 banks description

Function	Bank number	Description
General Configuration	1	To set and configure the different modes
DAC	2	To set the DAC value
Sequencer Configuration	3	To configure the sequencer
Pixel Control	4	To configure the pixel array
Monitoring	7	To monitor registers
Multi-Frame Emulation	8	To emulate hit pixels on several frames (test mode)
Analogue Pixel Selection	9	To select analogue pixel (test mode)
Readout Configuration	10	To configure readout (test mode)

3.3 Detailed description

Table 6 describes the general address mapping. The cells with the background in orange are the part which are combine with the OFFSET register in case of indirect access (see section 1.3.2 page 8). When NU (Not Used) is given in this table the value could be 0 or 1.

Table 6: Address mapping used in MIMOSIS1

Function	Access	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
General Configuration	RW	BANK[3]	NU							BANK[2 :0]			Fixed	Register Address[3] [3:0]			
		0	-							0	0	1	0	0 to 15			
DAC	RW	BANK[3]	NU							BANK[2 :0]			Fixed	Register Address[3] [3:0]			
		0	-							0	1	0	0	0 to 15			
Sequencer Configuration	RW	BANK[3]	NU						Reg. Address[3] [5]	BANK[2 :0]			Register Address[3] [4:0]				
		0	-						see section 6	0	1	1	see section 6				
Pixel Control	RW	BANK[3]	BCAS	Region Address[3] [5:0]						BANK[2 :0]			Register mask [4:0]				
		0		0 to 63						1	0	0	see section 7				
Monitoring	RO	BANK[3]	NU							BANK[2 :0]			Fixed	Register Address[3] [3:0]			
		0	-							1	1	1	0	0 to 15			
Multi-Frame Emulation	RW	BANK[3]	NU	Region Address[3] [5:0]						BANK[2 :0]			NU		Frame Address [2:0]		
		1	-	0 to 63						0	0	0	-		0 to 7		
Analogue Pixel Selection	RW	BANK[3]	NU							BANK[2 :0]			NU				MSB/LSB[3]
		1	-							0	0	1	-				0 or 1
Readout Test Configuration	RW	BANK[3]	NU							BANK[2 :0]			Register Address[3] [4:0]				
		1	-							0	1	0	0 to 19				

[3] Part combined with OFFSET register in case of indirect access mode see section 1.3.2 page 8

4 General Configuration registers

Table 7 gives the general description of the 16 general configuration registers. These registers are available through bank number 1 and are selected with bits 3 to 0 of ADD_LSB CMDID.

Table 7: General Configuration registers description

Register	Address [15:0] Hex	Reset Value Hex	Description of the configuration
RUNMODE	0020	02	Working mode
TRIMDAC	0021	6E	DAC trimming
INJCURR	0022	00	DAC bypass current injection
INJVOLT1	0023	00	DAC bypass voltage injection part 1
INJVOLT2	0024	00	DAC bypass voltage injection part 2
MONCURR	0025	00	DAC current monitoring selection
MONVOLT	0026	00	DAC voltage monitoring selection
CLKGEN1	0027	00	Clocks generator part 1
CLKGEN2	0028	00	Clocks generator part 2
PLL	0029	11	PLL
PLLLOCK	002A	38	PLL lock detector
MONTEMP	002B	00	Temperature sensor monitoring selection
SLVSTX	002C	15	SLVS Transceiver
SLVSRX	002D	08	SLVS Receiver
OUTPUT	002E	00	Output pads
MONPWR	002F	00	Power voltage monitoring selection

4.1 RUNMODE register: Working mode configuration

The RUNMODE register has an impact on the working mode of MIMOSIS1. The modes can be divided into two main parts: the pixels modes for mode working with pixels, and the digital periphery modes for modes working without pixels. Table 8 gives the description of this register.

Table 8: RUNMODE register description: Working mode configuration

Name	Bits	Reset	Description
EN_CLKRESCUE_TERM	7	0	Enable rescue clock (320 MHz) SLVS 100 Ω termination
EN_CLKSER	6	0	Enable output clock serializer (160 MHz) test option
EN_CUSTOM_FLV	5	0	Enable custom fill level for elastic buffer test option
EN_CUSTOM_BW	4	0	Enable custom bandwidth for frame generator test option
EN_PATTERN	3	0	Enable pattern for serializer test mode
EN_PULSEINJ	2	0	Enable external pulse injection test option
EN_PIXELMASK	1	1	Enable Pixel Masked (1) or Pulsed (0) mode for pixel array
EN_MFE	0	0	Enable Multi Frame Emulator test mode

Figure 8 describes the different modes to operate MIMOSIS1. In the pixels modes, there is the running mode which is the standard mode to operate MIMOSIS1, and the pixel pulsing modes which is the mode to inject digital or analogue pulse (selected by EN_PIXELMASK). The pixel pulsing modes could use a pulse generated by the sequencer or by an external source through PULSEINJ pad (selected by EN_PULSEINJ).

In the digital periphery modes, there is the readout test mode to test the readout from the input of the region to the output pads (selected by EN_MFE), and the serializer test mode to test the serializer with a programmable 128-bits words (selected by EN_PATTERN). For more details on the Multi Frame Emulator test mode see section 9 page 31.

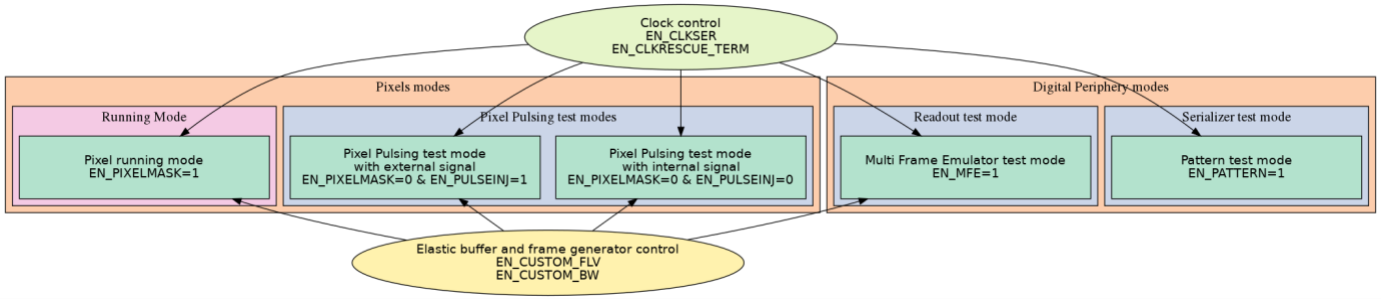

Figure 8: RUNMODE register and modes mapping

The other four bits of the register are used to modulate the modes. Two bits control the clocks which can be used in all the modes. One bit to enable the 160 MHz serializer clock on CLKSER_P and CLKSER_N SLVS pad (selected by EN_CLKSER). Another bit to control the 100 Ω termination of the SLVS rescue clock if it used (selected by EN_CLKRESCUE_TERM). Two other bits control the Elastic Buffer and Frame generator custom level to control parameters of these blocks (see section 11 page 34). In the case of pattern test mode these bits are useless.

4.2 TRIMDAC register: DAC trimming

Table 9 gives the description of the TRIMDAC register which is used to trim the DAC. The TRIM_REFCURR has an impact on all DAC, since it adjust the common current reference. TRIM_VCASNB and TRIM_VCASNC could be used to trim the threshold voltage of the two main pixel sub-arrays (B and C pixels sub-array are ¾ of the full array).

Table 9: TRIMDAC register description: DAC trimming

Name	Bits	Reset	Description
TRIM_VCASNC	7-5	3	Trimming bits for VCASNC
TRIM_VCASNB	4-2	3	Trimming bits for VCASNB
TRIM_REFCUR	1-0	2	Trimming bits for the internal current reference (impact all DACs)

4.3 INJCURR register: DAC bypass current injection configuration

Table 10 gives the description of the INJCURR register which is used to enable the current injection through pads to bypass the DAC.

Table 10: INJCURR register description: DAC bypass current injection configuration

Name	Bits	Reset	Description
Not Used	7-5	0	
IREFPLL	4	0	Enable IREFPLL current injection on pad IREFPLLINJ
IREF	3	0	Enable IREF current injection on pad IREFINJ
ITHR	2	0	Enable ITHR current injection on pad ITHRINJ
IDB	1	0	Enable IDB current injection on pad IDBINJ
IBIAS	0	0	Enable IBIAS current injection on pad IBIASINJ

4.4 INJVOLT1 and INJVOLT2 registers: DAC bypass voltage injection configuration

Table 11 and Table 12 give the description of the INJVOLT1 and INJVOLT2 registers which are used to enable the voltage injection through pads to bypass the DAC. The INJVOLT2 register is focus on the threshold (VCASN) for the different pixel sub-arrays.

Table 11: INJVOLT1 register description: DAC bypass voltage injection configuration part 1

Name	Bits	Reset	Description
Not Used	7-6	0	
VRESET	5	0	Enable VRESET voltage injection on pad VRESETINJ
VCLIP	4	0	Enable VCLIP voltage injection on pad VCLIPINJ
VCASP	3	0	Enable VCASP voltage injection on pad VCASPINJ
VCASN2	2	0	Enable VCASN2 voltage injection on pad VCASN2INJ
VPL	1	0	Enable VPL voltage injection on pad VPLINJ
VPH	0	0	Enable VPH voltage injection on pad VPHINJ

Table 12: INJVOLT2 register description: DAC bypass voltage injection configuration part 2

Name	Bits	Reset	Description
Not Used	7-4	0	
VCASND	3	0	Enable VCASND voltage injection on pad VCASNDINJ
VCASNC	2	0	Enable VCASNC voltage injection on pad VCASNCINJ
VCASNB	1	0	Enable VCASNB voltage injection on pad VCASNBINJ
VCASNA	0	0	Enable VCASNA voltage injection on pad VCASNAINJ

4.5 MONCURR register: DAC current monitoring selection

Table 13 gives the mapping to measure on the IMON pad the selected DAC current. The IMON pad should be connected to a 10 kΩ grounded resistor. If the register is set to 0 the IMON pad is set in high-impedance.

Table 13: MONCURR lookup table

MONCURR Value (Dec)	Current selected on IMON pad
0	None (High Impedance)
1	IBIAS
2	IDB
3	ITHR
4	ITEST

4.6 MONVOLT register: DAC voltage monitoring selection

Table 14 gives the mapping to measure on the VMON pad the selected DAC voltage. If the register is set to 0 the VMON pad is set in high-impedance.

Table 14: MONVOLT lookup table

MONVOLT Value (Dec)	Voltage selected on VMON pad
0	None (High Impedance)
1	VPH
2	VPL
3	VCASN2
4	VCASP
5	VCLIP
6	VRESET
7	VCASNA
8	VCASNB
9	VCASNC
10	VCASND

4.7 CLKGEN1 and CLKGEN2 registers: Clocks generator configuration

Table 15 and Table 16 give the description of the CLKGEN1 and CLKGEN2 registers which are used to configure the clocks generator.

Need to add some details

Table 15: CLKGEN1 register description: Clocks generator configuration part 1

Name	Bits	Reset	Description
SEL_PHASE	7-4	0	320 MHz Clock phase adjustment to adjust internal and external 40 MHz clocks
EN_SYNC	3	0	Enable synchronization of multiple MIMOSIS1 through SYNC_IN_P and SYNC_IN_N SLVS pads
SEL_START	2-1	0	Start mode selection: Automatic: 0 (by default after PLL locked) Software: 1 (by sending 03 to INSTR CMDID see section 2 page 10) External: 2 or 3 (via START_IN_P and START_IN N SLVS pad)
SEL_CLOCK	0	0	Clock selection: Main @ 40 MHz (CLK_P and CLK_N SLVS pad): 0 Rescue @ 320 MHz[4] (CLKRESCUE_P CLKRESCUE_N SLVS pad): 1

Table 16 : CLKGEN2 register description: Clocks generator configuration part 2

Name	Bits	Reset	Description
Not Used	7-6	0	
EN_START_SYNC_TERM	5	0	Enable START_IN and SYNC_IN SLVS 100 Ω termination
FILTER_VAL	4-1	0	Filter glitches on PLL lock flag of N times main clock period (25 ns)
DIS_LOCK_GATING	0	0	Disable generated clocks gating with filtered PLL lock flag

[4] In case of PLL issue

4.8 PLL register: PLL configuration

Table 17 gives the description of the PLL register which is used to configure the PLL. EN_LOCKPLL and EN_CLKPLL are used to enable output pad to observe, respectively, the lock flag and the clock generated by the PLL. TRIM_REFCURPLL is used to trim the PLL current reference. The PLL has an embedded low-dropout (LDO) regulator to power the VCO. It goal is to minimize the consumption and the phase noise of the PLL. It could be disable with DIS_PLL_LDO, and in this case the VCO is powered by the analog domain (AVDD and AVSS). The VCO could be enable with EN_PLL_VCO. The VCO could be disable in case of PLL failure and the use of CLKRESCUE_P and CLKRESCUE_N SLVS pad. It is recommended, in this case, to disable the VCO to limit the noise induced by a free running VCO.

Table 17: PLL register description: PLL configuration

Name	Bits	Reset	Description
Not Used	7	0	
EN_ LOCKPLL	6	0	Enable LOCKPLL pad
EN_CLKPLL	5	0	Enable CLKPLL_P CLKPLL_N SLVS pad
TRIM_ REFCURPLL	4-2	4	Trimming bits for PLL current reference
DIS_PLL_LDO	1	0	Disable low-dropout PLL regulator (when disable VCO powered through AVDD and AVSS)
EN_PLL_VCO	0	1	Enable VCO

4.9 PLLLOCK register: PLL lock detector configuration

Table 18 gives the description of the PLLLOCK register which is used to configure the PLL lock detector. The lock detector is based on a current comparator, which has a variable gain (with GAIN) and a variable threshold (THRESHOLD).

Table 18: PLLLOCK register description: PLL lock detector configuration

Name	Bits	Reset	Description
Not Used	7	0	
GAIN	6-3	7	Gain of current comparator to detect PLL lock from phase comparator
THRESHOLD	2-0	0	Threshold of current comparator to detect PLL lock from phase comparator

4.10 MONTEMP register: Temperature sensor monitoring selection

Table 19 gives the description of the MONTEMP register which is used to select one of the 32 differential temperature sensors on the TMONP and TMONN pads. If the EN_TMON is set to 0 the pads are in high impedance. The position of the temperature sensors are given in appendix A.

Table 19: MONTEMP register description: Temperature sensor monitoring selection

Name	Bits	Reset	Description
Not Used	7-6	0	
EN_TMON	5	0	Enable TMONP and TMONN pads
SEL_CODE	4-0	0	Select one of the 32 differential temperature sensors

4.11 SLVSTX register: SLVS TX configuration

Table 20 gives the description of the SLVSTX register which is used to configure the bias of the SLVS transceiver. This configuration is common for all the SLVS transceiver pads. The bias gives a voltage to set the common mode of the differential signal (SLVS standard is 200 mV). This voltage is derivate from the power supply and the bit BIAS_TXV allows to add 20%, if the power supply is low. The bias generates also a current for the amplifier inside the pad which could be adjusted with BIAS_TXI.

Table 20: SLVSTX register description: SLVS TX configuration

Name	Bits	Reset	Description
Not Used	7-6	0	
DIS_BIAS_TXV	5	0	Disable common mode voltage for SLVS transmitter allowing injection from VCMSLVSINJ pad
BIAS_TXV	4	1	Add 20% on the standard common mode voltage for SLVS transmitter if set to 1 (standard value 200 mV)
BIAS_TXI	3-0	5	Current DAC for SLVS transmitter pad (common for all pad)

4.12 SLVSRX register: SLVS RX configuration

Table 21 gives the description of the SLVSRX register which is used to configure the bias of the SLVS receiver. The register is divided in two parts, the BIAS_RX_CLKRESCUE is to adjust the current of the CLKRESCUE_P and CLKRESCUE_N pads, and the BIAS_RX is to adjust the current for all the other SLVS receiver.

Table 21: SLVSRX register description: SLVS RX configuration

Name	Bits	Reset	Description
BIAS_RX_CLKRESCUE	7-4	0	Current DAC for SLVS CLKRESCUE receiver pad
BIAS_RX	3-0	8	Current DAC for all other SLVS receiver pad

4.13 OUTPUT register: Output pads configuration

Table 22 gives the description of the OUTPUT register which is used to configure some output pads. EN_SEQMARKER1, EN_SEQMARKER2, and EN_DATAMARKER are to enable SLVS pads. The OUTPUTMODE is to configure the number of DATA output pads which are used. If the EN_SOFT_OUTPUTMODE is set to 1 the configuration of the output is done by the register otherwise it is done by the CMOS pads OUPTUMODE. The EN_ALWAYS_DATA is to avoid high impedance output on DATA pads when all the output are not used.

Table 22: OUTPUT register description: Output pads configuration

Name	Bits	Reset	Description
Not Used	7	0	
EN_SEQMARKER2	6	0	Enable SEQMARKER2_P SEQMARKER2_N SLVS pads
EN_SEQMARKER1	5	0	Enable SEQMARKER1_P SEQMARKER1_N SLVS pads
EN_DATAMARKER	4	0	Enable DATAMARKER_P DATAMARKER_N SLVS pads
EN_ALWAYS_DATA	3	0	Enable all DATA_P[7:0] and DATA_N[7:0] SLVS pads independently of OUTPUTMODE to avoid floating outputs[5]
EN_SOFT_OUTPUTMODE	2	0	Enable OUTPUTMODE configuration through registers instead of pads
OUTPUTMODE	1-0	0	OUTPUTMODE configuration setting: 0: 1 output 1: 2 outputs 2: 4 outputs 3: 8 outputs

4.14 MONPWR register: Power voltage monitoring selection

Table 23 gives the description of the MONPWR register which is used to select one of the 16 power monitor on the PWRMON pad. Each monitor could monitor the power or the ground. The DVSS_PRB and AVSS_PRB pads could be used as references of the digital or analogue domain. The SEL_DOMAIN is to select the analogue (1) or digital (0) power domain. SEL_PWR_GRD is to select the power (1) or the ground (0). Then SEL_CODE is to select one of the 8 power monitors of the domain. The position of the power sensors are given in appendix B.

Table 23: MONPWR register description: Power voltage monitoring selection

Name	Bits	Reset	Description
Not Used	7-6	0	
SEL_DOMAIN	5	0	Analogue (1) or digital (0) power domain selection
SEL_PWR_GRD	4	0	Power (1) or ground (0) selection
SEL_CODE	3-0	0	Select one of the 8 power monitors of the domain

[5] Didn't change data scheme

5 DAC registers

Table 24 gives the general description of the 15 DAC registers. These registers are available through bank number 2 and are selected with bits 3 to 0 of ADD_LSB CMDID. All the DACs, except the IBUFBIAS, are used to control voltages or currents for the pixels. The detail description of the voltages and currents for the pixels are describe in another document (not written yet).

Table 24: DAC registers general description

Register	Address	Reset Value			Range		Step	Description
	Hex	Hex	Dec	Ana	Min	Max		
IBIAS	0040	40	64	20 nA	0 nA	80 nA	312 pA	Pixel current
ITHR	0041	34	52	0.5 nA	0 nA	2.5 nA	9.8 pA	Pixel current
IDB	0042	1C	28	4.4 nA	0 nA	40 nA	157 pA	Pixel current
VRESET	0043	AB	171	1.4 V	0.37 V	1.79 V	6 mV	Pixel input amplifier reset voltage
VPL	0044	57	87	0.9V	0.37 V	1.79 V	6 mV	Pixel voltage for charge injection (low value)
VPH	0045	68	104	1.0 V	0.37 V	1.79 V	6 mV	Pixel voltage for charge injection (high value) VPH+VPH_FINE
VPH_FINE	0046	0	0	0 V	0 V	256 mV	1 mV	
VCASP	0047	43	67	0.4 V	0 V	1.54 V	6 mV	Pixel voltage
VCASNA	0048	53	83	0.5 V	0 V	1.54 V	6 mV	Pixel threshold voltage for submatrix A
VCASNB	0049	53	83	0.5 V	0 V	1.54 V	6 mV	Pixel threshold voltage for submatrix B
VCASNC	004A	53	83	0.5 V	0 V	1.54 V	6 mV	Pixel threshold voltage for submatrix C
VCASND	004B	53	83	0.5 V	0 V	1.54 V	6 mV	Pixel threshold voltage for submatrix D
VCASN2	004C	53	83	0..5 V	0 V	1.54 V	6 mV	Pixel voltage
VCLIP	004D	32	50	0.3 V	0 V	1.54 V	6 mV	Pixel clipping amplifier voltage
IBUFBIAS	004E	7D	125	5 µA	0 nA	10 µA	312 pA	Internal buffer bias (not in pixel)

6 Sequencer Configuration registers

Table 25 gives the general description of the 49 Sequencer configuration 8-bits registers. These registers are available through bank number 3 and are selected with bits 4 to 0 of ADD_LSB CMDID and bit 0 of ADD_MSB CMDID.

Table 25: Sequencer Configuration registers general description

Register	8 MSB address Hex	8 LSB address Hex	register number MSB	register number LSB	reset value MSB	reset value LSB	Type	Description
PIXLOAD_A	0160	0060	10	0	0	0	Sig.	Pixel signal to transfer the value from the recorder memory to the player memory
PIXLOAD_B	0170	0070	30	20	0	1		
PIXREAD_A	0161	0061	11	1	0	0	Sig.	Pixel signal to read the value of the player memory and reset its
PIXREAD_B	0171	0071	31	21	0	97		
PIXRSTB_A	0162	0062	12	2	0	98	Sig.	Pixel signal to reset all the player memories
PIXRSTB_B	0172	0072	32	22	0	99		
DPSTART_A	0163	0063	13	3	0	0	Sig.	Digital Periphery signal to start the readout of a new frame
DPSTART_B	0173	0073	33	23	0	1		
DPTOKEN_A	0164	0064	14	4	0	1	Sig.	Digital Periphery signal to launch the data in the readout
DPTOKEN_B	0174	0074	34	24	0	2		
DPEND_A	0165	0065	15	5	0	98	Sig.	Digital Periphery signal to end the readout of the current frame
DPEND_B	0175	0075	35	25	0	99		
PIXPULSEA_A	0166	0066	16	6	0	0	Sig.	Pixel signal to generate an analogue pulse
PIXPULSEA_B	0176	0076	36	26	0	0		
PIXPULSED_A	0167	0067	17	7	0	0	Sig.	Pixel signal to generate a digital pulse
PIXPULSED_B	0177	0077	37	27	0	0		
MKSEQ1_A	0168	0068	18	8	0	0	Sig.	Sequencer signal connected to the pad SEQMARKER1 gated every N frames (N=1,2,4,8,16,32,64, or 128)
MKSEQ1_B	0178	0078	38	28	0	2		
MKSEQ2_A	0169	0069	19	9	0	0	Sig.	Sequencer signal connected to the pad SEQMARKER2
MKSEQ2_B	0179	0079	39	29	0	2		
POLARITY	017A	007A	46	40	0	5	Par.	10 bit polarity parameter for the 10 configurable signals (one hot encoding)
FRAMELENGTH	017B	007B	47	41	0	100	Par.	Parameter to define the frame length
MAXFRAME	017C	007C	48	42	0	0	Par.	Parameter to define the maximum number of frames to halt the sequencer
MODPULSE	NU	007D		43	0	0	Par.	Parameter to gate PIXPULSEA/D every N frames (N=1,2,4,8,16,32,64, or 128)
MODPIXRSTB	NU	007E		44	0	0	Par.	Parameter to gate PIXRSTB every N frames (N=1,2,4,8,16,32,64, or 128)
MODMKSEQ1	NU	007F		45	0	0	Par.	Parameter to gate MKSEQ1 every N frames (N=1,2,4,8,16,32,64, or 128)

6.1 Sequencer description

The sequencer generates 10 configurable signals. Five of them are distributed to the pixel and start with the PIX prefix. Three of them are send to the digital periphery and start with the DP prefix. Then, two of them go directly to pad for external synchronization and start with the MK prefix.

The sequencer is configured through 6 parameters (either with 8-bits or 16-bits words) and a set of 2 16-bits words for each signal. The addresses of the 8 MSBs of the registers are available with the bit 0 set to 1 of the ADDR_MSB CMDID. The 8 MSBs-of the sequencer configuration registers, except for POLARITY register, need to be configured for long integration time (larger than 12.8 µs with nominal main clock set to 40 MHz).

6.1.1 Sequencer parameters

The FRAMELENGTH register defined the period of the 10 signals by counting the number of 20 MHz clock period (the sequencer clock is the main clock divided by 2). When the number of 20 MHz clock period reach the value of FRAMELENGTH, the signals are restarted.

The MAXFRAME register define the number of frames to halt the sequencer. If it is set to 0 the sequencer run indefinitely.

The MODPULSE, MODPIXRSTB and MODMKSEQ1 registers are used to gate the signal every N frames with N equal to 2^{MODREG} with a maximum of 7 for MODREG. MODEPULSE gates the signal PIXPULSEA or PIXPULSED. MODPIXRSTB gates the signal PIXRSTB. MODMKSEQ1 gates the signal MKSEQ1. Figure 9: Sequencer gating exampleFigure 9 shows an example of gating with MKSEQ1 with MODMKSEQ1 set to 2. MKSEQ2 is a copy of MKSEQ1 without gating. In this example, every 4 frames (2^2) the signal is repeated.

6.1.2 Sequencer signals

A signal is entirely defined with 2 16-bits words (with _A and _B suffix) and the POLARITY register. The sequencer use an internal counter which it incremented every rising edge of the clock sequencer. The sequencer clock is the main clock divided by 2 and leads to a period of 50 ns for the nominal value of 40 MHz. The maximum value of this counter is set with FRAMELENGT register. When the value of the internal counter reach the lowest value set in one of both register associated with a signal (with the _A and _B suffix) the value of the signal is toggle. Then when the value of the internal counter reach the highest value set in the registers, the value of the signal is toggle and go back to its initial value.

The value of both registers associated with a signal could be inverted, there is no predefine order.

The initial value is given by the POLARITY register with a one hot encoding (see Table 26 for detail). If both registers (_A and _B) are set to 0 the value of the signal is constant and depends only of the initial value. Figure 10 shows an example of configuration for the sequencer with two different values of POLARITY

Table 26: POLARITY register detail

Signal	POLARITY bit
PIXLOAD	0
PIXREAD	1
PIXRSTB	2
DPSTART	3
DPTOKEN	4
DPEND	5
PIXPULSEA	6
PIXPULSED	7
MKSEQ1	8
MKSEQ2	9

6.2 Sequencer registers recommended relative values

To ensure the synchronization between the pixel readout and the digital periphery readout some relative values must be maintain. It is not recommended to change it.

Table 27 gives the recommended relative values of some critical signals use for synchronization. These values depend of the given FRAMELENGTH set to L.

Table 27: Sequencer registers recommended relative values

Register	Value	Note
FRAMELENGTH	L	Initial value which depends the other
PIXLOAD_A	0	Recommended to be fixed
PIXLOAD_B	1	Recommended to be fixed
DPSTART_A	0	Recommended to be fixed
DPSTART_B	1	Recommended to be fixed
DPTOKEN_A	1	Recommended to be fixed
DPTOKEN_B	2	Recommended to be fixed
DPEND_A	L-2	
DPEND_B	L-1	
PIXREAD_A	0	Could be higher (the difference between PIXREAD_A and PIXREAD_B gives the maximum number of read pixels)
PIXREAD_B	L-3	Could be lower
PIXRSTB_A	L-2	Could be lower but keeping at least larger than PIXREAD_B+1
PIXRSTB_B	L-1	Could be lower

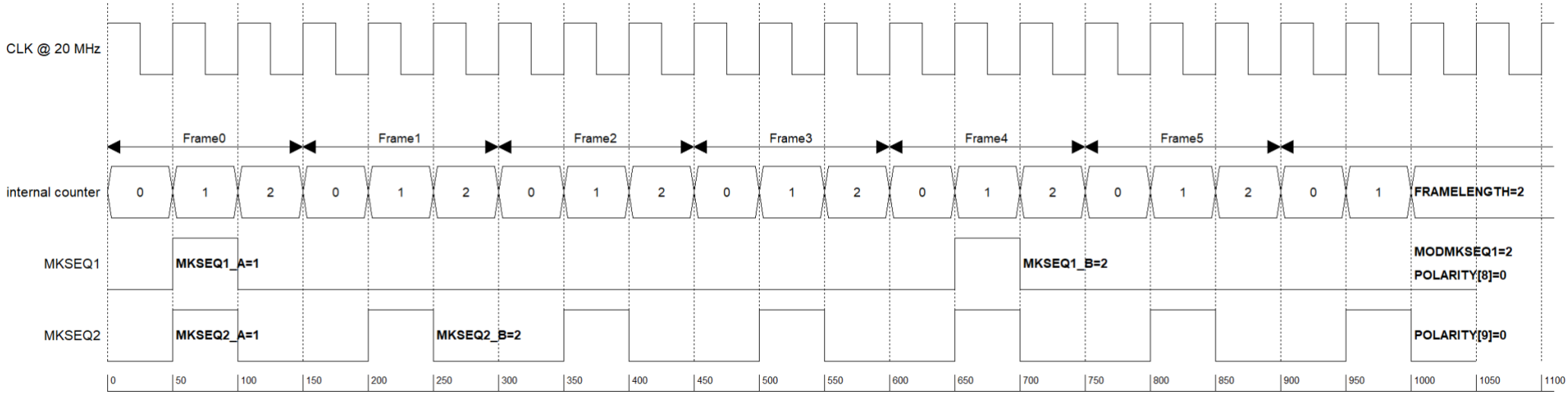

Figure 9: Sequencer gating example

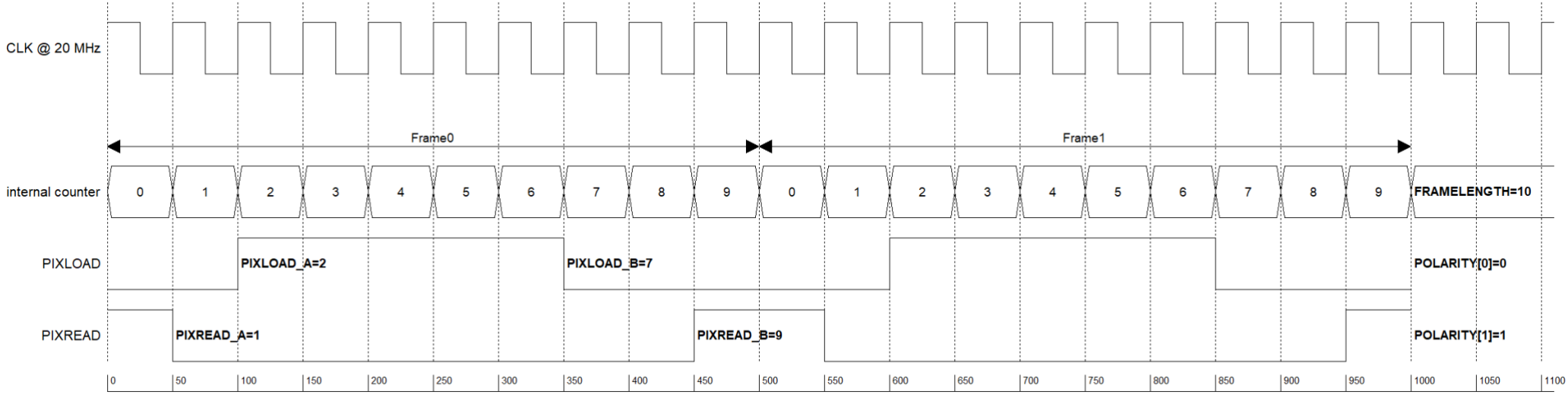

Figure 10: Sequencer configuration example

7 Pixel Control registers

The 320 pixel control registers are divided in 5 registers in each 64 regions. These registers are available through bank number 4 and are selected with bits 5 to 0 of ADD_MSB CMDID to select the region and bits 4 to 0 of ADD_LSB CMDID to select the type of registers.

Table 28 gives the region selection scheme for pixel control registers through the ADD_MSB CMDID. The address of the region where the registers are written is given by bits 5 to 0. The region 0 is located on the left side of the chip and the Region 63 is located on the right side of the chip (with the pads located at the bottom). A broadcast function is accessible with bit 6 to write the corresponding registers in all the region in one command. The region address section is the section incremented during the indirect access.

Table 28: Pixel control registers selection through ADD_MSB CMDID

7	6	5	4	3	2	1	0
BANK[3]	Broadcast Region	Region Address [5:0]					
0	Selection all regions (1) or one (0)	0 to 63					

Table 29 gives the register selection inside a region. Each bit of the Register mask is associated to a register. In case of write access, if a bit is set to one the value is written to the corresponding registers (one or several).

Table 29: Pixel control registers selection through ADD_LSB CMDID

7	6	5	4	3	2	1	0
BANK[2:0]			Register mask [4:0]				
1	0	0	PULSE_GATING	DIS_PE	SEL_ROW	SEL_COLRIGHT	SEL_COLLEFT

Table 30 gives the general description of the 5 pixel control registers inside a region. The interpretation of the addressing depends if the register use a column or a row addressing scheme.

7.1 Column addressing scheme

The registers using a column addressing scheme are based on the address of the pixel priority encoder (from 0 to 511). The region address multiply by 8 gives the address of the first pixel priority encoder in a group of 8. Then, if bit N is set to 1 in the written word, the N^{th} pixel priority encoder inside the group is selected.

For example, if 10 is sent to the register at the region address 18, the address of the selected pixel priority encoder are 145 and 147 (18x8+1 and 18x8+3).

Reciprocally, to select line M, the corresponding region address is given by the Euclidean division of M by 8, and the bit given by M modulus 8 of the send word is set to 1.

For example, to select column 341, the region address is 42 (341/8) and the bit 5 (341 mod 8) of the send word is set to 1.

7.2 Row addressing scheme

The register using the row addressing scheme are based on the row number (from 0 to 503). There are using a similar working principle than the column addressing scheme. The region address multiply by 8 gives the address of the first row in a group of 8. Then, if bit N is set to 1 in the written word, the N^{th} row inside the group is selected.

Table 30: Pixel control registers general description

Register Name	Addressing Scheme	Description
PULSE_GATING	Column	Gate the PIXPULSEA or PIXPULSED signal in the pixel priority encoder
DIS_PE	Column	Disable the pixel priority encoder by masking the valid signal
SEL_ROW	Row	Select a row of pixels to store data inside the pixel
SEL_COLRIGHT	Column	Select the right column of pixels respect to the pixel priority encoder (i.e. pixel address modulo 4 is equal to 1 or 2) to store data inside the pixel
SEL_COLLEFT	Column	Select the right column of pixels respect to the pixel priority encoder (i.e. pixel address modulo 4 is equal to 0 or 3) to store data inside the pixel

7.3 Registers description

The PULSE_GATING registers are used to limit the spread of the PIXPULSEA and PIXPULSED in the whole matrix when pulsing mode (analogue or digital) is used, and then the noise on the power supplies.

The DIS_PE registers are used to disable the priority encoder by masking the valid signal. Thus, the read signal is not send to the pixels connected to the disabled priority encoders.

The SEL_ROW, SEL_COLRIGHT, and SEL_COLLEFT registers are used together to select one or several rows, and one or several columns. When a pixel has is row and column selected together, it enables the writing mode of the memory inside the pixel. The data written in the memory is set through the flag MASK_PULSE_DATA of the INSTR CMDID. This memory is used to mask or to enable the pulsing of the pixel depending of the EN_PIXELMASK signal (bit 1 of RUNMODE register). If the EN_PIXELMASK is set to 1 the memory works in masking mode.

8 Monitoring registers

Table 31 gives the general description of the 15 monitoring registers. These registers are available through bank number 7 and are selected with bits 3 to 0 of ADD_LSB CMDID. There is two kinds of monitoring registers, the monitor type and the event type. The monitor type gives an image of the bit associated with it. The event type works as an event counter a return the number of event has occurred on the associated bit. The reset value of the MON_POR_LOCK and MON_PAD depends of the status of some blocks and are not predictable.

Table 31: Monitoring registers general description

Register	Address [15:0] Hex	Reset Value Hex	Type	Description of the monitoring
MON_POR_LOCK	00E0	--	Monitor	Power On Rest and PLL lock
MON_PAD	00E1	--	Monitor	PADs
MON_FR_CPT_0	00E2	00	Monitor	Frame counter bits 7-0
MON_FR_CPT_1	00E3	00	Monitor	Frame counter bits 15-8
MON_FR_CPT_2	00E4	00	Monitor	Frame counter bits 23-16
MON_FR_CPT_3	00E5	00	Monitor	Frame counter bits 31-24
EV_TMR_SEQ	00E6	00	Event	Triple Modular Redundancy Error in sequencer
EV_LOCK	00E7	00	Event	PLL lock
EV_LOCKFILTER	00E8	00	Event	PLL lock after filtering
EV_POR1	00E9	00	Event	Power On Reset 1
EV_POR2	00EA	00	Event	Power On Reset 2
EV_POR3	00EB	00	Event	Power On Reset 3
EV_RSTB	00EC	00	Event	RSTB pad
EV_START	00ED	00	Event	START all types (auto, pad, and soft)
EV_DPSTART	00EE	00	Event	Digital Periphery Start

8.1 MON_POR_LOCK register

Table 32: MON_POR_LOCK register descriptionTable 32 gives the description of the MON_POR_LOCK register which is used to monitor the PLL lock flag and the power on reset blocs. LOCK and LOCKFILTER gives the status of the PLL lock before and after filtering (see section 4.9 page 19). The POR1, POR2 and POR3 are to monitor the status of the three power on reset used for redundancy to prevent single event effect.

Table 32: MON_POR_LOCK register description

Name	Bits	Reset	Description
Not Used	7-5	0	
LOCKFILTER	4	-	PLL lock after filtering (reset value depends of PLL status)
LOCK	3	-	PLL lock (reset value depends of PLL status)
POR3	2	0	Power On Reset 3
POR2	1	0	Power On Reset 2
POR1	0	0	Power On Reset 1

8.2 MON_PAD register

Table 33 gives the description of the MON_PAD register which is used to monitor the value of some pads.

Table 33: MON_PAD register description

Name	Bits	Reset	Description
Not Used	7-6	0	
DISPOR	5	-	DISPOR CMOS pad
ENINCR	4	-	ENINCR CMOS pad
SYNC_IN	3	-	SYNC_IN SLVS pad
START_IN	2	-	START_IN SLVS pad
OUTPUTMODE	1-0	-	OUTPUTMODE[1:0] CMOS pad

8.3 MON_FR_CPT registers

Table 34 gives the description of the four MON_FR_CPT registers which are used to monitor the value of the frame counter (32-bits word).

Table 34: MON_FR_CPT registers description

Name	Bits	Reset	Description
MON_FR_CPT_3	31-24	0	32 bits Frame counter split over 4 8-bits registers
MON_FR_CPT_2	23-16	0	
MON_FR_CPT_1	15-8	0	
MON_FR_CPT_0	7-0	0	

8.4 Event registers

The event registers are incremented on every event (rising or falling edge). There are experimental and could be affected by glitch issue.

9 Multi-Frame Emulation memories

The Multi-Frame Emulation memories are composed of 64 memories with 8 words of 8 bits. These memories are used with the Multi-Frame Emulation mode which is enable with EN_MFE signal (bit 0 of RUNMODE register). This mode consists in emulating the pixel region response.

Each memories are coupled to a region. Each word are associated with a frame. These registers are available through bank number 8 and are selected with bits 5 to 0 of ADD_MSB CMDID to select the region and bits 2 to 0 of ADD_LSB CMDID to select the frame number.

Table 35 gives the region selection scheme for Multi-Frame Emulation through the ADD_MSB CMDID. The address of the region where the registers are written is given by bits 5 to 0. The region 0 is located on the left side of the chip and the Region 63 is located on the right side of the chip (with the pads located at the bottom).

Table 35: Multi-Frame Emulation memories selection through ADD_MSB CMDID

Bit	7	6	5	4	3	2	1	0
Name	BANK[3]	NU	Region Address [5:0]					
Value	1	-	0 to 63					

Table 36 gives the frame address scheme for Multi-Frame Emulation memories.

Table 36: Multi-Frame Emulation memories selection through ADD_LSB CMDID

Bit	7	6	5	4	3	2	1	0
Name	BANK[2:0]			NU		Frame Address [2:0]		
Value	1	0	0	0		0 to 7		

The Multi-Frame Emulation memories are based on memories and could not be reset. Before using them, it is recommended to write all the values.

The Multi-Frame Emulation mode send 16-bits words at the input of the region buffers to replace the pixel response. Table 37 gives the scheme of the send word. The MSB is fixed to 0 to be sure that there is no dedicated words in the data frame. Bits 14 to 12 are the truncated region number LSBs. Bits 11-8 are the truncated frame counter LSBs. And bits 7 to 0 are the emulated pixel counter. The emulated pixel counter is incremented each times a pixel is read (every 50 ns). The maximum value of this counter is given by the value stores in the Multi-Frame Emulation memories. This maximum value could be different for each region and for each frames. Every 8 frames the maximum value are repeated.

Table 37: Data word send in Multi-Frame Emulation mode

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Fixed	Region Number			Frame Counter				Emulated Pixel Counter							
Value	0	0 to 7			0 to 15				0 to N							

The maximum value for the Emulated Pixel Counter could not be greater than the programed FRAMELENGTH (see section 6 page 23)

10 Analogue Pixel Selection

Table 38 gives the general description of the 2 analogue pixel selection. These registers are available through bank number 9 and are selected with bit 0 of ADD_LSB CMDID. SEL_ANAPIX0 and SEL_ANAPIX1 are combined together to form 16-bits words called SEL_ANAPIX.

Table 38: Analogue Pixel Selection registers general description

Register	Address [15:0] Hex	Reset Value Hex	Description of the configuration
SEL_ANAPIX0	8020	00	Analogue Pixel Selection LSB
SEL_ANAPIX1	8021	00	Analogue Pixel Selection MSB

The SEL_ANAPIX is used to select and connect a pixel in the first row. The output of the amplifier and the output of the discriminator are respectively connected to pads ANAOUT[0] and ANAOUT[1]. If SEL_ANAPIX is set to 0 no pixel are connect to output pads. If SEL_ANAPIX is set to a value different of 0, the pixel located at the column address SEL_ANAPIX-1 is connect to the pads. The left column address is 0 and the right column address is 1023.

11 Readout Test Configuration registers

Table 39Table 7 gives the general description of the 20 readout test configuration registers. These registers are available through bank number 10 and are selected with bits 4 to 0 of ADD_LSB CMDID. These registers allows to define 3 words used to test the serializer and the elastic buffer (PATTERN, BANDWIDTH and FILLLEVEL).

Table 39: General Configuration registers description

Register	Address [15:0] Hex	Reset Value Hex	Description of the configuration
PATTERN0	8040	00	128-bits pattern word send to the serializer when EN_PATTERN set to 1 (see section 4.1) PATTERN0 are the LSB and PATTERN15 are the MSB
PATTERN1	8041	00	
PATTERN2	8042	00	
PATTERN3	8043	00	
PATTERN4	8044	00	
PATTERN5	8045	00	
PATTERN6	8046	00	
PATTERN7	8047	00	
PATTERN8	8048	00	
PATTERN9	8049	00	
PATTERN10	804A	00	
PATTERN11	804B	00	
PATTERN12	804C	00	
PATTERN13	804D	00	
PATTERN14	804E	00	
PATTERN15	804F	00	
BANDWIDTH0	8050	00	10-bits word used in the frame generator when EN_CUSTOM_BW set to 1(see section 4.1) BANDWIDTH0 are the LSB and BANDWIDTH1 are the MSB
BANDWIDTH1	8051	00	
FILLLEVEL0	8052	00	11-bits word used in the elastic buffer when EN_CUSTOM_FLV set to 1(see section 4.1) FILLLEVEL 0are the LSB and FILLEVEL1 are the MSB
FILLLEVEL1	8053	00	

PATTERN is a 128-bits words used to test the serialization. This word is send indefinitely to the serializer when EN_PATTERN is set to 1.

BANDWIDTH and FILLLEVEL are words to define the level of saturation of the elastic buffers. BANDWIDTH is a 10-bits words used in the frame generator to define the capability in term of words of the serializer during one frame duration. It depends of the number of outputs and the frame duration. FILLLEVEL is an 11-bits words used in the elastic buffer to define the number of words that could be written in the elastic buffer during a frame duration.

BANDWIDTH and FILLLEVEL could have an important impact on the saturation of the elastic buffer. Please don't used the associated mode unless you know you are doing.

Appendix A: Temperature Sensor location

Need to be done

Appendix B: Power sensor location

Need to be done