MIMOSIS1 Description

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1 Introduction

The purpose of this document is the description of MIMOSIS1 architecture. MIMOSIS1 is the first full-scale prototype aimed for the CBM-MVD. The sensor is based on the ALPIDE sensor used for the ALICE ITS. It will be engineered in Tower Semiconductor 180 nm CMOS Image sensor process, which comes with a quad-well technology and a certain flexibility in terms of the thickness of the epitaxial layer.

2 Logical arrangement

2.1 Introduction

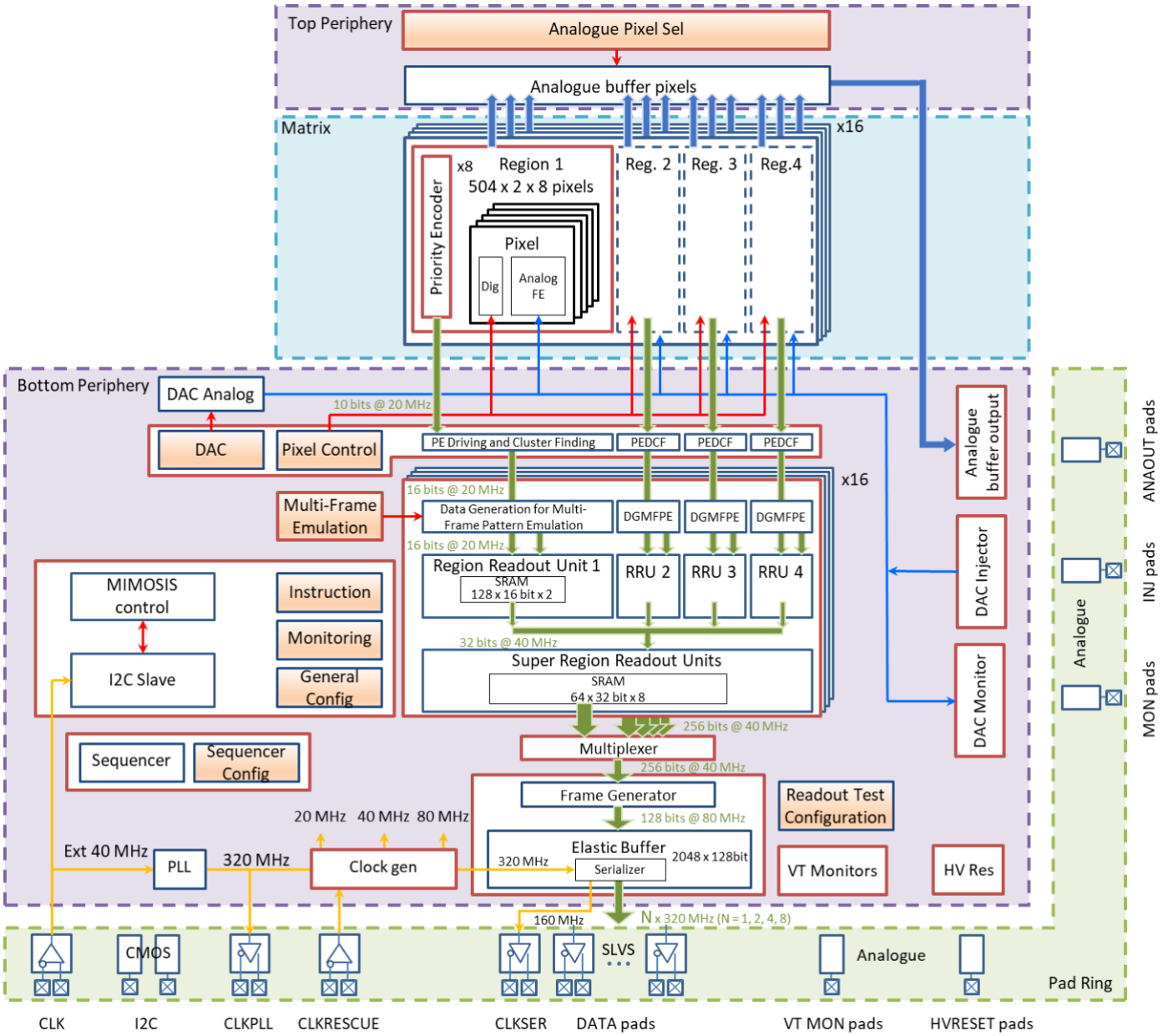


Figure 1: MIMOSIS1 logical arrangement

Figure 1 shows the logical arrangement of MIMOSIS1. The sensor could be divided in 4 parts:

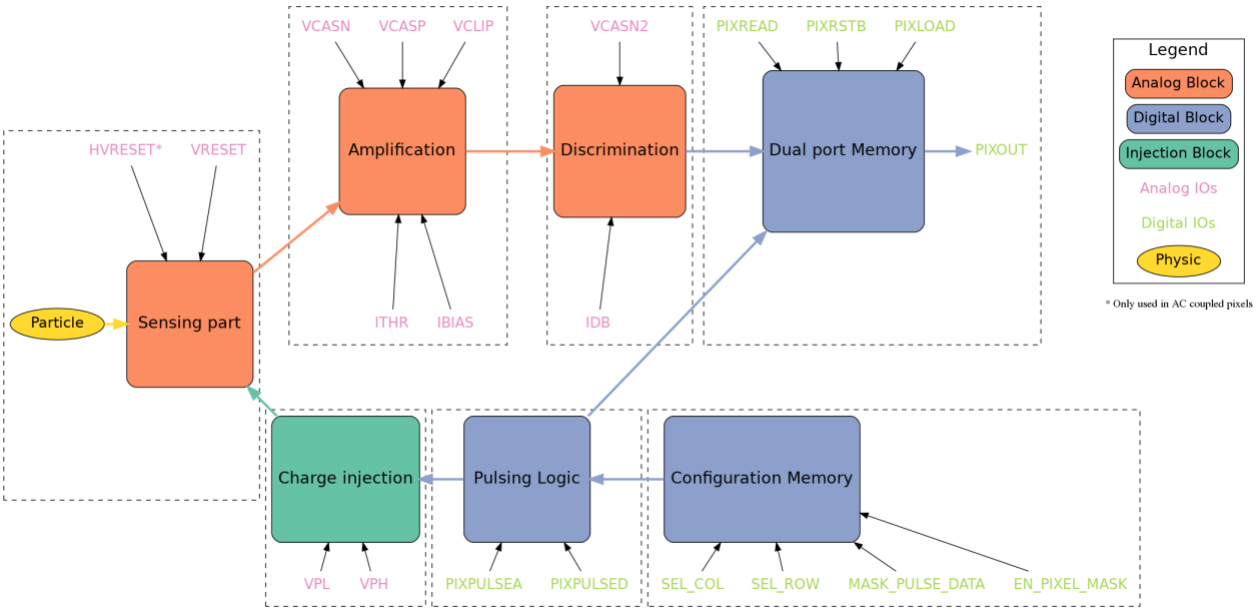
- The pad ring which is the interface with the outside world. It is located at the bottom edge of the sensor;
- The top periphery where an analog readout of the first row of pixels is implemented. It is located at the top edge o f the sensor;

- The bottom periphery where all the logic to configure and read the sensor are located; It is located bellow the pixels matrix.
- The pixels matrix which is the sensitive part and is composed of 1024 columns by 504 rows.

2.2 Pixel readout description

This section will describes the pixel readout from the pixel to the output pads.

2.2.1 Pixel



2.2.2 Region

For the readout, the pixels array is divided into 64 logical part called Region. All the Regions are read in parallel. Figure 2 shows the pixels Region arrangement. A region is coumposed of 8 Pixel Priority Encoders (PPE). PPE provides the signal to control and read a double column of 504 pixels each, thus the PPE control and read 1008 pixels.

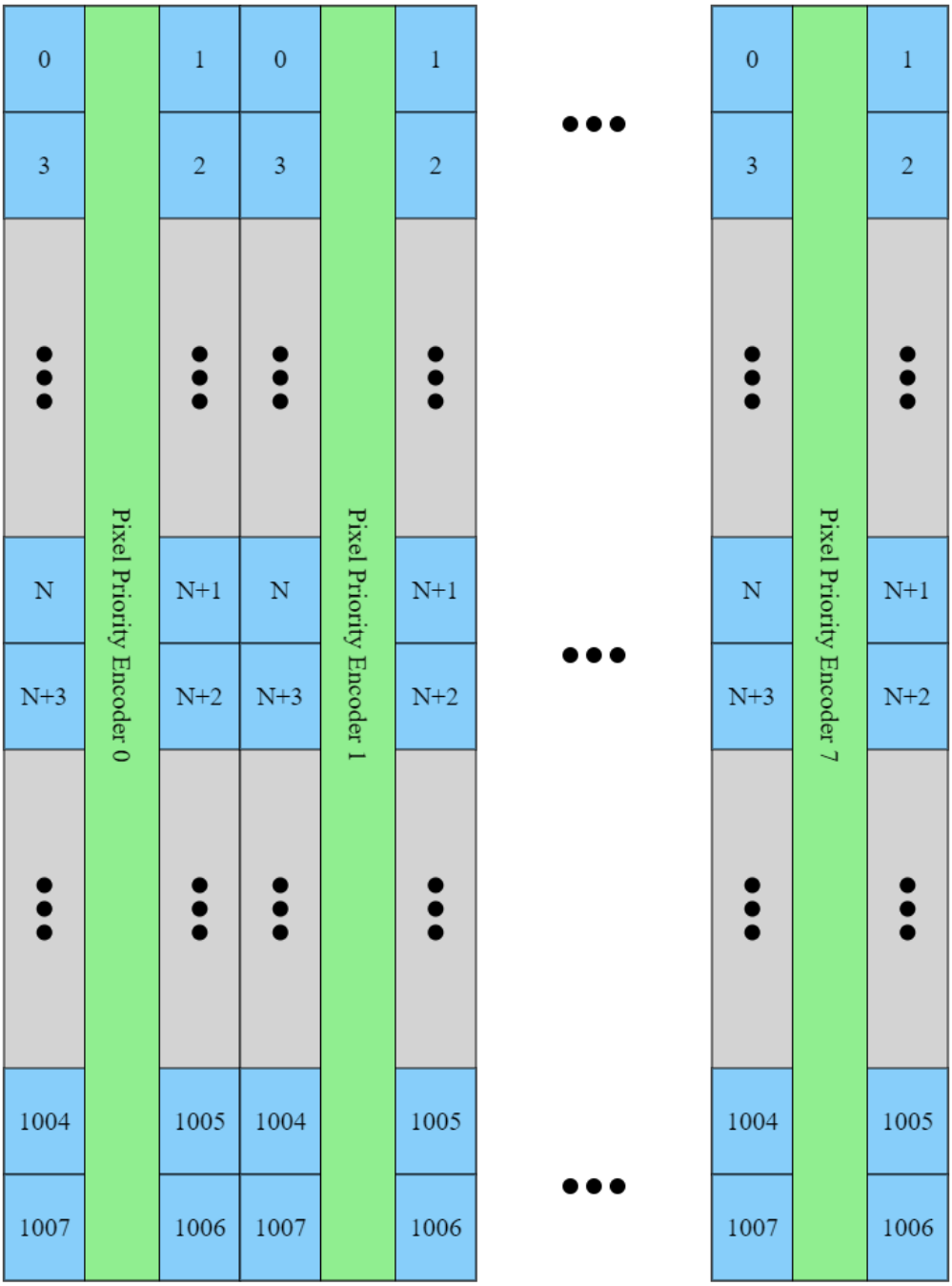


Figure 2: MIMOSIS1 Region description

The PPE drives the commands to the appropriate pixels and compute the 10 bits address of the pixel which is currently read. The PPE computes the addresses of the hit pixels starting with the pixels having the lowest address (from top to bottom). The PPE inside a region are read serially starting from the PPE with the lowest address (from left to right) by the Column Priority Encoder (CPE).

The CPE works smilarly to the PPE, it drives the commands to the appropriate PPE and computes the 3 bits address of the PPE which is currently read. The CPE reads only the PPE with hit pixels. The two addresses are combine to form a 16-bits data word (3 bits are reserved for cluster coding which will be implementet in MIMOSIS2). The 16-bits data words provided by the CPE of one region are stored in a memory located in the Region Readout Unit (RRU). At the beginning of each frame a region header which is used to tag the Region number inside the data frame, is generated and store in the RRU memory (see

MIMOSIS1 Data Format document). The memories inside the RRU are double port memories using a double buffering technique. One half of the memory is used to write the current frame and the other half is used to read the previous frame.

During the readout of the Region an overflow can occur if the number of hit pixels inside the region is larger than the duration of the PIXREAD signal express in CLK half clock period (50 ns, if 40 MHz is used). The duration of the PIXREAD is given by the difference between the two sequencer configuration registers PIXREAD_A and PIXREAD_B (see MIMOSIS1 I²C controller document, section 6). By default this duration is set to 97. The duration of PIXREAD must be lower than or equal to 127, otherwise in case of saturation all the previous written data are lost. This limitation comes from the size of the memory of the RRU, which is 128 16-bits words minus one to store the region header.

2.2.3 Super Region

The Super Region is a group of 4 Regions, and do not intervene in pixel address scheme unlike the Region. They are used to mitigate data bandwidth over the width of the sensors. All the Super Region are read in parallel. The Region Readout Unit memory inside a Super Region are read serially starting from the Region with the lowest address (from left to right) using a token mechanism. Consequently, all RRU without hit are skipped. Two 16-bits data words from the RRU memory are store in the memory of the Super Region Unit (SRU) at the same time. The memories inside the SRU are double port memories using a double buffering technique. One half of the memory is used to write the current frame and the other half is used to read the previous frame.

An overflow can occur at this level because the time needed to store the data coming from the 4 RRU in the SRU may exceed the available time. Indeed the integration window synchronisation and the token mechanism limit the number of available time to transfer the data between the RRU and the SRU. Due to the clock speed of 40 MHz and the 32 bits bus width to read and write the data, four 16-bits words could be transfer during one CLK half clock period (50 ns, if 40 MHz is used). The token mechanism need one period of the clock at 40 MHz to go through one RRU to the next one. For all the RRU the time needed for the token mechanism consume six 16-bits words (3 times two 16-bits words). The integration window synchronisation starts from the beginning of the DPEND and ends from the ending of DPTOKEN. Assuming that the lowest value of the sequencer configuration registers is the registers with the _A suffix (see MIMOSIS1 I²C controller document, section 6), the time needed for the integration window synchronisation is given by $((FRAMELENGTH - DPEND\_A + DPTOKEN\_B) \times 2 - 1) \times 2$. The recommended relative values of the sequencer leads to fourteen 16-bits words (see MIMOSIS1 I²C controller document, Table 27). Consequently, for an integration window of 5 µs the maximum number of 16-bits data words store in one SRU is 380.

2.2.4 Multiplexer

The Multiplexer distributes all the signals over the width of the sensor to read the RRU and SRU. The Super Region Unit memories are read serially starting from the Region with the lowest address (from left to right) using a token mechanism. Consequently all SRU without hit are skipped. Sixteen 16-bits data words from the SRU memory are read at the same time and send it to the Frame Generator to deals with the data bandwidth.

2.2.5 Frame Generator

The Frame Generator builds data frame from the sixteen 16-bits data words, remove the double 16-bits IDLE words and send eight 16-bits data words to the elastic buffer. A 16-bits IDLE words is a specific 16-bits data word inserted in the data flux when no data word is available (see MIMOSIS1 Data Format document). At the beginning of an integration window, it builds the header. At the end of an integration window, it builds the trailer. In case of overflow in the elastic buffer the Frame Generator suspend the writing in the elastic buffer up to the beginning of a new integration window. The rest of the data store in the SRU are lost.

2.2.6 Elastic Buffer

The Elastic Buffer works like a FIFO memory (First In First Out) of eight 16-bits data words for the input and the output. In case of 8 outputs sensor configuration the writing speed is 4 times large than the reading speed. In case of 1 outputs sensor configuration the writing speed is 32 times larger than the reading speed. The Elatsic Buffer can store 32768 16-bits words. If the Elastic Buffer is empty or waiting to complete the trailer, IDLE words (specific word set to FCAA, see MIMOSIS1 Data Format document) are sent to the output stage in order to maintain an activity on the serial link.

The overflow of the Elastic Buffer is managed by two parameters the BANDWIDTH and the FILLLEVEL. The FILLLEVEL parameter activates the limitation of bandwidth if the the remaning 16-bits words inside the elastic buffer is larger than this value at the beginning of an integration window. The default value is set to 100. The BANDWIDTH parameter ensure that the number of written 16-bits words in the Elastic Buffer which will be read later in a time smaller than the integration window. Due to the synchronisation of integration window the value of BANDWIDTH is given by :

$$BANDWIDTH = 8\left(\frac{FRAMELENGTH}{8} \times 2^{OUTPUTMODE} - 5\right)$$

With FRAMELENGTH express in CLK half clock period (the same value as put in the register). For an integration window of 5 µs the value of BANDWIDTH is set automatically in function of OUTPUTMODE which is set by pads or by I²C (see MIMOSIS1 I²C controller document, section 4.13).

2.2.7 Output Stage

The output stage serializes the eight 16-bits data words through a number of serializers depending of the number of outputs set by OUTPUTMODE. The number of outputs and serializers is equal to $2^{\text{OUTPUTMODE}}$. The output speed of the serializer are set to 8 times the input clock (320 MHz with a 40 MHz input clock). The output stage also detects the header inside the data (based on 8 HEADER words, see MIMOSIS1 Data Format document) and send an optional synchronisation signal on DATAMARKER pads. The output stage generates the optional CLKSER signal which can be used to sample the DATA pads in a double data rate.

2.2.8 Readout patterns injection

To test the readout, patterns could be injected at three different levels:

- Pixels level in digital or analogue mode
- Region readout unit input
- Output Stage input

2.2.8.1 Pixel pattern injection

A one bit memory is located in each pixel and can be write with I²C transaction. This memory is used to mask or to configure the injection of each pixel. When the chip is in the injection mode, which is set by EN_PIXELMASK bit in RUNMODE register (see MIMOSIS1 I²C controller document, section 4.1), an analogue or a digital pulse can be sent to the pixel (see section 2.2.1) through the PIXPULSEA or PIXPULSED sequencer signals (see MIMOSIS1 I²C controller document, section 6).

The in-pixel memory is selected through a row and a column enables. When both enables are selected the in-pixel memory store the value given by MASK_PULSE_DATA bit. A detailed description is given in MIMOSIS1 I²C controller document, section 7.

To limit the perturbations induced by the PIXPULSEA or PIXPULSED send to the whole pixel array a gating mechanism to limit the pulsing of selected columns according to the selected pixel is implemented. There is no automatic implementation of this mechanism and the pulse gating must be configured separately by I²C. A detailed description of the configuration is given in MIMOSIS1 I²C controller document, section 7.

2.2.8.2 Region Readout Unit pattern injection

To test the readout from the input of a the RRU up to the the outputs pads, a blocks called Data Generator for Multi-Frame Emmulation (DGMFPE) generating 16-bits words is inserted in each RRU. It works with the Multi-Frame Emmulation (MFE) blocks wich generates 64 signals to enable the data generations of DGMFPE. These enable signals are programmable by I²C based on a 8 frames period. For each region and for each frame the duration of the enable signal is express in number of 16-bits words send to the RRU. Every 8 frames the sequence is repeated. Consequently, an arbitray number of hit could be emulated for each region and for each frame over a set of 8 frames. See MIMOSIS1 I²C controller document, section 9, to have the full description of the programation of the MFE.

2.2.8.3 Output Stage pattern injection

To test the Output Stage a 128-bits wide pattern could be injected at the input. The 128-bits pattern is serialized and send through the number of pads selected with OUTPUTMODE, indefinitly. If the pattern match a HEADER word (see MIMOSIS1 Data Format document) the optional synchronisation signal on DATAMARKER pads is generated. See MIMOSIS1 I²C controller document, section 11, to have the description of the configuration of this pattern.

2.2.9 Analogue pixel outputs

The first row of the matrix could be read through two analogue outputs pads called ANAOUT. ANAOUT[0] is connected to the output of the amplifier and ANAOUT[1] is connected to the output of the discriminator. To select the pixel which is conncted to the outputs pads, a 16-bits register called SEL_ANAPIX is programmable by I²C. If the value of this register is set to a value different of 0, the pixel located at the column address SEL_ANAPIX-1 is connect to the pads. If the register is set to 0 none of the pixels are connected. The pads ANACOLBIAS[0:1] and ANAOUTBIAS[0:1] are current bias pads for the buffers used in the analogue readout. See MIMOSIS1 I²C controller document, section 10, to have the description the analog pixel selection.

2.3 DAC description

2.4 Sequencer description

2.5 Clocks generation description

This section describes the clocks generation inside MIMOSIS1. It generates the 5 clocks needed to run the readout part of MIMOSIS1, the optional output clock for serialization and the clock to refresh the hamming registers. The clock for the I²C is directly connected to the external CLK pad. The clocks generator could be divided in 3 parts:

- The gen_clock_master which selects the clock source for the main clock and generates a synchronization signal allowing the clocks alignement for several MIMOSIS1;
- The gen_clock_main which generates 3 of the readout clock needed by MIMOSIS1 and the clock to refresh the hamming registers;
- The gen_clock_ser which generates the clock for the serialization and the optional output clock for serialization.

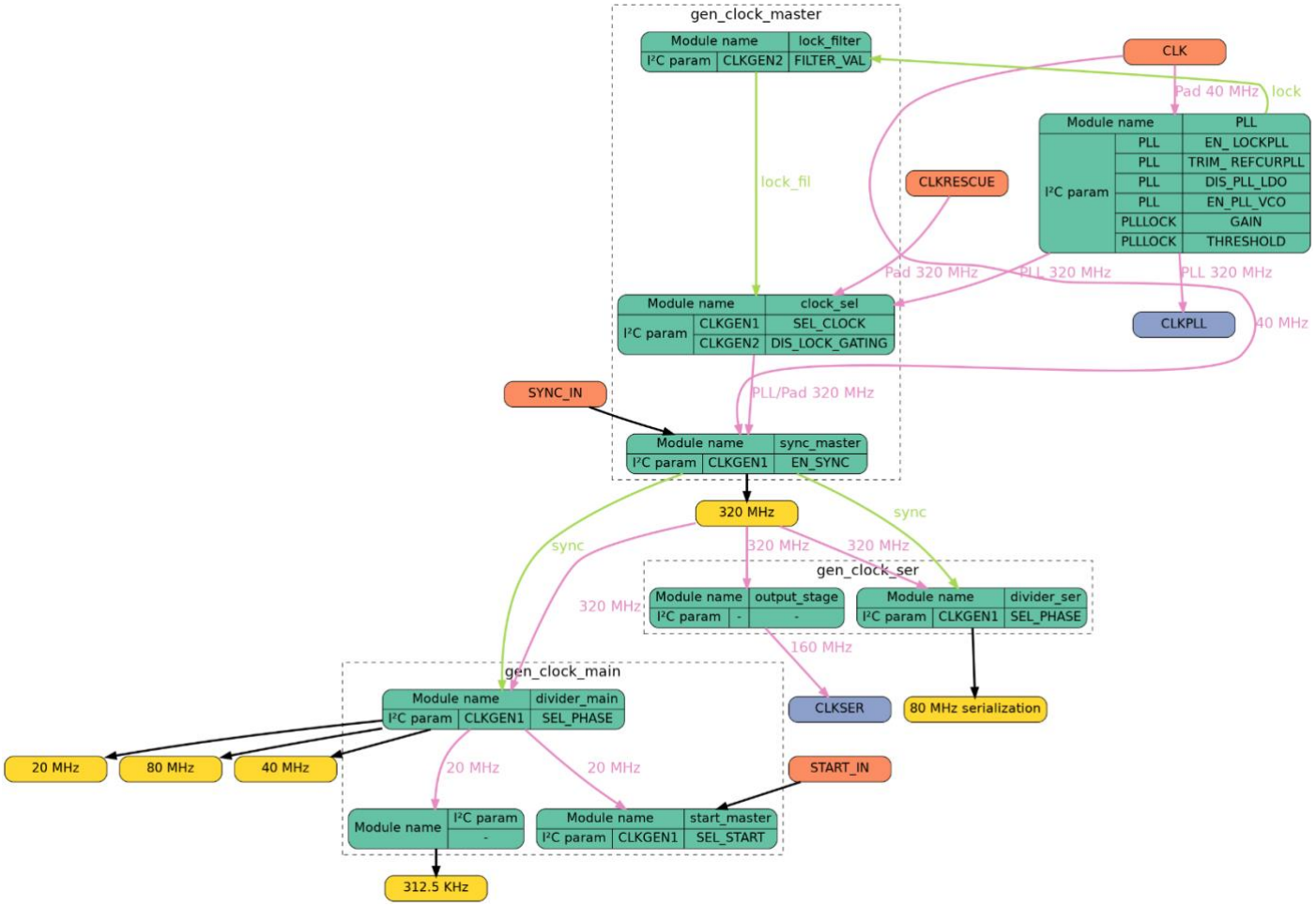


Figure 3: Clocks generation blocs diagram

2.5.1 gen_clock_master description

This part generate the main clock which all the other clocks are derivated and is composed of 3 modules:

- The clock_sel which select the source to generate the main clock
- The lock_filter which filter the lock flag from the PLL
- The sync_master which generates a synchronous signal over several MIMOSIS1

2.5.1.1 clock_sel description

This module select as a source the 320 MHz clock from the PLL or the 320 MHz from the CLKRESCUE pad through I²C with the bit SEL_CLOCK from the CLKGEN1 configuration register. When the PLL is the selected source the output clock could be gated with lock signal coming from the PLL to avoid the generation of clocks before the locking of the PLL. This gating could be disable through I²C with the bit DIS_LOCK_GATING from the CLKGEN2 configuration register.

2.5.1.2 lock_filter description

This module filter the glitches of the lock flag from the PLL to avoid loss of clock at the output of the clock_sel when the gating is enabled. The glitches larger than the value of FILTER_VAL times the period of the CLK signal are removed. The FILTER_VAL is programmable through I²C with the 4 bits FILTER_VAL from the CLKGEN2 configuration register.

2.5.1.3 sync_master description

The output of this module is the main 320 MHz clock which is used to generates all the other clocks for the readout of MIMOSIS1. It uses a external signal SYNC_IN as a synchronous reset to ensure the launch of all the generated clocks to be synchronous over several MIMOSIS1. When the SYNC_IN signal is set to 1 the output clock is forced to 0. On the falling edge of the SYNC_IN signal the synchronization is started. First, the SYNC_IN signal is latch on the falling edge of the 40 MHz clock provided by the CLK pad. Then, this synchronous SYNC_IN is latch with the 320 MHz clock coming from the clock_sel module. After, one period and a half of the 40 MHz clock, the 320 MHz output clock is started. To ensure a proper synchronization between several MIMOSIS1, the external SYNC_IN signal must be generated on a rising edge of the 40 MHz clock. The chip MIMOSIS1 need also to be set in automatic start (see section), and the finit state machines of the readout must be reset when SYNC_IN is set to 1 by sending C1 to the INSTR CMDID (see MIMOSIS1 I²C controller document, section 2.2).

2.6 VT Monitors description

2.7 I²C controller description

3 Physical arrangement

MIMOSIS1 sensor has a size of 31.1 mm by 17.2 mm and is composed of a pixel array of 1024 columns by 504 rows.

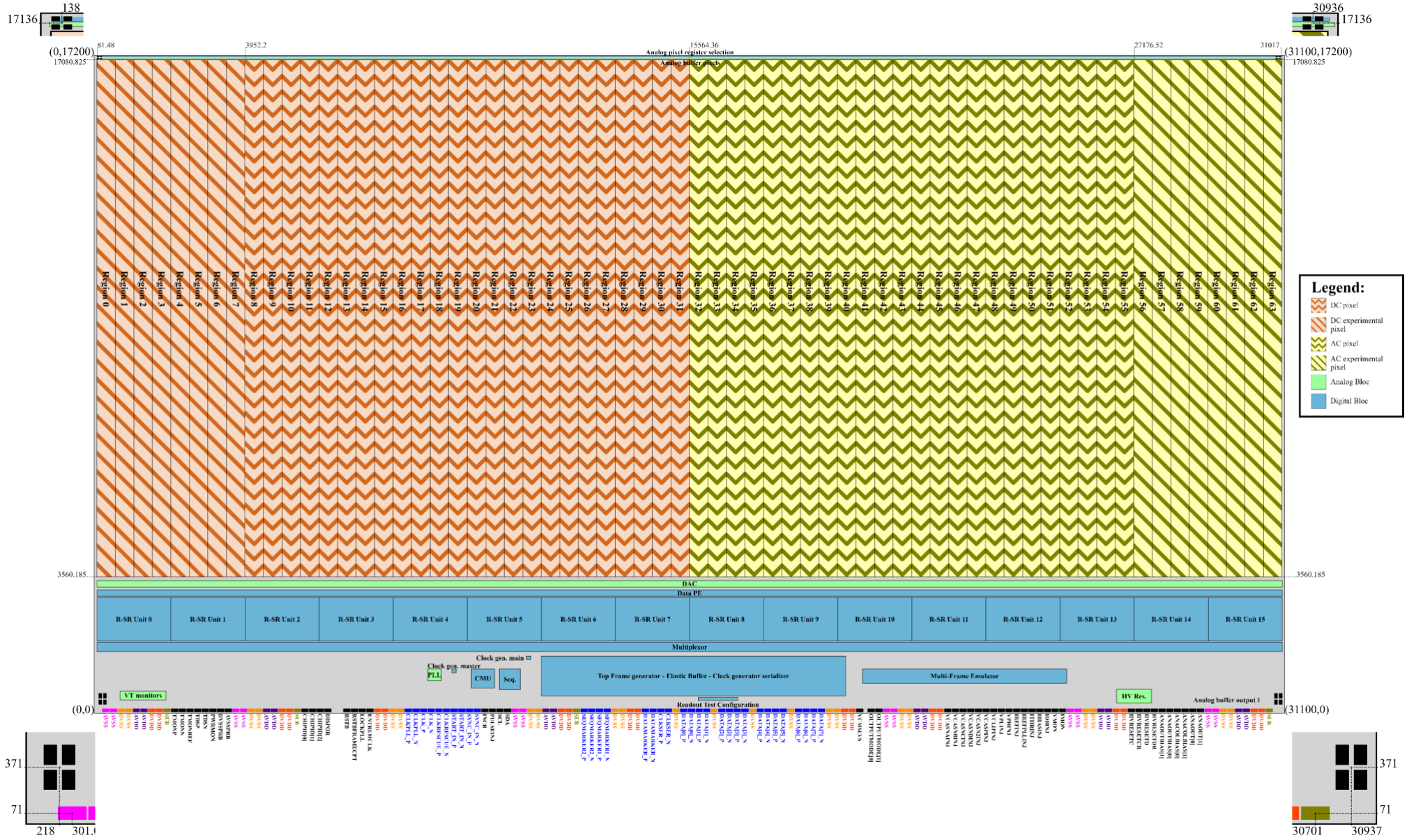


Figure 4: MIMOSIS1 physical arrangement