Contribution ID: **323** Type: **Presentazione orale**

Exploring Novel Neuromorphic Computing Architectures with a Multi-Node FPGA System

Thursday, 29 May 2025 11:30 (15 minutes)

Brain-inspired Spiking Neural Networks represent a promising frontier in computational models, offering potential advantages over traditional computing paradigms in terms of energy efficiency, temporal information processing, and adaptability to dynamic data. This can benefit numerous applications, such as real-time signal processing and pattern recognition in resource-constrained environments. Neuromorphic computing is an approach to hardware architecture design to efficiently implement these biologically-inspired networks, balancing biological plausibility against computational efficiency.

This presentation describes a new multi-core neuromorphic architecture prototype that is under development within the INFN Brainstain project, bringing together the diverse expertise present inside CSN5, from computational neuroscience to the design and implementation of high performance computing architectures dedicated to physics tasks.

Leveraging on the proprietary APEIRON framework for flexible, low latency communication we aim to deploy our architecture prototype on a multi-FPGA system, adopting a software-hardware codesign workflow that relies on the High Level Synthesis (HLS) programming paradigm for relatively fast and simple translation from a high level simulator of the architecture to the hardware design. Flexibility and modularity will allow us to explore support for different models of neuron dynamics, such as multi-compartment neuron models, and study the system performance with different inter-core communication schemes, and with different AI applications.

This presentation will discuss our architectural approach, the current and planned features of the system, the status of the project and an outline of its future direction.

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Session Classification: Intelligenza artificiale

Track Classification: Intelligenza Artificiale