

Microfabrication platforms at TIFPA

Overlap Josephson junctions and high kinetic inductance circuits

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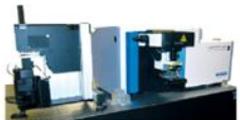
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Micro and Nano fabrication Facility @ FBK

clean room area moving to >2000m²



6" Microfabrication Area

Clean Room Detectors

700 m²; Class 10/100 0,8 um CMOS pilot line: Ion Implantation, Oxidation, Diffusion, RIE, Deep RIE (silicon and oxide), Lithography (**stepper 0.35 um** and **mask aligner**), metal sputtering, optical profilometry

Clean Room MEMS

500 m² Class 100/1000 diffusion, lithography (**mask aligner**), wafer bonding, electroplating, Si bulk micromachining, metal evaporation, RIE, mechanical and optical profilometry,

3D Integration Clean Room

200 m² Class 10/100 wafer temporary bonding/debonding, metal&fusion direct bonding, grinding&polishing, metrology for 3D stacked wafers, ALD.

Testing Area

300 m² manual parametric testing, automatic parametric/functional testing, optical testing (spectral responsivity, quantum efficiency), solar cells efficiency characterization, gas and pressure sensors test benches

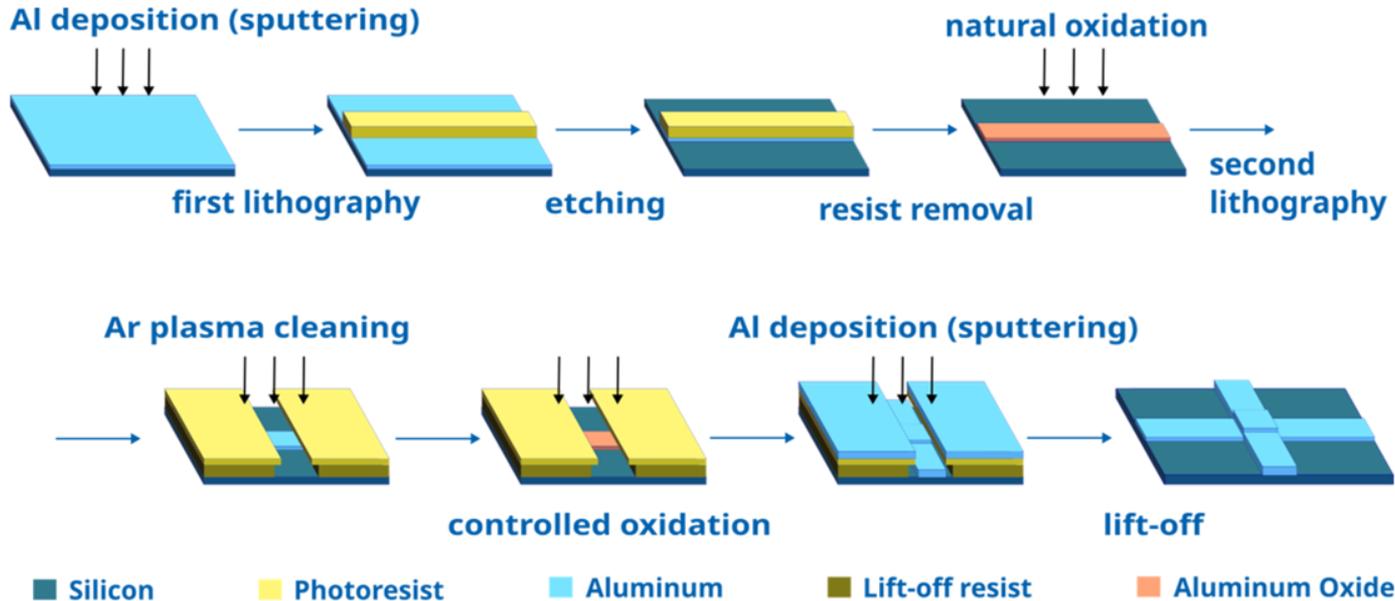
Integration Area

100 m² clean room Class 1000 Microassembly station; screen printing, bonding (ball & wedge bonder), Shear-Pull Tester, reflow oven, CNC micro-mill, pick and place

Nano- and Micro- Analytical Facility

Nano Raman, FIB-SEM-EDX-EBSD, D-SIMS, TOF-SIMS, XPS, AFS, XRD/XRF

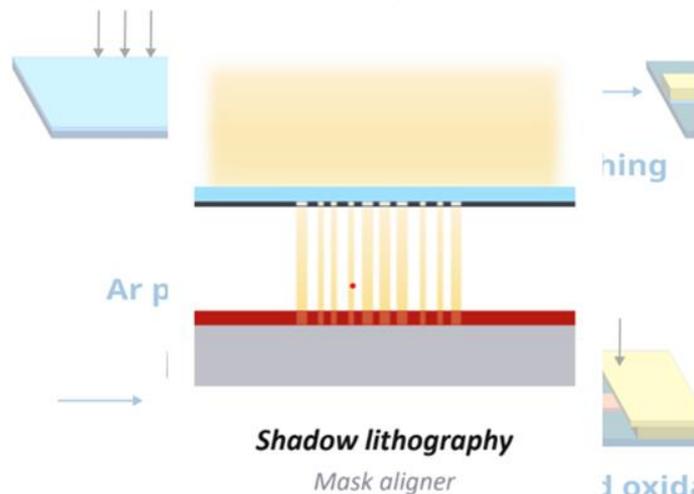
Fabrication process (for Josephson junctions)



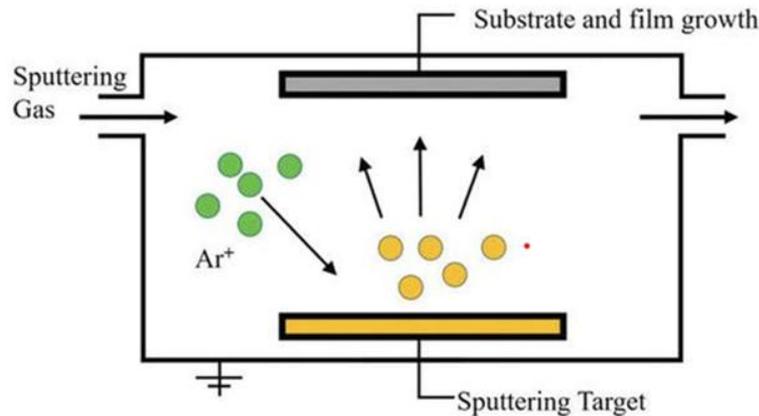
- Optical lithography
UV light mask aligner
- Etching
Al-selective acids bath
- Sputtering
DC Magnetron @ RT
- Lift-off
Lift-off resist-selective solvent bath

Fabrication process

Al deposition (sputtering)



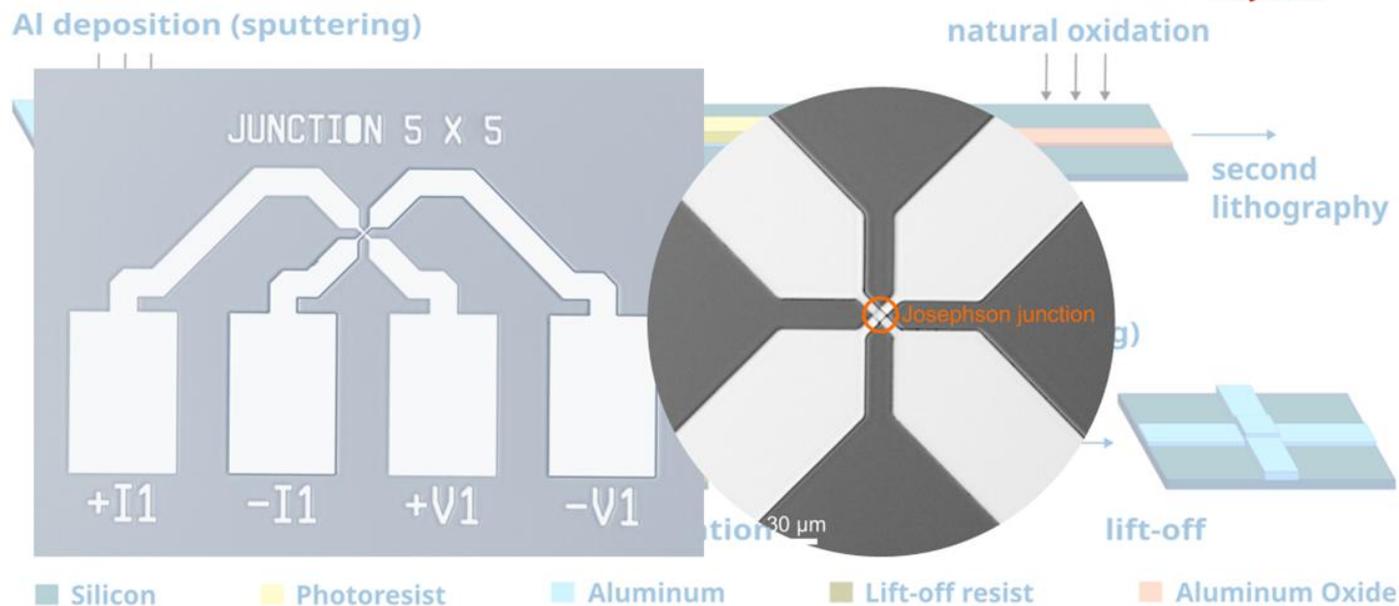
natural oxidation



■ Silicon ■ Photoresist ■ Aluminum ■ Lift-off resist ■ Aluminum Oxide

- Optical lithography
UV light mask aligner
- Etching
Al-selective acids bath
- Sputtering
DC Magnetron @ RT
- Lift-off
Lift-off resist-selective solvent bath

Fabrication process

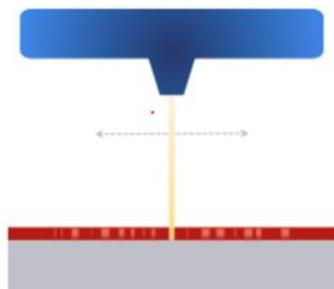


Different from Dolan style!!!

talks by [F. Ahrens](#) in [WP5](#) and [N. Crescini](#) in [WP6](#) to know about some devices we designed, realized and measured in our lab in Trento

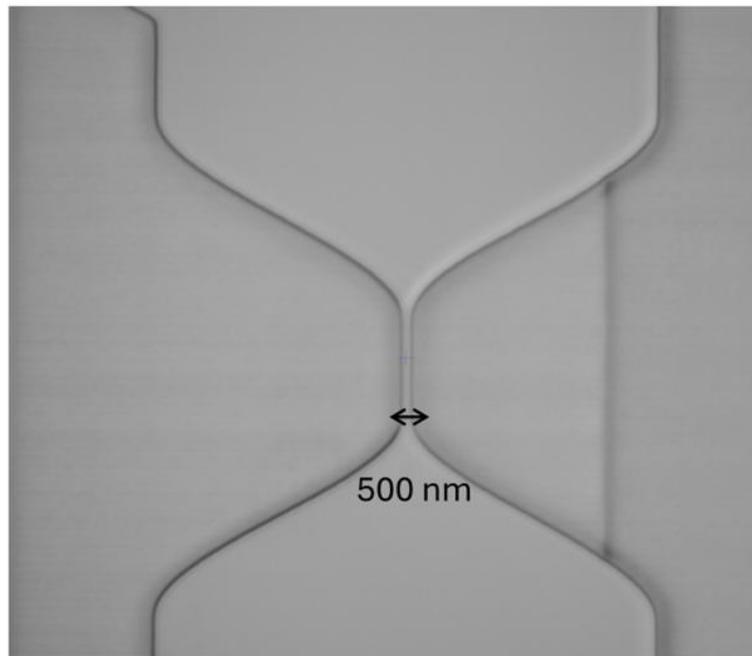
Fabrication process

what's next??



Direct lithography
Laser writer

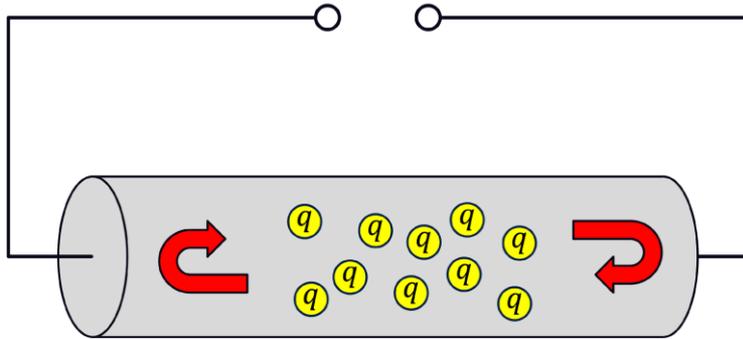
Next weeks/months



A possible future alternative can be **EBL**

Kinetic inductance non-linearity

$$U = U_0 e^{i\omega t}$$



$$\Rightarrow L(I) \approx L_0 \cdot \left(1 + \frac{I^2}{I_*^2} \right)$$

$L_0 = \frac{R_S \hbar}{\pi \Delta}$

$I_* \propto 1/\sqrt{R_n}$

Material with high kinetic inductance

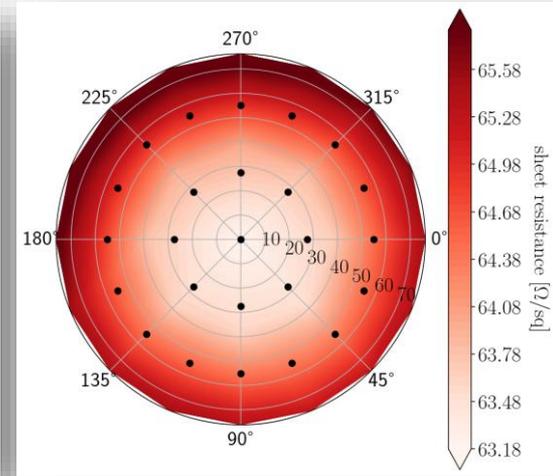
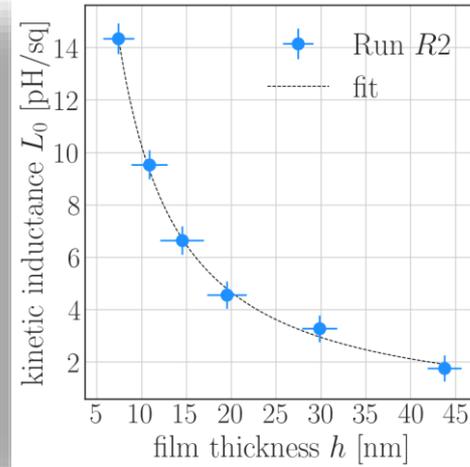
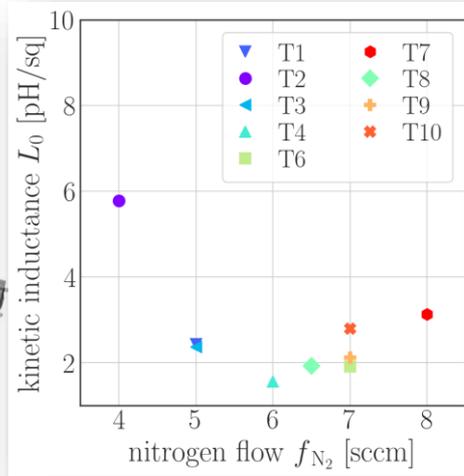
\Rightarrow high-resistivity superconductors

NbN, NbTiN, TiN

NbTiN Film Deposition Optimisation

Sputter target: $L_0 = \frac{R_S \cdot \hbar}{\pi \cdot T_C \cdot k_B \cdot 1.762}$

Nb_{80%}Ti_{20%}

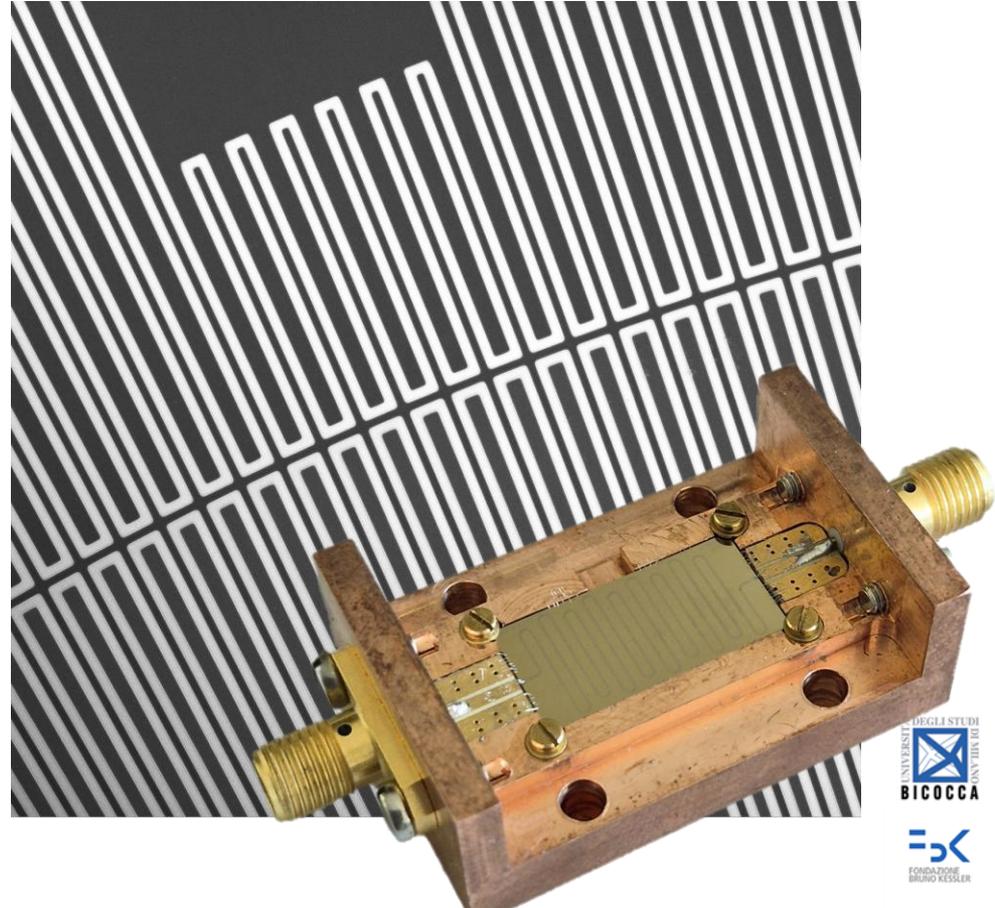
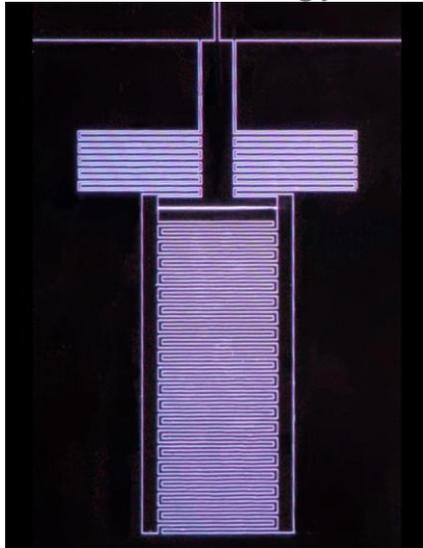


Kinetic inductance devices

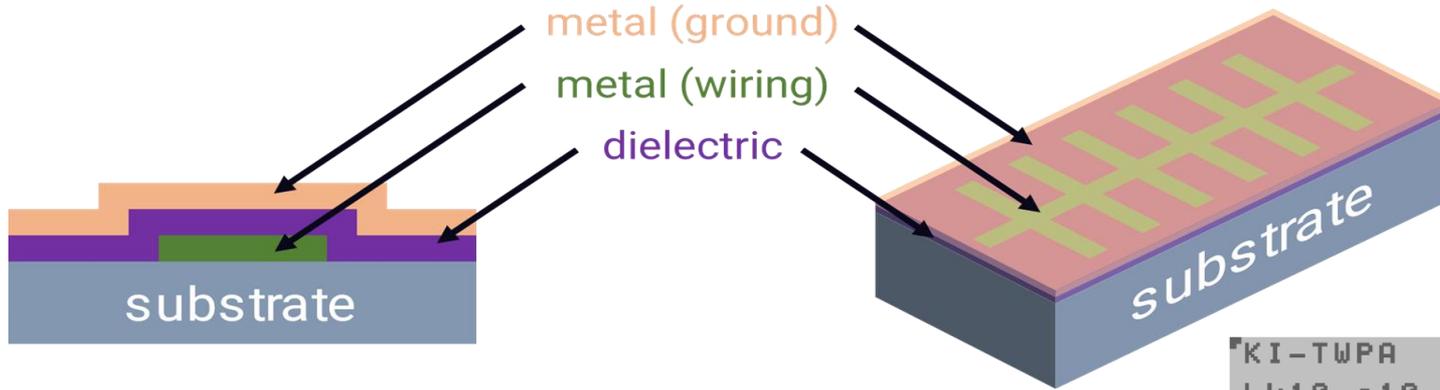
- Tunable resonator
- Traveling Wave Parametric Amplifier
- Traveling Wave Photon Energy Lifter



Talk in **WP5** by
F. Ahrens

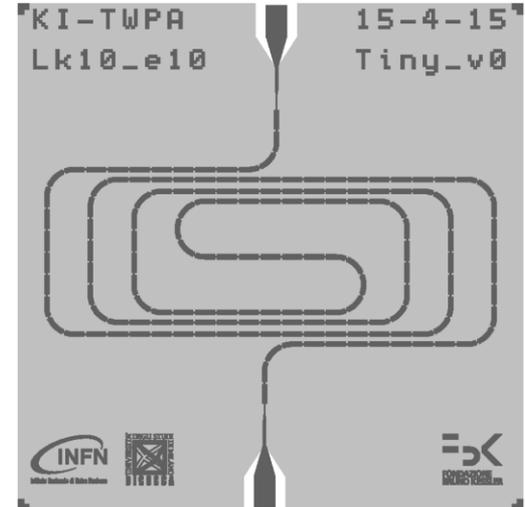


Next step: Inverted Microstrip geometry

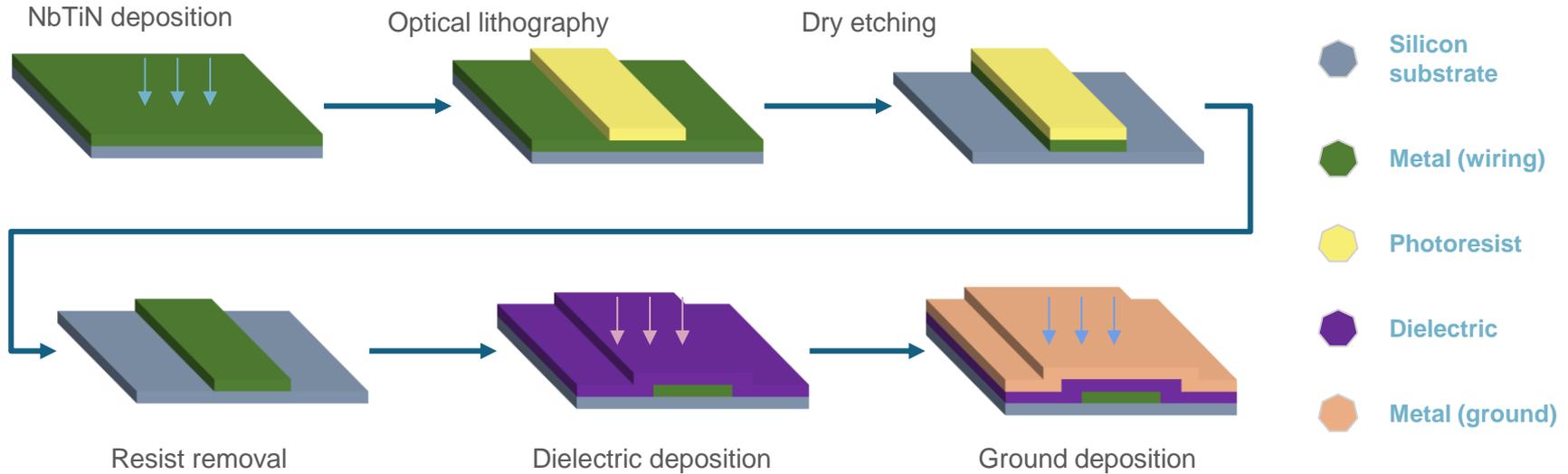


Advantages:

- More **compact** design
- Improved **grounding**
- High fabrication **yield**



Fabrication process



Challenges:

- Development of **low-loss dielectric**
 - PECVD/ICP-CVD **a-Si**
 - ALD **Al₂O₃**
- **Increase** sheet kinetic **inductance**