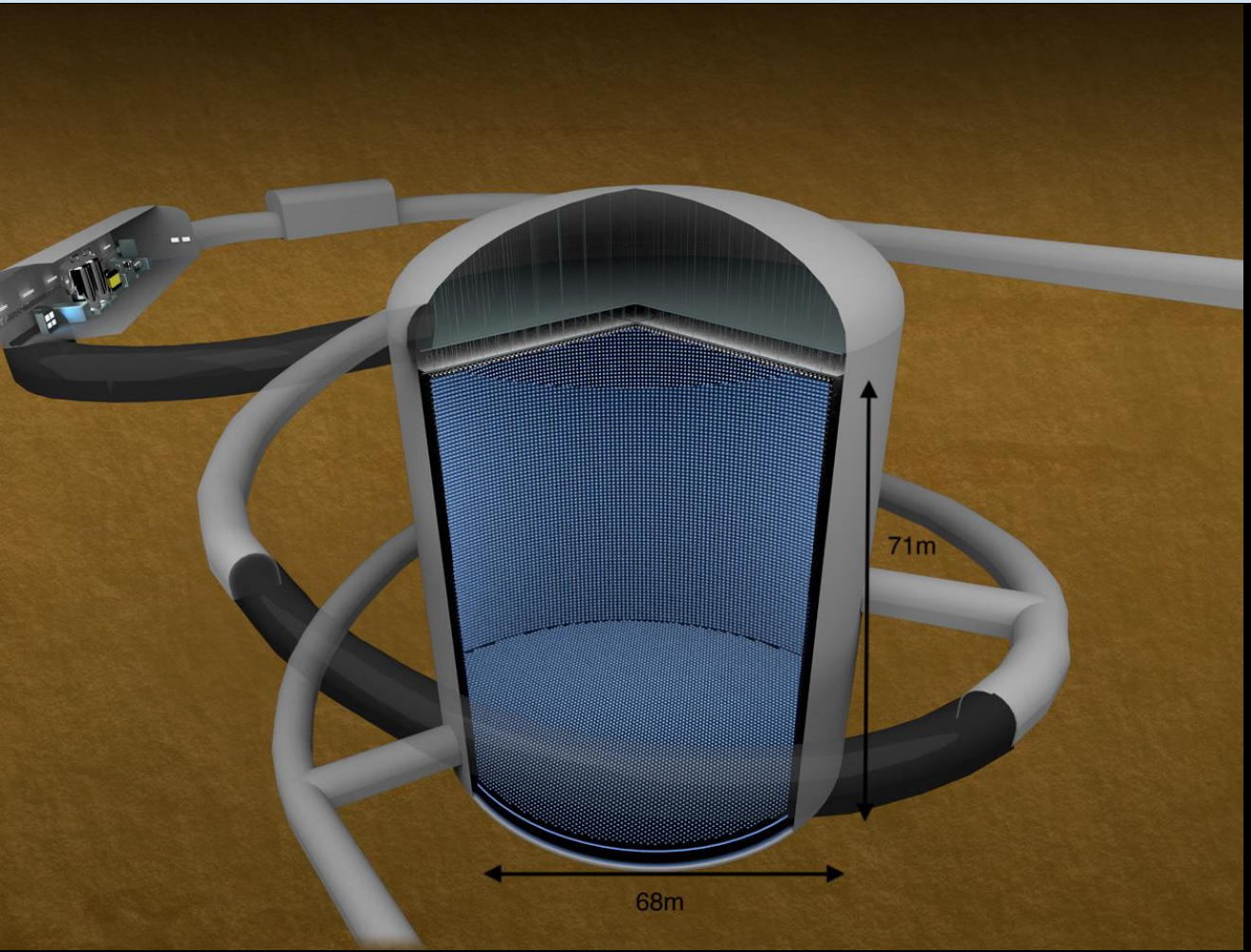
JENNIFER 2
EU grant n.822070

Hyper-Kamiokande



Hyper-K Underwater Electronics

Stefano russo

Jennifer2 Meeting

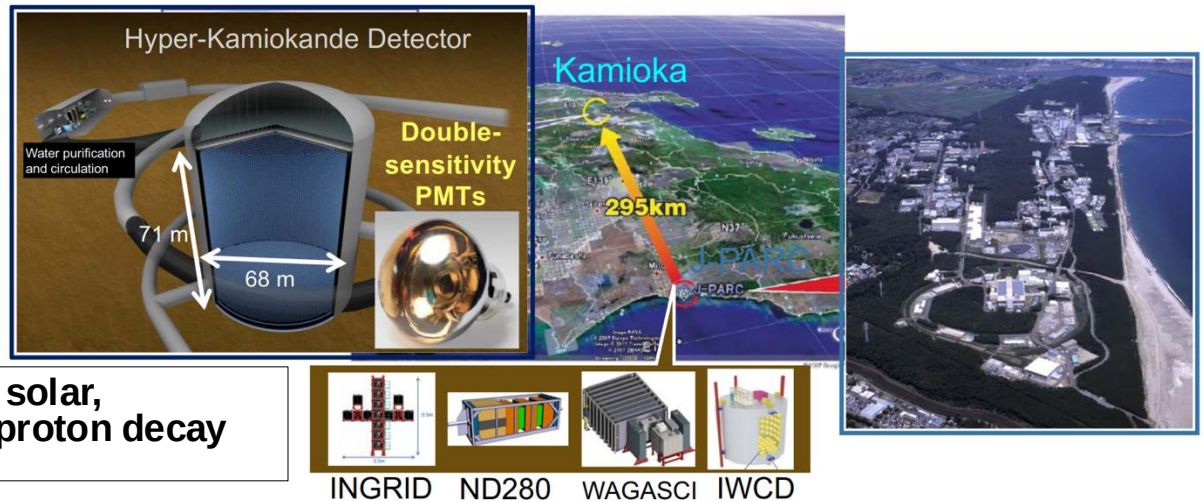
Pisa - 04/4/2025

On behalf of: F.Ameli, A.Di Nola, L.Ludovici and J. Pinzino

Thanks : FD4,FD2 HK WG

Hyper-K in a nutshell

Hyper-K water Cherenkov at Kamioka (host U-Tokyo)



High intensity proton beam at JPARC (host KEK)

Accelerator, atmospheric, solar, supernova neutrinos and proton decay

- **World largest detector for nucleon decay and neutrino experiment**
  - 8.4 times larger fiducial mass (188kt) than Super-K, with new photo-sensors: twice-as-sensitive 20‘‘ PMTs and new multi-PMTs
- **World most intense neutrino beam**
  - 2.6 higher JPARC beam intensity (1.3MW) than T2K 2020 (~500kW); T2K 2024: 800kW
- **New (IWCD) and upgraded (ND280) near detectors to control systematic errors**

Underwater electronics vessels

Underwater system (France, Italy, Japan, Korea, Poland, Spain, Switzerland, UK)

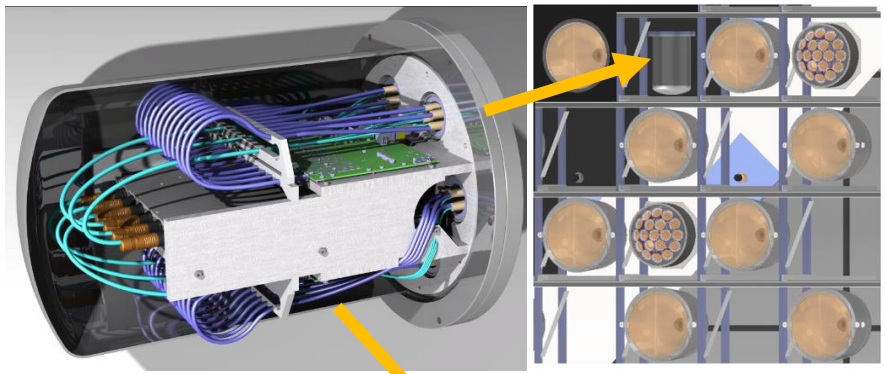
- Front-end digitizers (OD:)
- On-board calibrator
- Data Processing Board
- Timing/Synchronization
- HV, LV power supplies (CAEN)
- Pressure tolerant cases
- Cables, feedthroughs, optical fibres (shared)

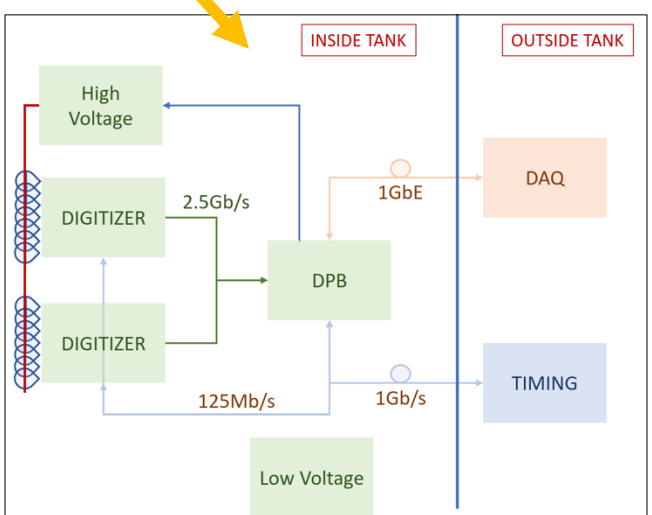
Out-of-water system

- DAQ
- Timing/Clock gener.&distrib.
- Infrastructure (huts, air conditioning, cable trays,…)

System tests, pre-calibration, and assembly (shared)

Installation, test, calibration (shared)





20’’ PMTs front-end digitizer selection

Electronics in water: low noise, low power, high dynamic range

In 2019 (Jennifer 2 Technical Report) there were already competing design:

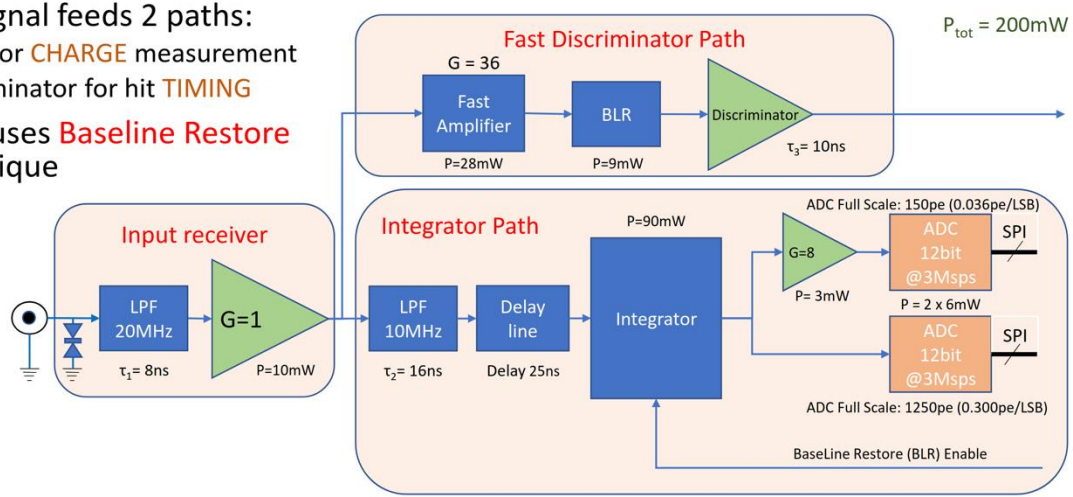
- QTC, an old ASIC developed for SK (Japan)
- Capacitive arrays (out-of-the-water ?)
- HKROC, a new ASIC developed for HK (France, OMEGA)
- → INFN proposal based on discrete components

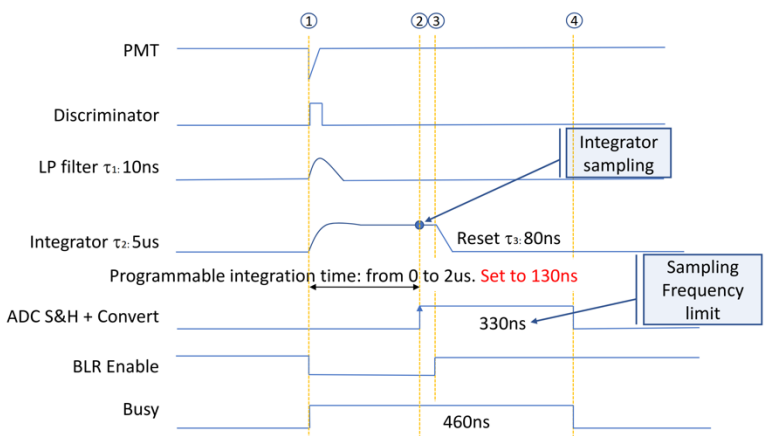
May 2020	Start design and simulation of a front-end based on discrete components, leveraging the experience with the mPMTs electronics design
Jun 2020	Proposal to the Collaboration
Sep 2020	Single channel prototype V1.0
Jan 2022	Single channel prototype V1.3 and 24 channel board (digitizer+DPB)
Jun 2022	Complete characterization of the board performance (TechNote for the technology selection review)
Sep 2022	Selection of INFN proposal (second half of Jennifer 2)

Front-end digitizer

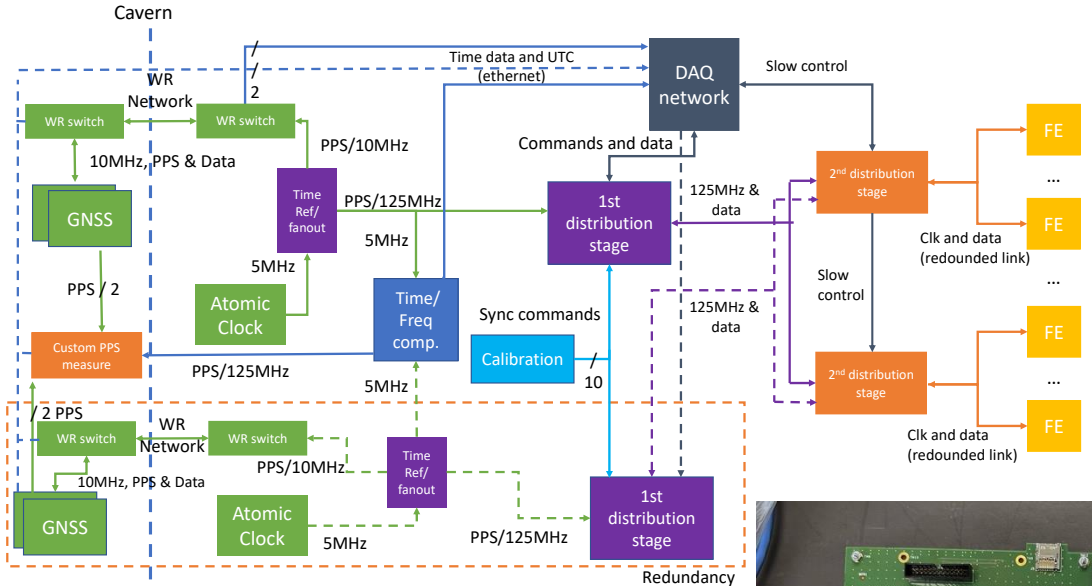
Item	Requirements	Performance obtained	Section of document
Trigger	self triggering for each channel	OK	3.1
Signal reflection	<1%	<1% up to 75 MHz	4.6
Discriminator threshold	1/6 pe	0.08 pe with « 1 Hz noise	4.2
Processing speed/hit	<1 μs	~ 450 ns	3.1
Maximum hit rate	>1 MHz per channel	~ 2 MHz	3.1
Charge dynamic range	0.1 to 1250 p.e. (0.19 to 2375 pC)	0.1 to 1300 pe (adaptable with one resistor modification)	4.4
Charge resolution (RMS)	< 0.1 pe for signals below 10 pe < 1 % for signals from 10 pe	0.08 pe at 1 pe 1.1% at 10 pe, less for bigger signal	4.5 4.4
Timing LSB	<0.5 ns	0.25 ns (same TDC as QTC)	3.1
Timing resolution (RMS)	<0.3 ns at 1 p.e. <0.2 ns for signals above 5 p.e.	210 ps at 1 pe ~170 ps at 5 pe	4.10 4.10
Power consumption	<1 W per channel	0.2 W per channel (analog FE), total <400 mW per channel	3.2

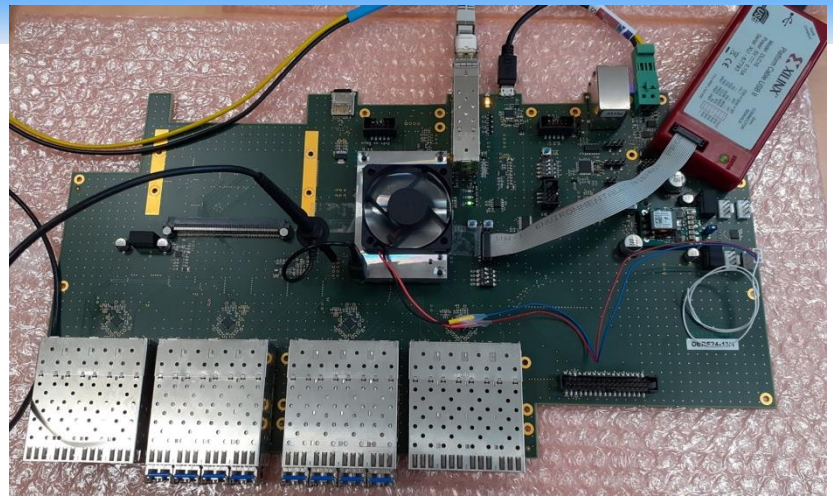
- PMT input signal feeds 2 paths:
  - Integrator for CHARGE measurement
  - Fast Discriminator for hit TIMING
- Final design uses Baseline Restore Enable technique



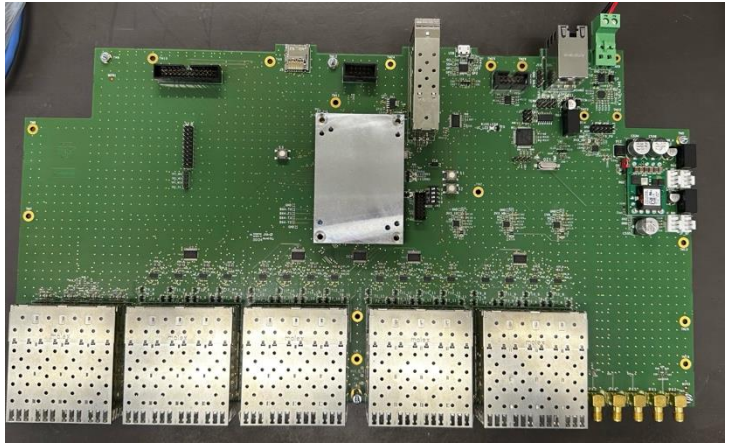


Time Distribution System



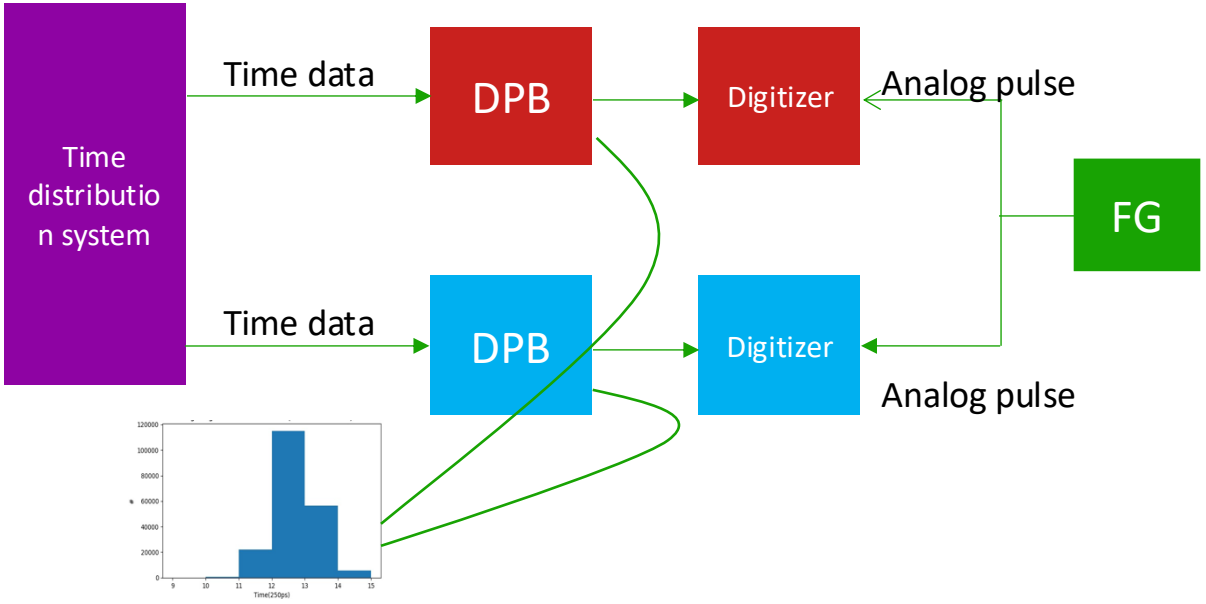


1st distribution stage

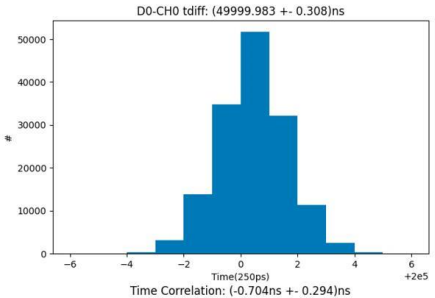


2nd distribution stage

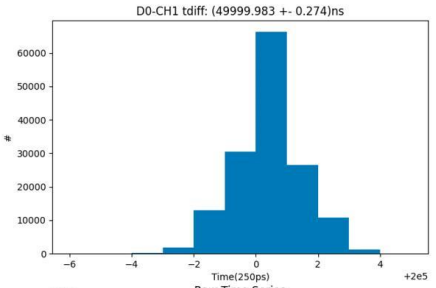
Timing synchronization test

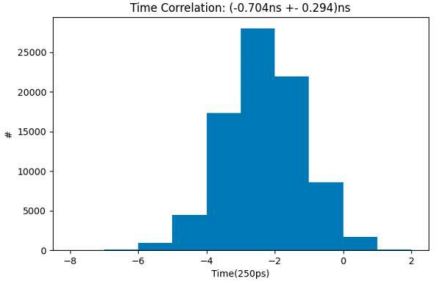


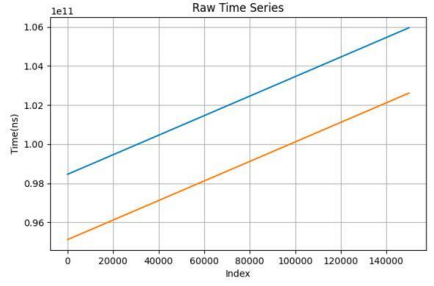
Time stamp Dig-1



Time stamp Dig-2







Time stamp difference

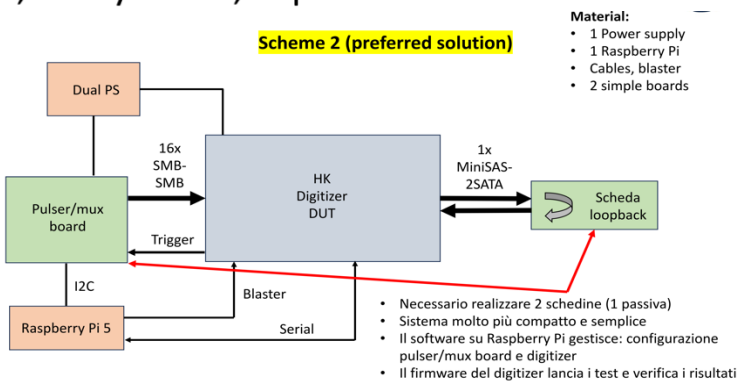
The two time-stamps differ by a mean value of 0.7 ns and the distribution sigma is 294 ps which is coherent with the TDC resolution.

Same results after TDM and DPB reboot.

Frontend board tests at production company

Testbench for early board-screening during production

- TB is aimed to assess Digitizer functionalities at production company premises.
  - TB consists of HW, SW, and FW components
- The task should be accomplished in the simplest possible way, limiting number of connections and external boards
  - Performance assessment will be implemented at CERN, before integration
- 2 possible options:
  - Using as much as possible commercial products and HK boards: complex, many items, expensive
  - Self-made, with fewer items though with custom designed test boards
- Required items:
  - HW: Function Generator, Testbench PC, Cables, Support Boards, …
  - SW: PC code to handle board tests
  - FW: custom FPGA code which implements Built In Self Test

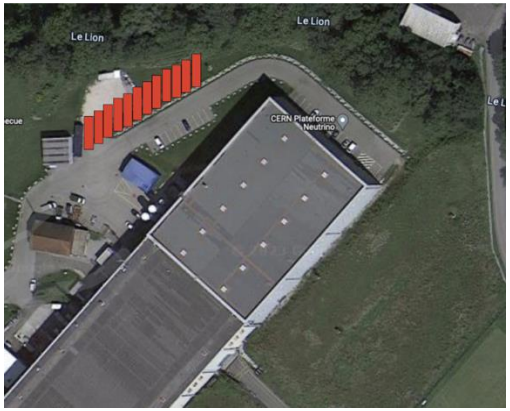


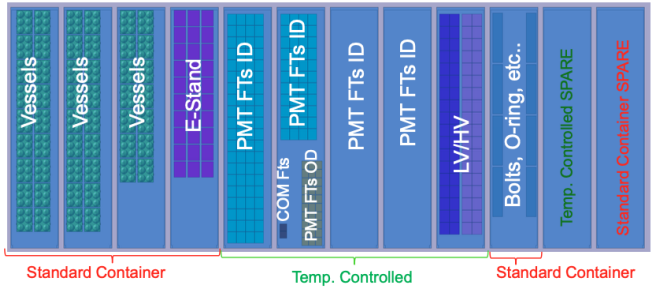
1. QC&QA, functional tests, burn-in at production companies

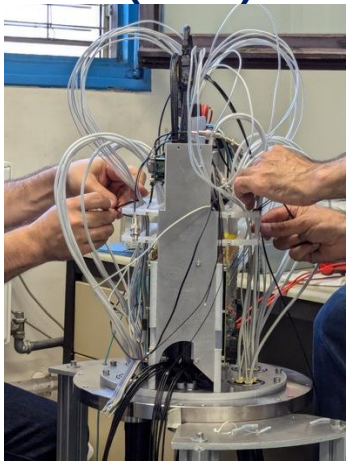
2. Calibration (digitizers) and underwater vessels integration and tests, at CERN

Underwater vessels assembly at CERN / NP08

- LoI submitted (CERN-SPSC-2023-021) in Aug.2023, Addendum (CERN-SPSC-2024-04) Jan.2024
  - **As it is not an experiment, no need for a proposal or a formal SPSC approval**
  - **After meeting with CERN Research Director it was informally agreed that the electronics assembly project will be hosted by the CERN Neutrino Platform (NP08)**







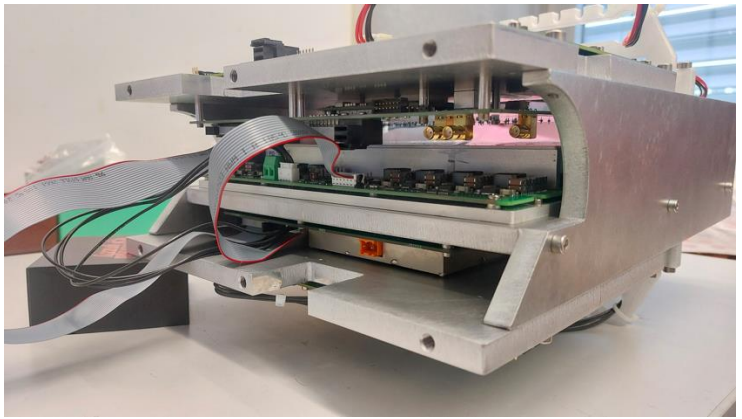
- 12 40-ft containers placed near EHN1 (Neutrino Platform) to store components
- Assembly and storage of assembled units in EHN1 (crane available for truck loading)
- After functional test and burn-in at production company, boards delivered at CERN for calibration (digitizer) and integration in the underwater vessels
- 4-6 underwater vessels will be assembled per day by 8 workers, for a total of 900 vessels
- Functional and pressure test of the assembled vessels

First electronics underwater vessel assembly

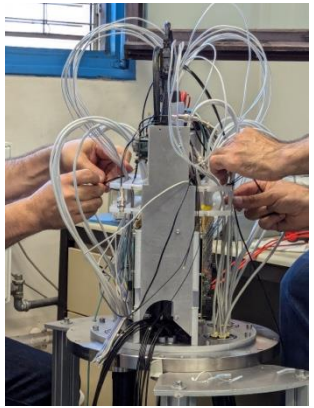
Assembly of underwater vessel

Components:

- Patched DPB
- LV and HV boards
- Two Digitizer boards
- AXON FTs
- Com FT (150 m long cable/fibers)



Boards on the electronics stand

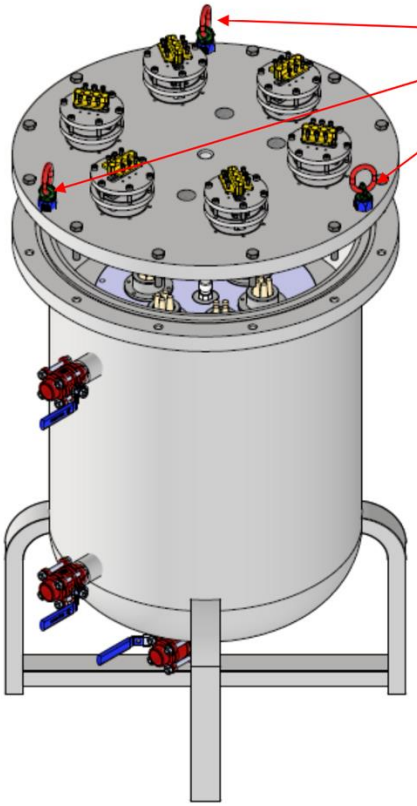


Electronics stand assembly

- Assembly of the board on the electrics stand finalized
- Vessels assembled at CERN and Japan: finalize procedure
- Electrical connections and fiber communications established
- Final test on the electrical stand
- Closure of the vessel:
  - Silica bags,
  - Nitrogen flushing,
  - Saving temperature and humidity before, during and after closure of the vessel.
- Immerse the vessel into the water tank,
- Data are saved into local database

Electronic vessels at the under water test facility at CERN

Underwater vessels pressure test

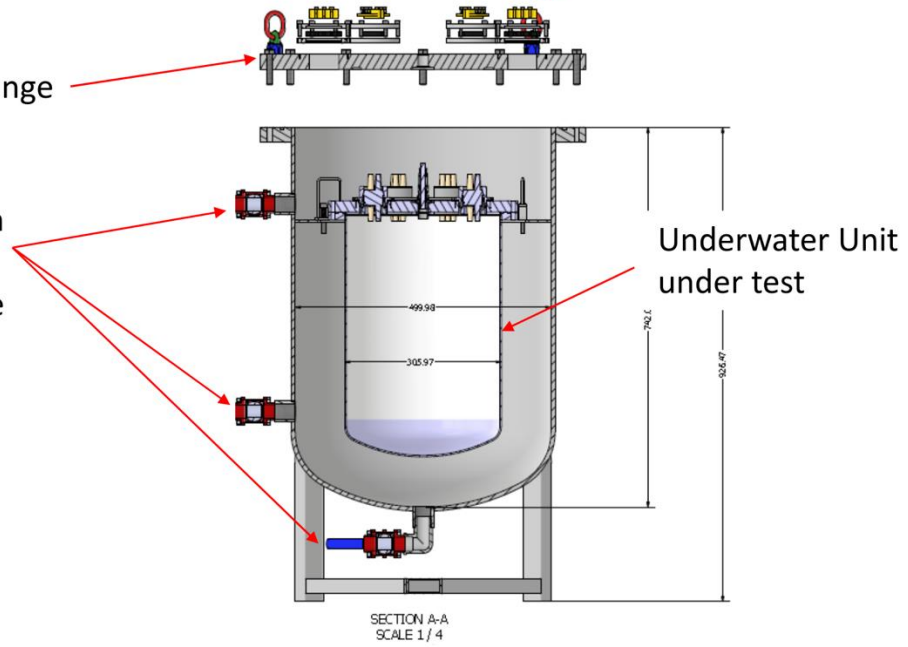


Lifting system
for the main flange

Feedthrough
system

main flange

Water filling and
evacuation system
(plus dedicated
inlet/outlet on the
main flange)



Approximatively: 1 meter h x 0.5 m w , 150 liters of water

Long term underwater tests

Former WA105 cryostat in b182 at CERN repurposed as underwater electronics test facility

Submerging up to 10 modules at the same time

Heat dissipation model. Thermal contacts validation. Heat budget

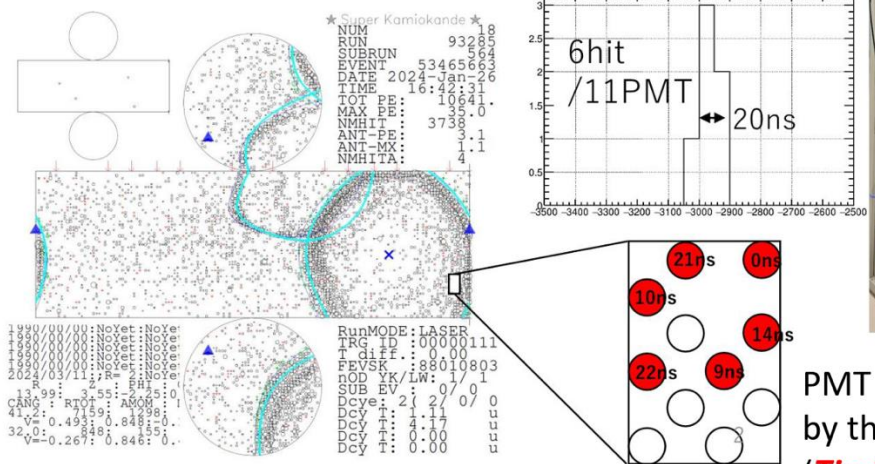
On-going underwater vessel tests and plan long term test (1 years) during mass production

HK Digitizer tests in Super-Kamiokande

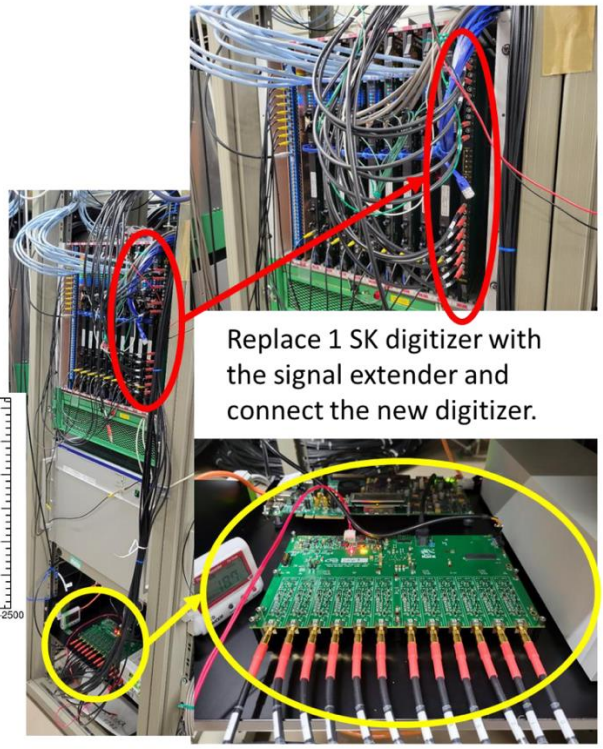
Digitizer performance check
(Stand alone, before assembly)

Collected SK & HK PMT data using the HK digitizer.

Atmospheric neutrino candidate events were recorded using the HK electronics.



PMT hits observed
by the SK electronics



PMT hits observed
by the HK electronics.
(***Timing adjustment is very rough.***
No calibrations are applied.)

Multi-PMT Optical Module

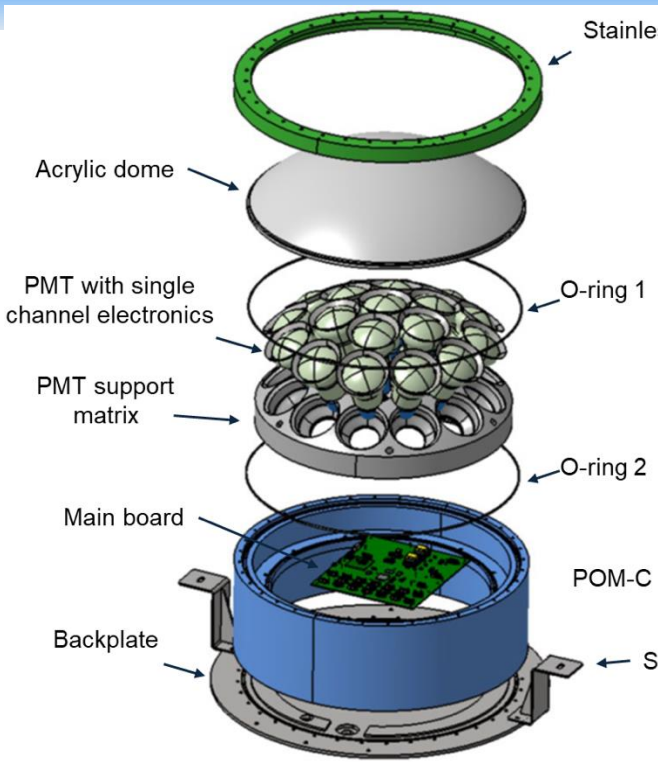
Proposed to the collaboration in 2016 as alternative/complementary to the 20’’ PMTs

The idea comes from the KM3NeT DOMs, **modified** and **optimized** to meet the HK requirements

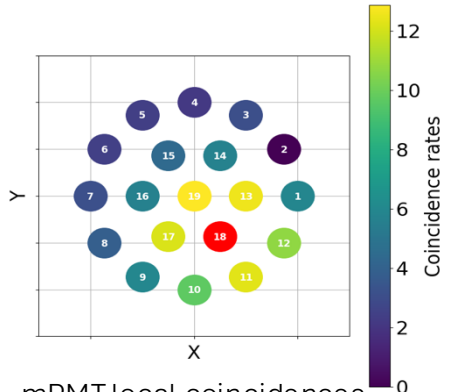
They were proposed to the Hyper-K collaboration, which accepted the use of them along the 20’’ due to the **numerous improvements** that they would bring

mPMT features:

- Superior photon counting
- Improved angular acceptance
- Extension of dynamic range
- Intrinsic directional sensitivity
- Local coincidences



Breakdown structure of the mPMT module

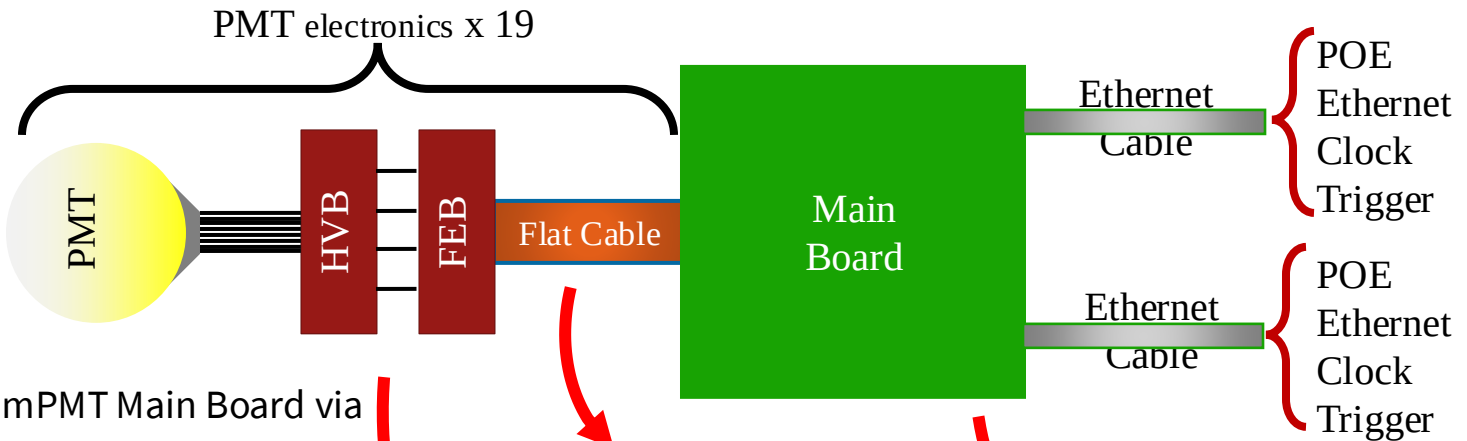


mPMT local coincidences of PMT 18 with the other 18 PMTs

KM3NeT DOM

Multi-PMT Electronics Overview

Each of the 19 single channels has its own High-Voltage Board (**HVB**) and Front-end Board (**FEB**)



All the channels then connect to the mPMT Main Board via flat cables

The **main board** mounts the main processor of the whole detector, it comunicates with the DAQ and supplies the voltage needed by the FEB and HVB of each channel

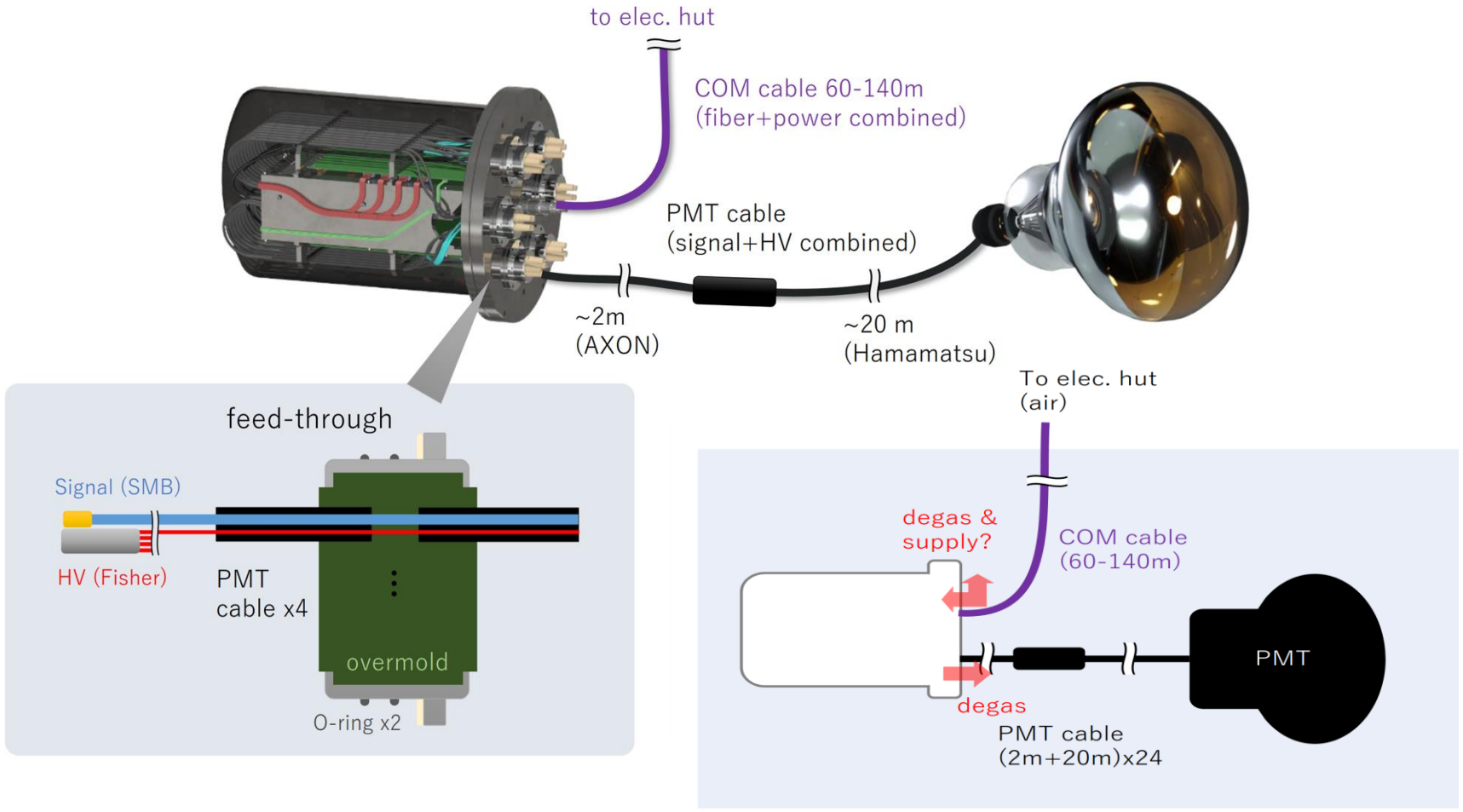
Requirement : Total Power consumption <4W
HVB: 3mW
FEB: 40mW

Summary & Outlook

- Jennifer2 has given a fundamental support to the electronics development to reach the actual status
- Design and prototype validation. Collaboration wide review
- System integration tests at several labs. Full VST at CERN and Kamioka
- Mockup installation test at Kamioka (procedures validation)
- Preparation of assembly lines
- Tendering and procurement started for several components (PMTs, HV, LV, vessels, timing, ...), or starting shortly after PR Review conclusion
- Assembly of electronics underwater vessels at CERN currently scheduled for Q3 2025
- Assembly of multi-PMTs at INFN/NA, Poland and Canada currently scheduled for Q3 2025

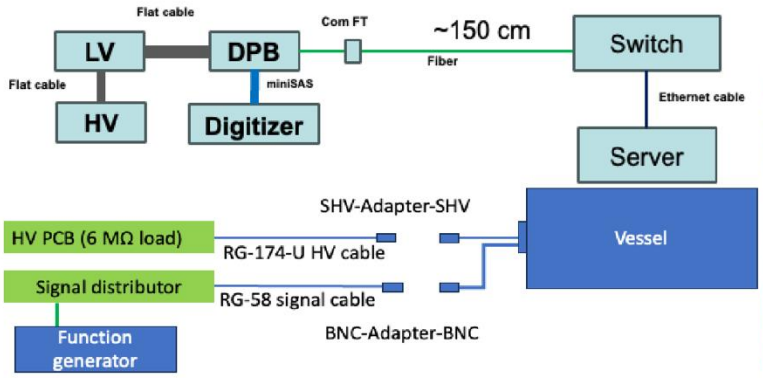
Thank you !

Degassing


to elec. hut
COM cable 60-140m
(fiber+power combined)
PMT cable
(signal+HV combined)
~2m
(AXON)
~20 m
(Hamamatsu)
feed-through
Signal (SMB)
HV (Fisher)
PMT
cable x4
overmold
O-ring x2
To elec. hut
(air)
degas &
supply?
COM cable
(60-140m)
PMT
degas
PMT cable
(2m+20m)x24

Underwater test at CERN

Fully assembled underwater module is in the water for tests since February.



Feb. 8	Assembled the board on the stand
Feb. 15	Immersed the vessel in the water. (Water temperature is 16 C).
Feb. 20	HV board switched ON at nominal power i.e. 6 MΩ load at 2500 V (kept running until March 15)
Mar. 15	Water temperature was set to 14 C.
Mar. 17	Powering on the digitizer boards.
Mar. 25	Powering on all the boards (LV/HV/DPB/Digitizers)