Update on Firmware porting from ArriaVGX to Cyclone10GX FPGA device

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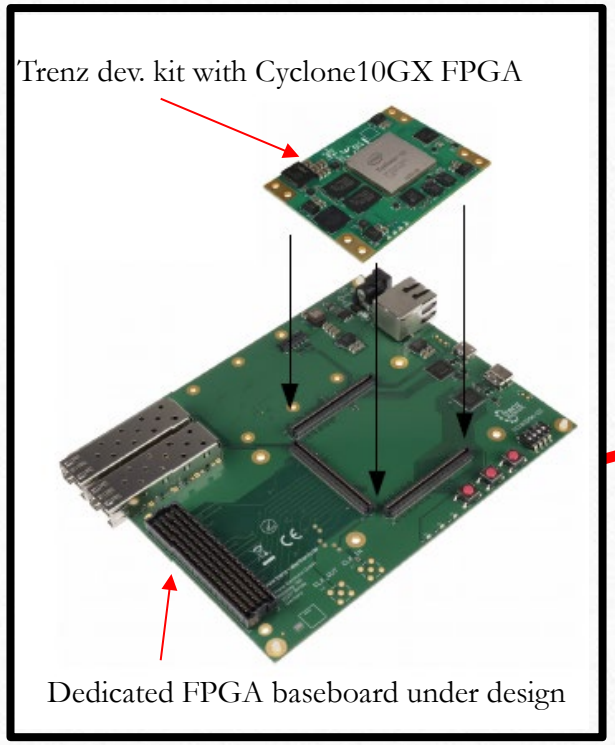
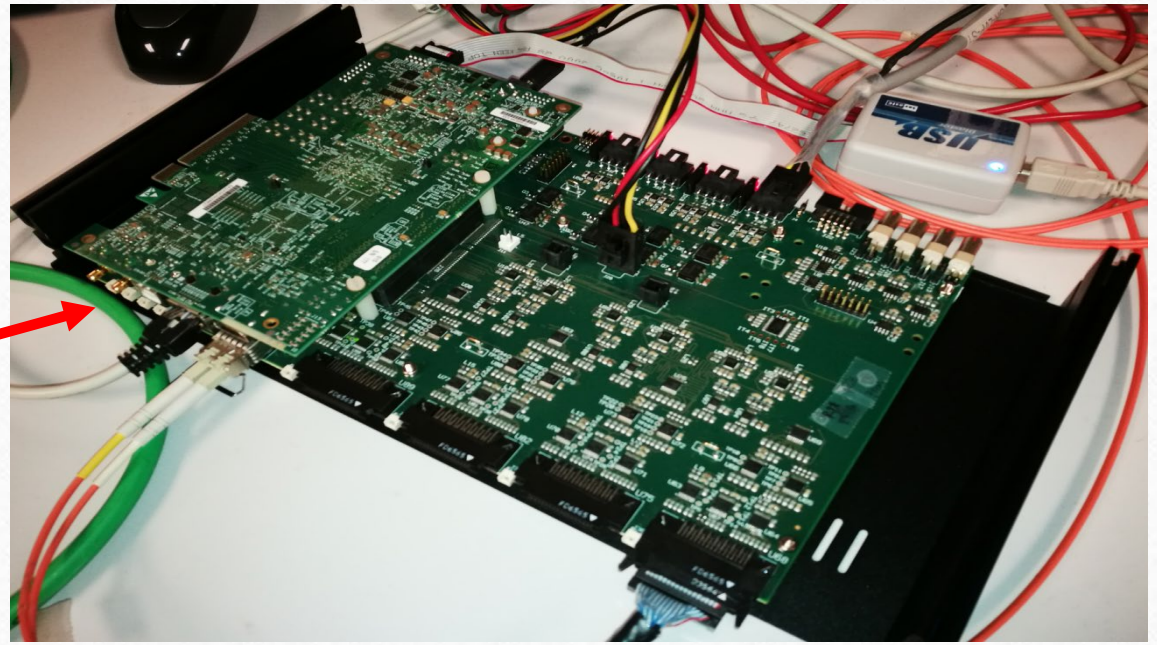
GEMROC: Off-detector readout module for BES-III CGEM-IT detector





GEMROC module dimensions: 334mm x 176mm x 44mm

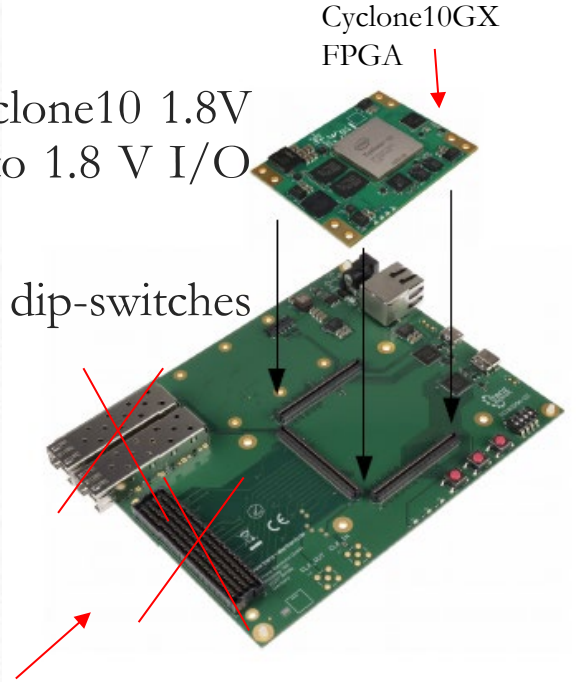
A dedicated board is under development in order to replace the Intel/ALTERA ArriaV dev. kit currently mounted, inside the GEMROC module, on the GEMROC Interface Card.

The new FPGA baseboard will mount the Trenz Electronic dev. kit TEI0006-04-API23A based on a Cyclone10 GX-10CX220 FPGA.

NEW FPGA BASEBOARD - DESIGN

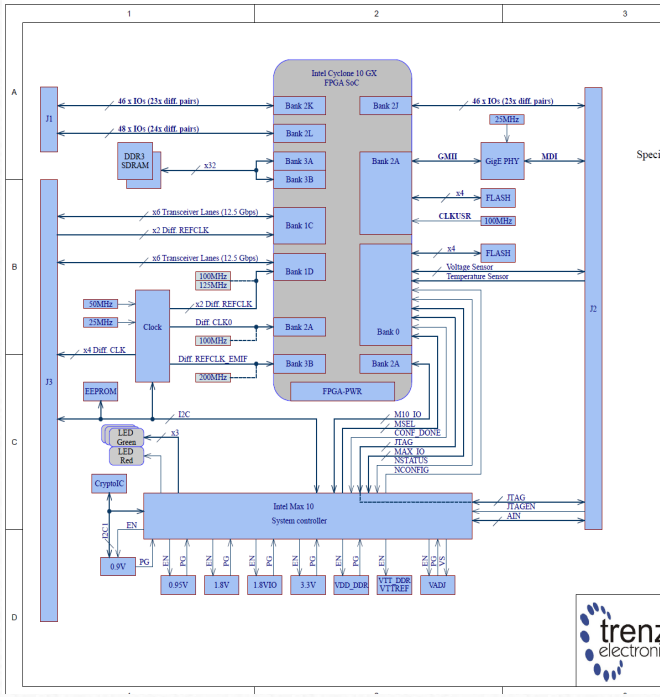
- The new FPGA baseboard maintains the original ArriaV form factor and is compatible with the current GEMROC off-detector readout mainboard (the mechanics will remain the same as for the Arria V):
- The new FPGA baseboard is connected to the GEMROC interface card using the same HSMC connector provided by ArriaV devkit.
- The new FPGA baseboard provides a set of buffers/level translators to adapt Cyclone10 1.8V I/O to the original ArriaV 2.5V I/O (LVDS Cyclone10gx I/O banks support up to 1.8 V I/O Standards).
- The new FPGA baseboard features a Gbit ethernet port, a USB programming port, dip-switches and power modules.

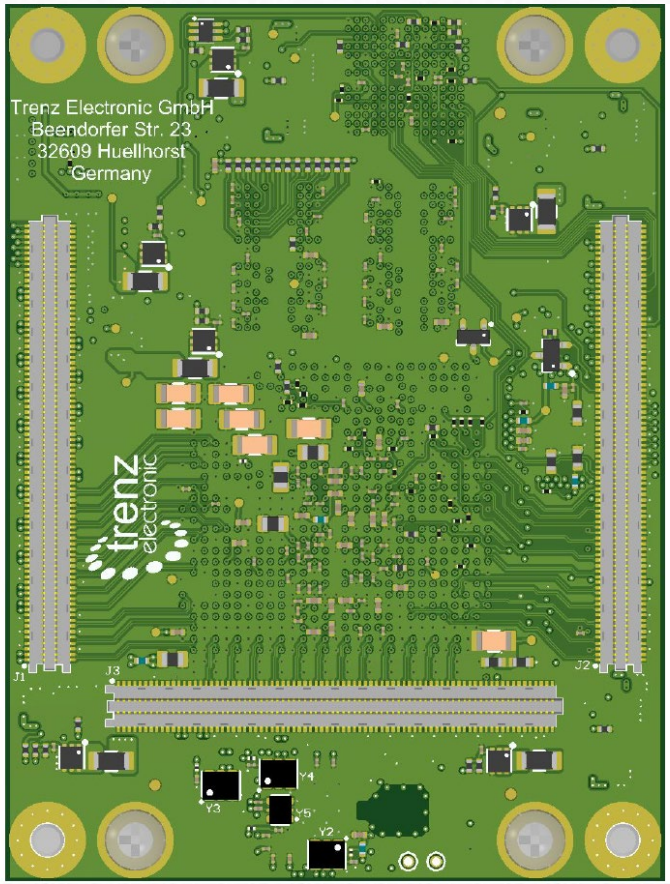
Trenz dev. kit with Cyclone10GX FPGA

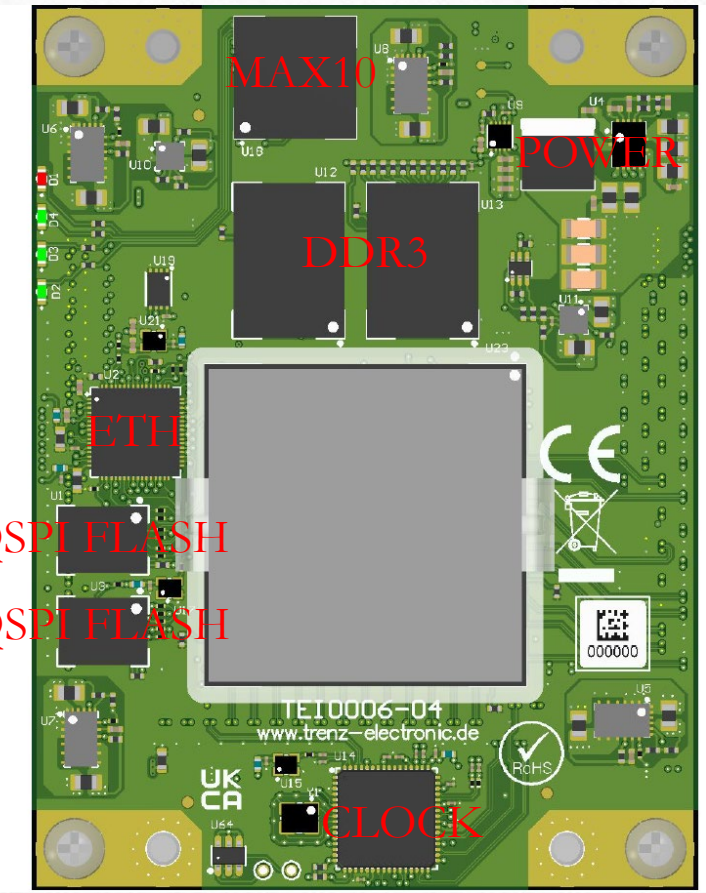


Dedicated baseboard under design

Intel Cyclone10GX interface on Trenz module







MAX10 FPGA = system controller (level translator – power management – jtag configuration - onboard clock programming)

Functional test with Cyclone10GX devkit (TEI0006 – Trenz Electronic)

- A Functional test has been done using the TEI0006 Cyclone10 dev.kit installed on a TEIB0006 baseboard.
- The baseboard includes an ethernet port, an USB programming port, one FMC and two SFP+ connectors.
- The dev.kit has been programmed using the USB Blaster interface integrated on the baseboard (this is the main interface for remote programming and debugging operations).
- The ethernet link uses a GMII PHY interface: original ethernet firmware developed for the ArriaV dev.kit has been adapted and ported to the new hardware (successful test completed).

Current status – Cyclone10GX FPGA firmware porting

- Porting of GEMROC firmware onto this platform (From Standard version to Quartus Prime Pro 23.2 migration):
  - The upgrade of all instantiated Intel/ALTERA IP blocks was done.
  - A QSys - Platform designer - project was realized to include the NiosII processor and its peripherals for the slow control port.
  - Pin placement and Quartus Fitter was satisfied.
  - Full compilation to get an output top.sof file has been done.
  - Ethernet Port interface was tested.
  - Main trigger functions have been implemented (signal reception from BESIII Fast Control System and their distribution to FCS local fanout).
- Software for Cyclone10 GX FPGA to be tested.
- In Ferrara now available 5 Trenz TEI006 (Cyclone10GX220) FPGA boards.