Welcome to ESC25

the XVI INFN International School on

“Architectures, tools ad methodologies for developing efficient large scale scientific computing applications”

September 29 - October 9, 2025
Bertinoro (FC) Italy

Alberto Garfagnini – INFN-PD and Padova University

On behalf of

The Italian Institute for Nuclear Physics (INFN):

- Bologna, CNAF, Padova, providing most of the support

The University of Bologna, Department of Physics and Astronomy

The ESC25 lecturers

- and their Institutions

Attendance this year

- 21 participants were selected
- 10 from foreign Institutions (9 from CERN)
- 11 from Italian Institutions

Bertinoro in the past

Bertinoro is a nice medieval village, famous for its **hospitality** and therefore quite well suited as a location for a center like CeUB

- the name most likely comes from **"Castrum Brittinori"** (XI century) and it is probably due to the frequent stopping of pilgrims coming from Britain, in their way to Rome, used to take in the quiet surroundings of Bertinoro
- A legend says that Galla Placidia, daughter of the Roman emperor Theodosius I, drank local wine in a humble clay chalice and said

  "Non di così rozzo calice sei degno, o vino, ma di *berti in oro*"

- One of the monument in Bertinoro known as **Colonna delle Anelle** ("Column of the Rings" or "Column of hospitality") is a column in white stone with 12 rings erected in 1300 by the noble families to express **their commitment to hospitality**.
- Each one of the rings corresponded to a family
- foreigners arriving in town, could select the family to be hosted, by **tying** the horse bridles to the corresponding ring

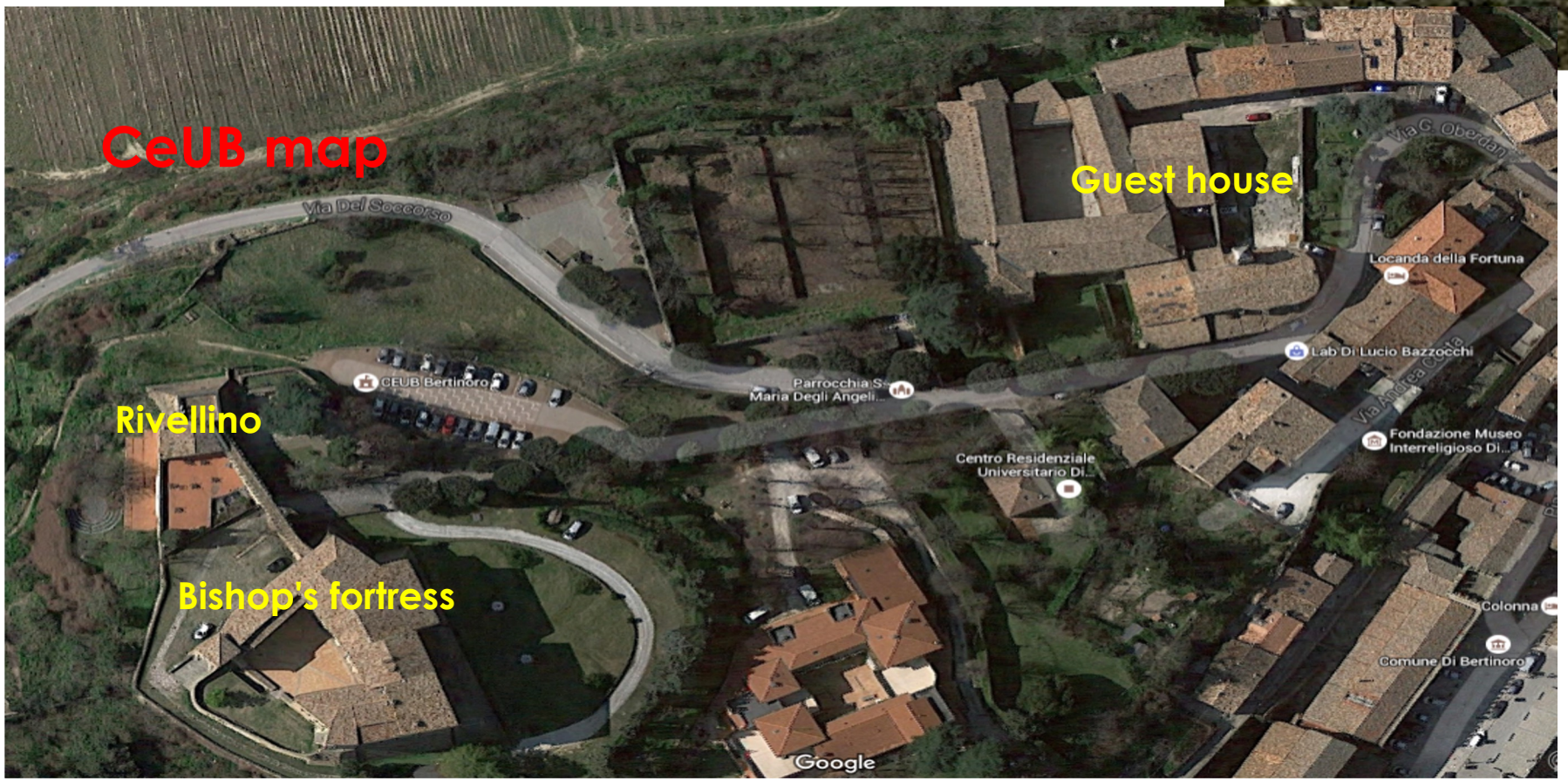
Bertinoro today

Bertinoro still hosted a "**Hospitality Festival**". Held at the end of August or first week of September (September 4-7, 2025)
it includes an entire night of music, dances and events, some historic commemorations and the final Hospitality Rite (https://www.visitbertinoro.it/it/eventi/festa-dell-ospitalita-2025/)

In this ceremony visitors **can be hosted** for lunch by a family in the town simply **taking one of the envelopes** tied to the rings of the Hospitality column (which inside has the name of the hosting family).

You will not get this opportunity this week, but I'm sure you will at least enjoy the **good food and wine** that Bertinoro will offer to you while you are staying here

CeUB: University Residential Center of Bertinoro



The CeUB facilities

- The Center was brought back in use with renovation work that started in 1991 in the fortress and in the guest house, followed by integration of additional buildings

- Today the Center offers:
  - **15 lecturing/meeting rooms** inside the Bishop's Fortress, the Rivellino, St. Sylvester church and the Theatre;
  - **2 computer labs**, 20 and 50 seats;
  - **86 bedrooms** (single, twin, double);
  - a **canteen with 200 seats** for breakfast, lunch and gala dinners
  - **120+ events** per year
  - up to **30.000** presences per year

Why hosting the ESC school

- High Energy Physics has been **heavily relying** on computing since long time
  - for many years the scale of resources needed by HEP experiments was such that the computing centers of the hosting lab **were coping well** with the core computing data processing needs
  - the UA1/2 experiments that discovered the Z and W bosons at CERN were good examples
  - the model started to break at the end of the last century when experiments, like the BaBar experiment at the SLAC B-factory, had to deal with a **huge amount of data** and the computing power had to be scaled up by more than one order of magnitude w.r.t. **the initial estimates**
  - the investment needed started to grow very significant
  - for the first time it was felt necessary to distribute the processing of the data stored on tape to an external center

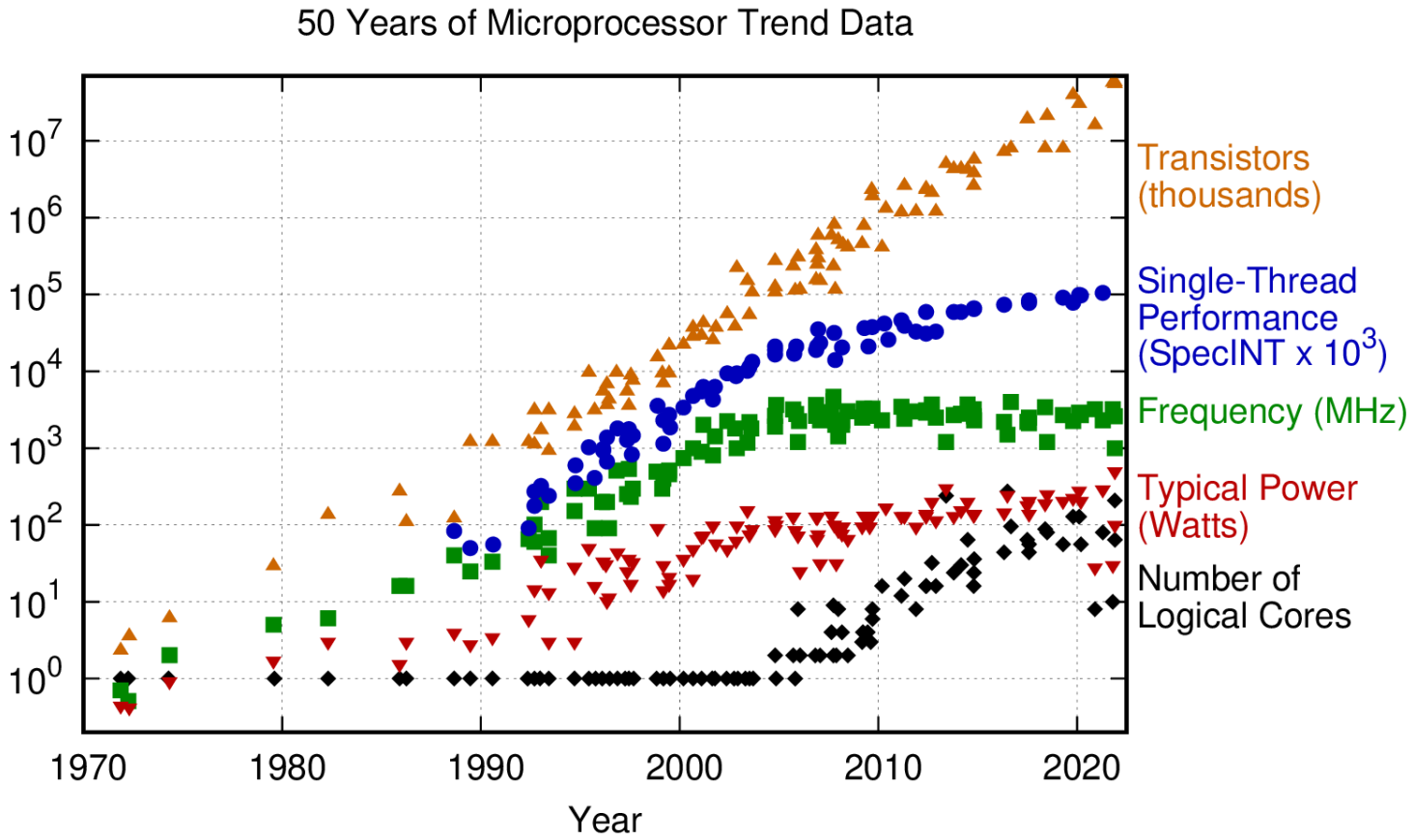
The end of the “free ride”

Transistor counts follow an exponential growth

The highest transistor count in any IC chip is a deep learning engine called the Wafer Scale Engine 2 by Cerebras, using a special design to route around any non-functional core on the device: it has **2.6 trillion** MOSFETs, manufactured using TSMC's 7 nm FinFET process

Additional transistors will provide more cores

To benefit from future processors parallel workloads are mandatory



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2021 by K. Rupp

- Data and plot available at
- https://github.com/karlrupp/microprocessor-trend-data

Cerebras WSE-3

Fabrication process
5nm

Silicon area
46,225mm²

Transistors
4 Trillion

AI-optimized cores
900,000

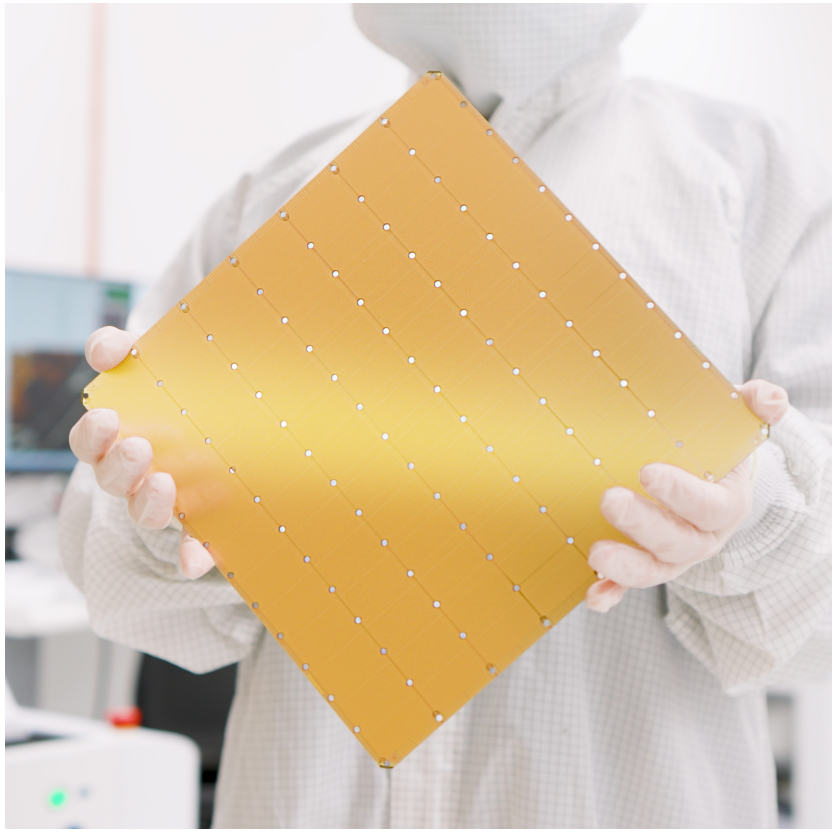
Memory (on-chip)
44GB

Memory bandwidth
21PB/s

Fabric bandwidth
214Pb/s

Cerebras WSE-3
4 Trillion Transistors
46,225 mm² Silicon

Largest GPU
80 BillionTransistors
814 mm² Silicon



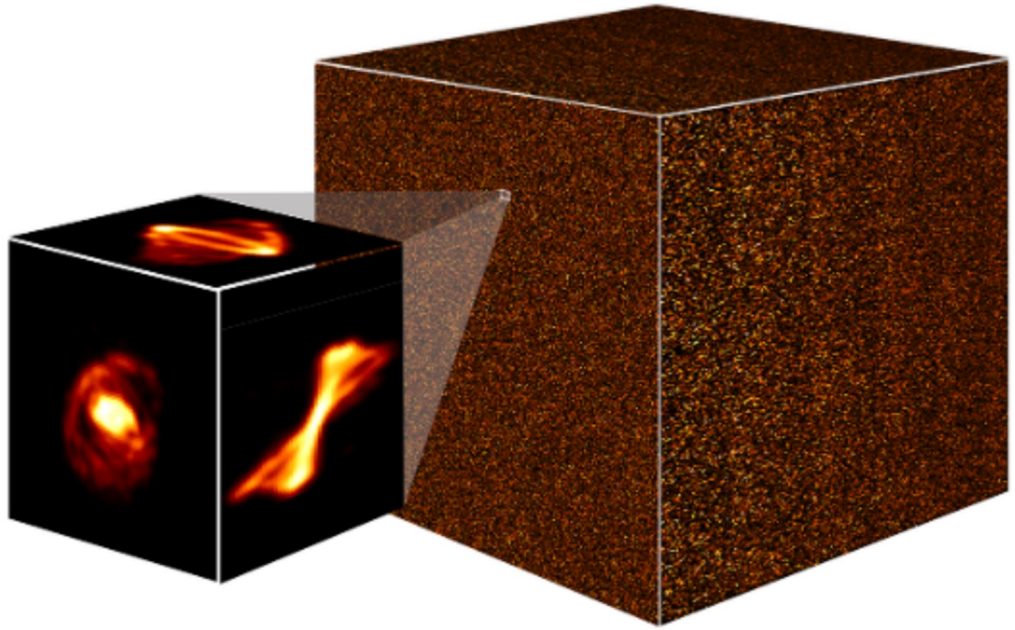
The Cerebras Wafer Scale Engine (WSE) is a single, wafer-scale integrated processor that includes compute, memory and interconnect fabric.

Why a computing school about efficiency

- The conception of this school was motivated by the awareness that efficient usage of computing resources in our field:
- had to be taken seriously, given the level of computing investment now required
- in the past was not always well understood and taken into proper consideration
- was becoming more and more challenging due in particular to the physical constraints in increasing scalar performance and the attempts to exploit anyway Moore's law with new processor architectures
  - many cores, co-processors, GPU, vector units, new architectures (RISC-V), etc.
  - memory access getting more and more critical
  - ....

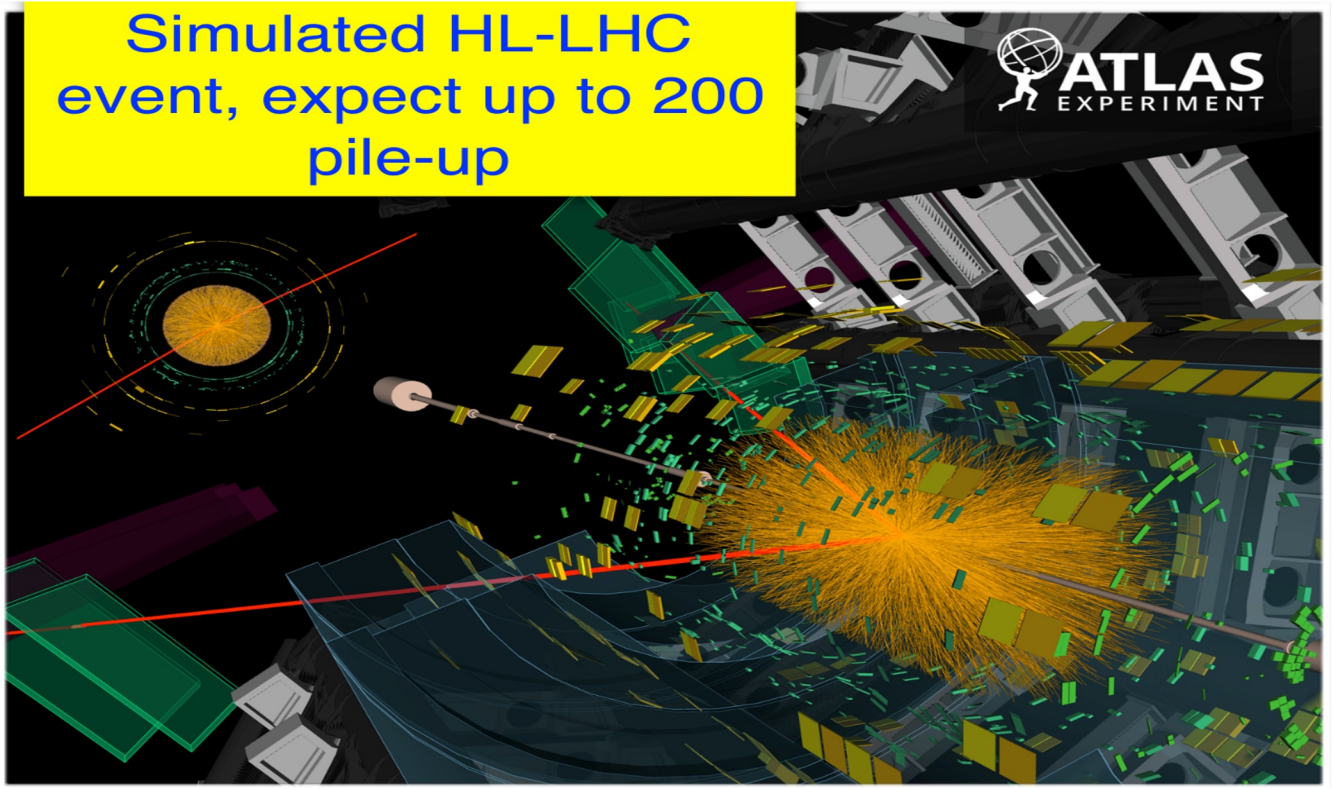
Future will be more challenging

SKA Science Data Challenge: analyse a simulated datacube 1 TB in size, in order to find and characterise the neutral hydrogen content of galaxies across a sky area of 20 square degrees.



SKA 1TB data cube

https://www.skao.int/en



V. Kourlitis, "HL-LHC and Beyond Computing Challenges", https://cds.cern.ch/record/2861812/files/ATL-SOFT-SLIDE-2023-226.pdf

TOP 500 HPC

- https://top500.org/lists/top500/2025/06/

El Capitan system retains the No. 1 position
With El Capitan, Frontier, and Aurora, there are now 3 Exascale systems leading the TOP500
All three are installed at Department of Energy (DOE) laboratories in the United States

Italy has two systems in the TOP 10:
- HPC6 at Eni SpA
- Leonardo at CINECA

10 **Leonardo** - BullSequana XH2000, Xeon Platinum 8358 32C 2.6GHz, NVIDIA A100 SXM4 64 GB, Quad-rail NVIDIA HDR100 Infiniband, EVIDEN
EuroHPC/CINECA
Italy

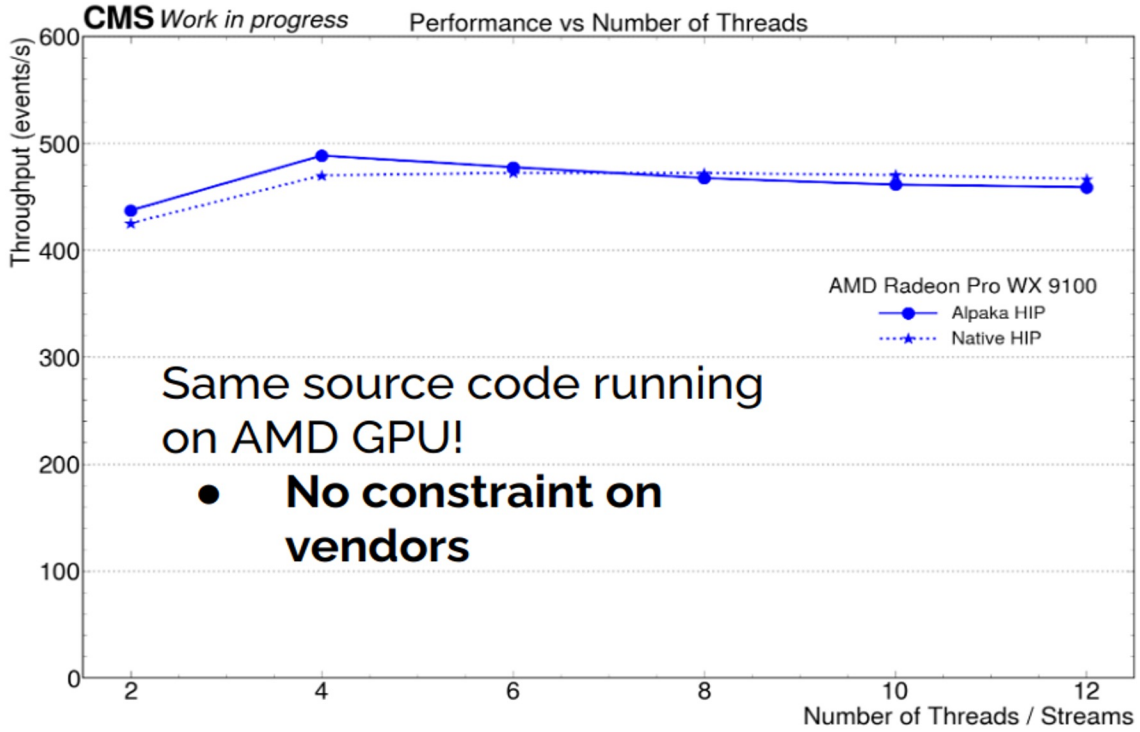
Cores	Rmax (PFlop/s)	Rpeak (PFlop/s)	Power (kW)
1,824,768	241.20	306.31	7,494

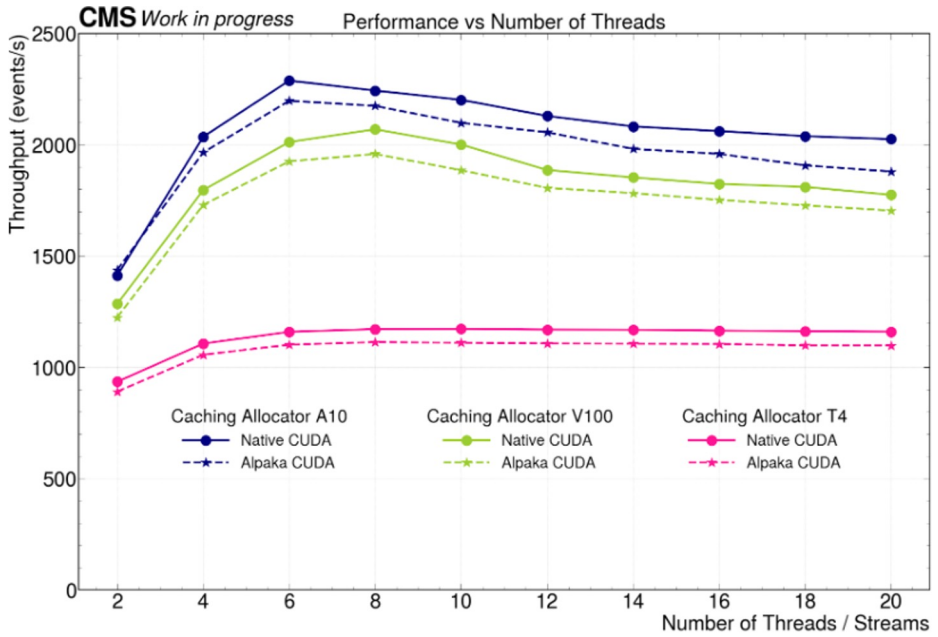
Rank	System	Cores	Rmax (PFlop/s)	Rpeak (PFlop/s)	Power (kW)
1	**El Capitan** - HPE Cray EX255a, AMD 4th Gen EPYC 24C 1.8GHz, AMD Instinct MI300A, Slingshot-11, TOSS, HPE DOE/NNSA/LLNL United States	11,039,616	1,742.00	2,746.38	29,581
2	**Frontier** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, HPE Cray OS, HPE DOE/SC/Oak Ridge National Laboratory United States	9,066,176	1,353.00	2,055.72	24,607
3	**Aurora** - HPE Cray EX - Intel Exascale Compute Blade, Xeon CPU Max 9470 52C 2.4GHz, Intel Data Center GPU Max, Slingshot-11, Intel DOE/SC/Argonne National Laboratory United States	9,264,128	1,012.00	1,980.01	38,698
4	**JUPITER Booster** - BullSequana XH3000, GH Superchip 72C 3GHz, NVIDIA GH200 Superchip, Quad-Rail NVIDIA InfiniBand NDR200, RedHat Enterprise Linux, EVIDEN EuroHPC/FZJ Germany	4,801,344	793.40	930.00	13,088
5	**Eagle** - Microsoft NDv5, Xeon Platinum 8480C 48C 2GHz, NVIDIA H100, NVIDIA Infiniband NDR, Microsoft Azure Microsoft Azure United States	2,073,600	561.20	846.84	
6	**HPC6** - HPE Cray EX235a, AMD Optimized 3rd Generation EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-11, RHEL 8.9, HPE Eni S.p.A. Italy	3,143,520	477.90	606.97	8,461

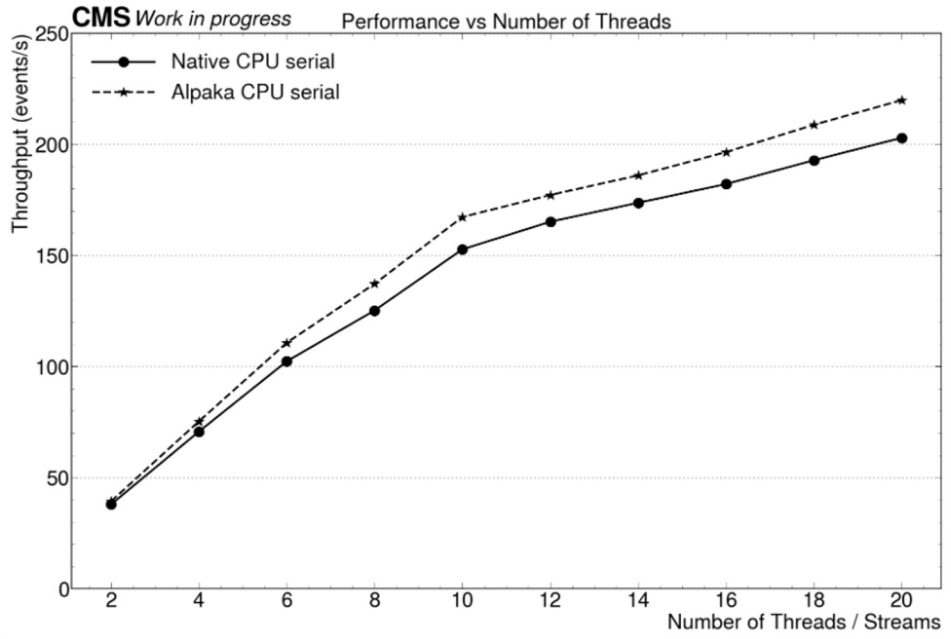
CMS Patatrack R&D

Heterogeneous computing and performance portability a reality at LHC experiments

Hackathon focused on improving the performance portability of the CMS reconstruction software for charged particle trajectories.







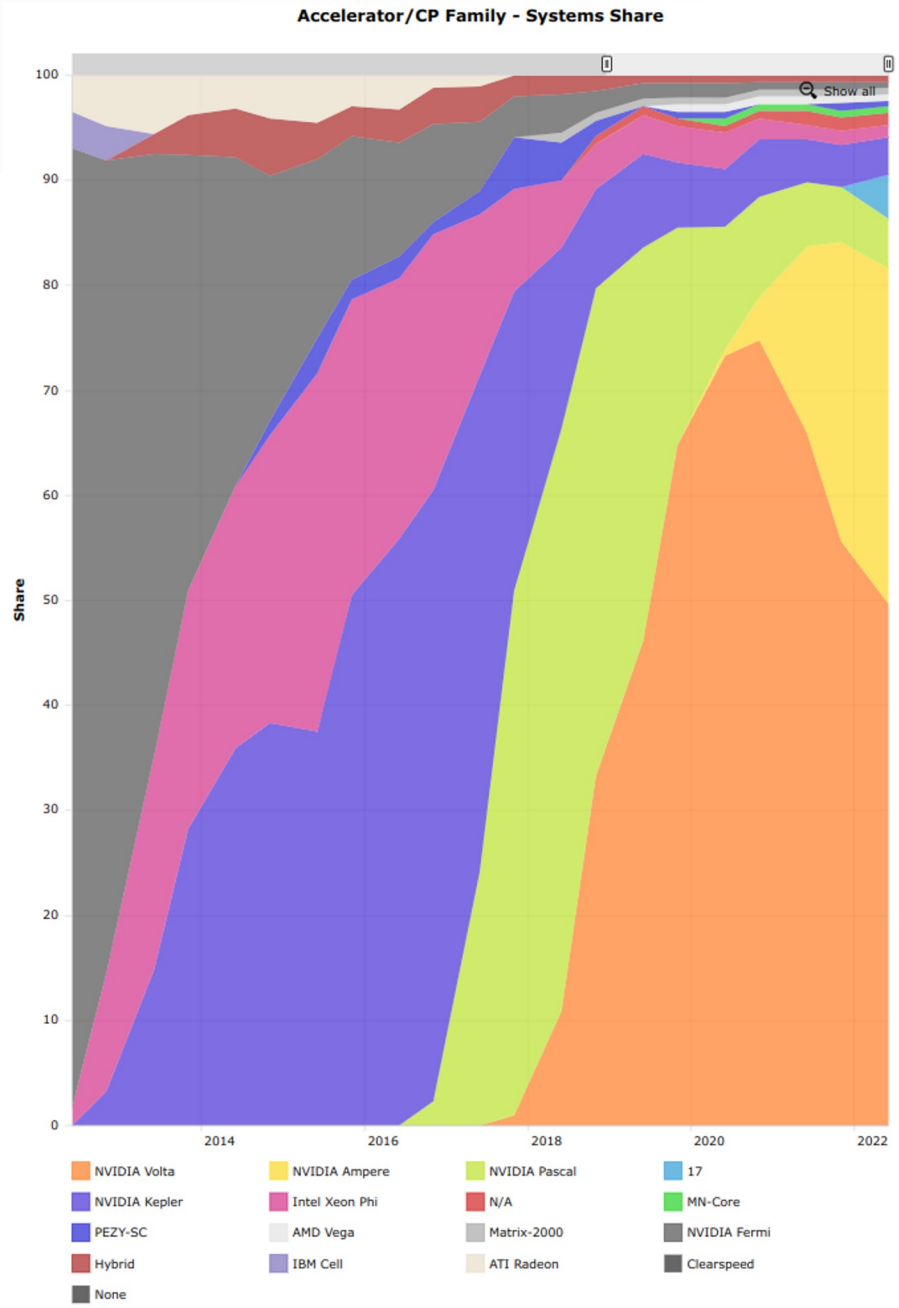
A quick look at HPC

Exascale computing
- 1000 PFlops, 1000 Pbytes

However, **no supercomputer runs real applications faster than 10 percent of its maximum peak design speed**

The natural trend is towards **poorer and poorer efficiencies** as systems scale out to Exascale

“it is not **power** or **reliability** that are the **exascale challenges**: it’s **programmability of complex memory hierarchies**”
Bronis R. de Supinski Chief Technology Officer (CTO) for Livermore Computing



The school evolution

- In the first editions of the School we tried to embrace **several key aspects** related to the efficient usage of computing resources in scientific applications, from **exploitation of modern CPUs** to **I/O related issues**
- however, we realized that the scope was too vast for a one-week-long school
- last year we experienced a longer (8 days) school to go deeper on few topics
- A longer school was welcomed by students, so this year you will have a longer time (11 days)
- a few years ago, we decided therefore to focus the School on the area where developments looked most disruptive and challenging: **parallel processing**

ESC25 lecture plan in a nutshell

Introduction to computing architectures and performance challenges

Core software efficiency (C++)

Parallel programming

GPUs and CUDA

Efficient Memory Usage

Debugging

Cluster computing with MPI

Calling C++ libraries from Python

oneTBB

OpenMP

Floating point computation and vectorization

Esc25 Social Event

RAVENNA UNESCO SITES AND SOCIAL DINNER

- 11.00 Departure from Bertinoro by bus
- 12.15 - 14.50 Arrival in Ravenna and free time for lunch
- 15.00 - 17.00 Ravenna guided visit in English
- 17:00 – 18:20 Free time in Ravenna
- 18:30 Bus from Ravenna ti Cervia
- 19.30 Social Dinner in Cervia at "Agriturismo Casa delle Aie"
- 21:30 Bus to CEUB

Evening Lectures

- Friday October 3rd at 18:00:
  “Use and Abuse of Random Numbers» T. Mattson

- Forse un’altra di Tim

Poster Session and Lightning talks

- Saturday 4th October, from 6 p.m. **Poster Session and Aperitivo** (Terrace of Rocca)

- Please give the posters to Anna within Wednesday 1st.

- Starting from Tuesday, after the afternoon lessons, there will be a moment for the lightning presentations. Please upload your files in the Drive folder.

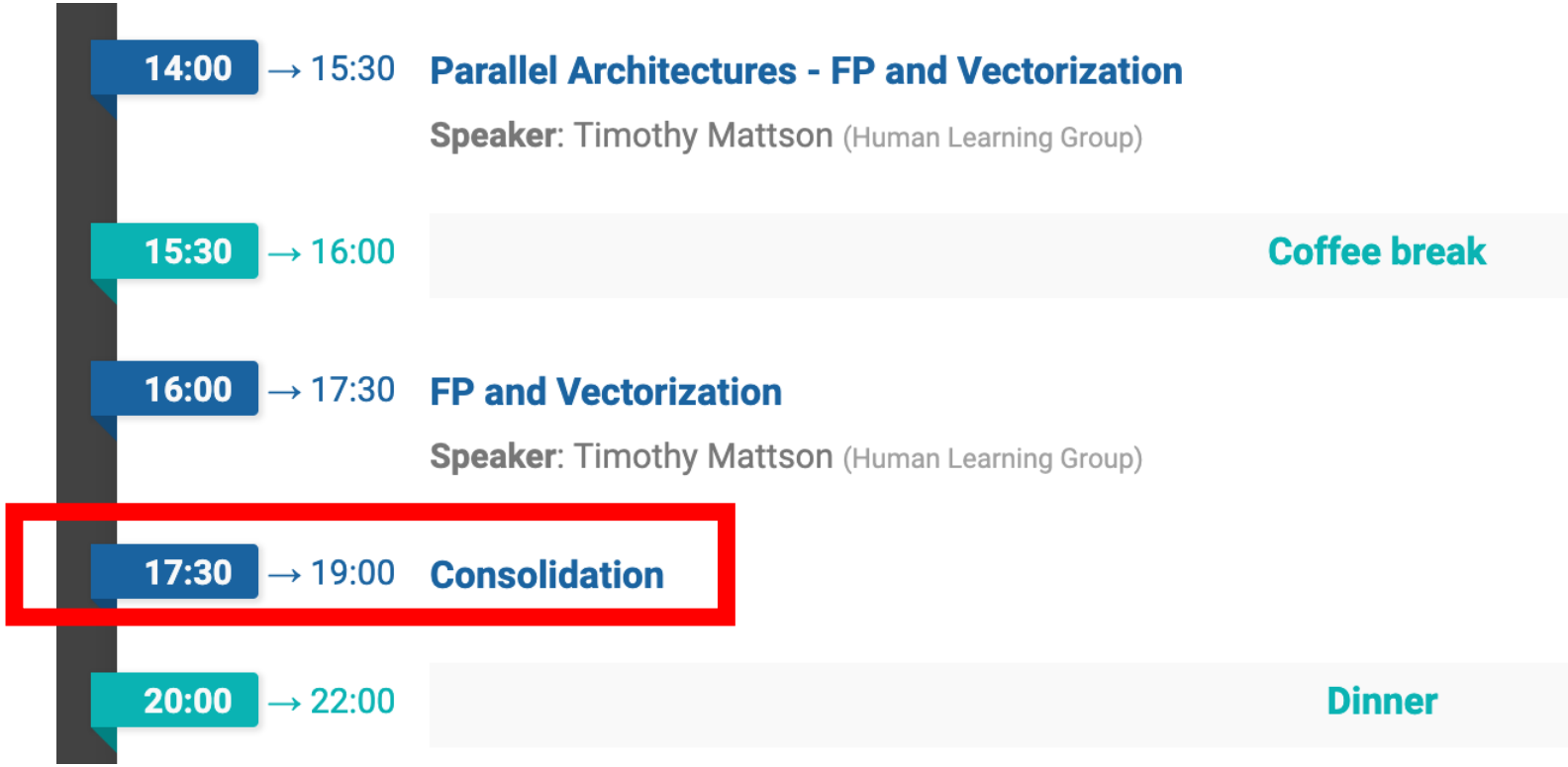
Improving the School

- we have been striving to **improve the School** year after year
- the feedback we got from the students has always been **very useful**
- on Wednesday, October 8 morning we will give you an opportunity to evaluate:
  - the **perceived quality** of various aspects of the School via the feedback questionnaire
  - the **competences you have acquired**
- through a final test, Wednesday October 8 at 14:00
  - information collected is of course **very valuable to us too**

Consolidation time

- to accommodate the need of students had to have some time for assimilating the material presented in the lectures there are some **consolidation time slots**

- **Almost every day, in the afternoon, you will have between 1.5- 2 hours to work on the exercises given by the lecturers**



Wireless and Social Networks

Bertinoro wireless network is available in all rooms including the guest house
[CeUB SSID and eduroam SSID]

EMAIL

esc_contact@lists.infn.it

TELEGRAM

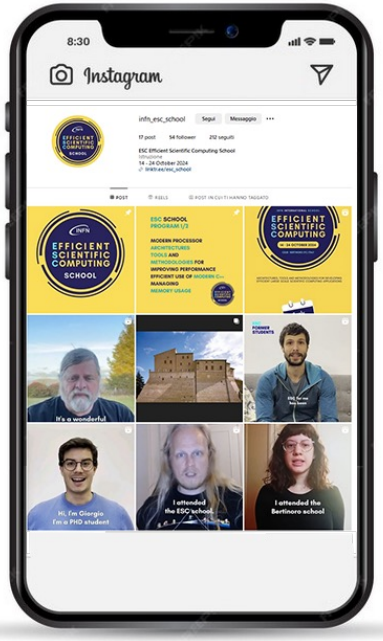
Join the channel for logistic updates

ESC25 - https://t.me/+RFxpEViQ-PAyYmVk

INSTAGRAM

Follow ESC and tag the school

@infn_esc_school



We wish you a very pleasant and "efficient", great time in Bertinoro

Backup