WP3 – Radiation tolerance and cryogenic operation

ASPIDES kickoff meeting

Giuliana Fiorillo, Bologna, 31 January 2025

WP3

Scope

- Establish the procedures for the radiation tolerance study of the test chip
  - select the sources for the irradiation campaign and the fluence/dose steps to reach a maximum fluence around 10^{13} 1MeV neutron equivalent/cm^2 and a maximum dose not exceeding 10 Mrad(SiO2). The selection criteria will into account on the one hand the actual applications and on the other the comparison with the scientific literature.
- Characterization of i) test chip, ii) prototype and iii) demonstrator in cryogenic conditions
  - operation of the hardware for device cooling and interfacing to the external instrumentation
- Main WP3 contributors: BO, NA, PV, TIFPA, TO + PD, MI
  - collaborate with WP2 in the design of the test boards for radiation tolerance tests and characterization at cryogenic temperatures
  - collaborate with WP4 for TCAD simulation tuning and modeling the effects of radiation and of cryogenic conditions on the device performance

WP3

Expressions of interest

nome	cognome	email	sezione	ruolo/contributo/interesse
Giuliana	Fiorillo	giuliana.fiorillo@na.infn.it	NA	WP leader
Marcello	Campajola	macampajola@na.infn.it	NA	studio del danno da radiazione (aumento DCR, RTS) e caratterizzazione a basse temperatura
Gianmaria	Collazuol	gianmaria.collazuol@pd.infn.it	PD	studi di caratterizzazione del sensore (efficienza, rumore, tempi) ed effetti danno da radiazione e basse temperature
Lodovico	Ratti	lodovico.ratti@unipv.it	PV	studio del danno da radiazione
Luigi	Rignanese	rignanes@bo.infn.it	BO	studi di effetti del danno da radiazione
Romualdo	Santoro	romualdo.santoro@uninsubria.it	MI	test di qualifica con contributo all'analisi dati

WP3

Interfaces

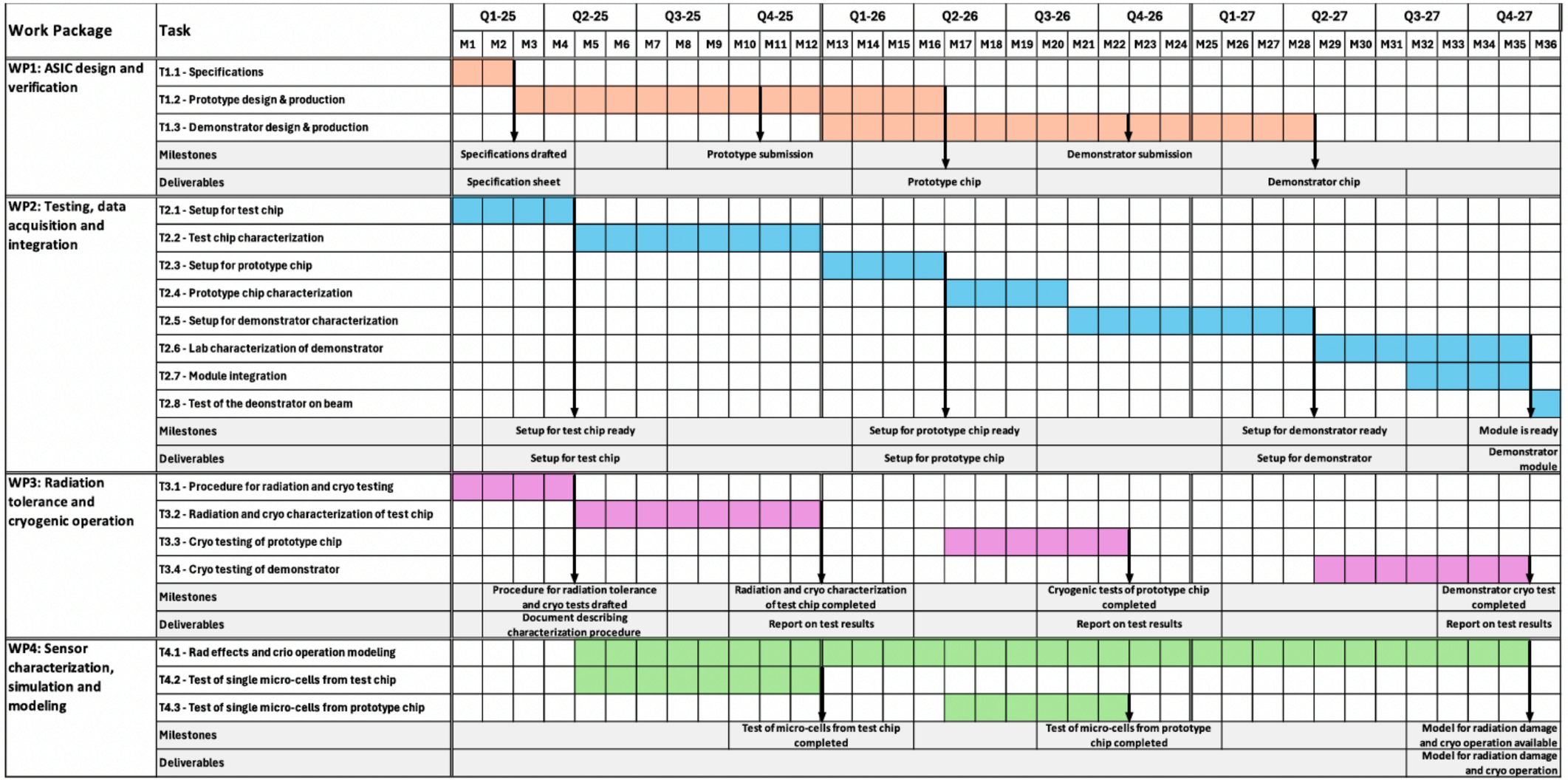
- WP2 – Testing, data acquisition and integration → Romualdo
  - design and assemble suitable test boards and acquisition systems also for radiation tolerance characterization and tests in cryogenic conditions
- WP4: Sensor characterization, simulation and modeling → ????
  - experimental data extracted after irradiation and from characterization at cryogenic temperatures will be in particular leveraged for modeling the effects of radiation and of cryogenic conditions on the device performance

WP3

Tasks & Milestones

- Tasks
  - Task 3.1 (M1-M4): definition of the procedures for radiation tolerance study and characterization at cryogenic temperature
  - Task 3.2 (M5-M12): radiation tolerance tests and characterization at cryogenic temperature of the **test chip**
  - Task 3.3 (M17-M22): characterization at cryogenic temperature of the **prototype chip**
  - Task 3.4 (M29-M35): characterization at cryogenic temperature of the **demonstrator chip**
- Milestones
  - M4: procedure for radiation tolerance test and characterization at cryogenic temperature drafted → document 30/4/25
  - M12: radiation tolerance tests and characterization at cryogenic temperature of the test chip completed → report 31/12/25
  - M22 characterization at cryogenic temperature of the prototype chip completed → report 31/10/26
  - M35 characterization at cryogenic temperature of the demonstrator chip completed → report 30/11/27

Timeline


Work Package
Task
Q1-25
Q2-25
Q3-25
Q4-25
Q1-26
Q2-26
Q3-26
Q4-26
Q1-27
Q2-27
Q3-27
Q4-27
M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 M11 M12 M13 M14 M15 M16 M17 M18 M19 M20 M21 M22 M23 M24 M25 M26 M27 M28 M29 M30 M31 M32 M33 M34 M35 M36
WP1: ASIC design and verification
T1.1 - Specifications
T1.2 - Prototype design & production
T1.3 - Demonstrator design & production
Milestones
Specifications drafted
Prototype submission
Demonstrator submission
Deliverables
Specification sheet
Prototype chip
Demonstrator chip
WP2: Testing, data acquisition and integration
T2.1 - Setup for test chip
T2.2 - Test chip characterization
T2.3 - Setup for prototype chip
T2.4 - Prototype chip characterization
T2.5 - Setup for demonstrator characterization
T2.6 - Lab characterization of demonstrator
T2.7 - Module integration
T2.8 - Test of the deonstrator on beam
Milestones
Setup for test chip ready
Setup for prototype chip ready
Setup for demonstrator ready
Module is ready
Deliverables
Setup for test chip
Setup for prototype chip
Setup for demonstrator
Demonstrator module
WP3: Radiation tolerance and cryogenic operation
T3.1 - Procedure for radiation and cryo testing
T3.2 - Radiation and cryo characterization of test chip
T3.3 - Cryo testing of prototype chip
T3.4 - Cryo testing of demonstrator
Milestones
Procedure for radiation tolerance and cryo tests drafted
Radiation and cryo characterization of test chip completed
Cryogenic tests of prototype chip completed
Demonstrator cryo test completed
Deliverables
Document describing characterization procedure
Report on test results
Report on test results
Report on test results
WP4: Sensor characterization, simulation and modeling
T4.1 - Rad effects and crio operation modeling
T4.2 - Test of single micro-cells from test chip
T4.3 - Test of single micro-cells from prototype chip
Milestones
Test of micro-cells from test chip completed
Test of micro-cells from prototype chip completed
Model for radiation damage and cryo operation available
Deliverables
Model for radiation damage and cryo operation

Cryogenic tests

Goals & Plans

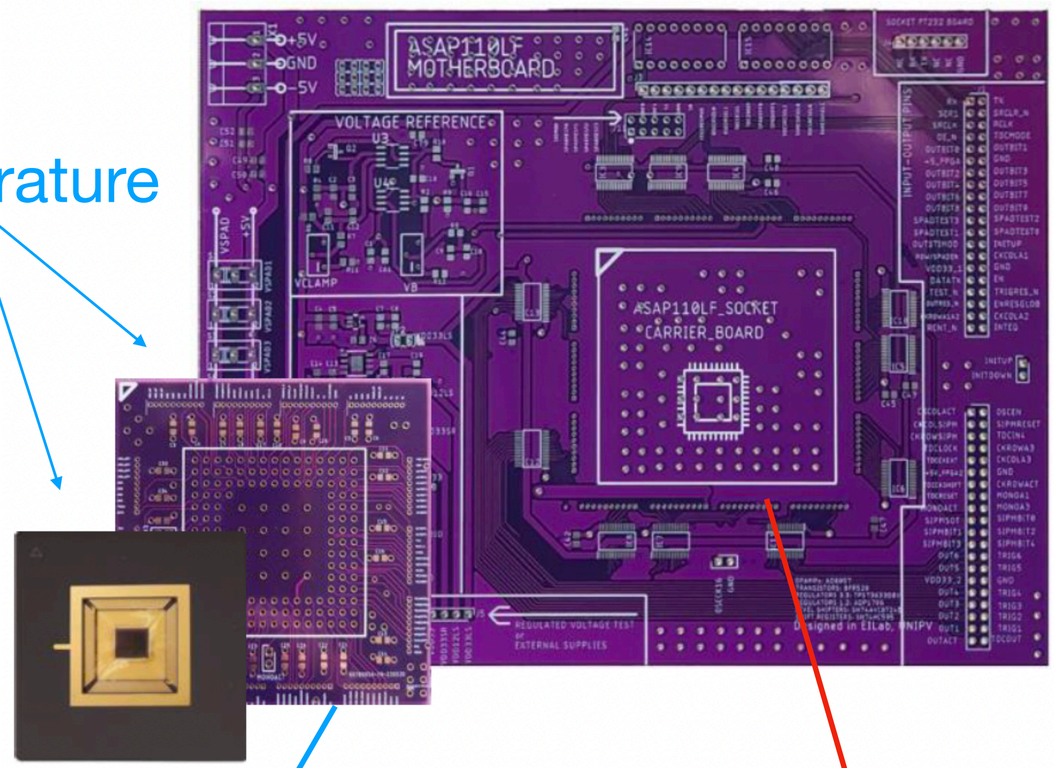
- Goal:
  - Characterization of the test chip at 77K (LN), possibly also as a function of T (dry system)
    - IV and CV curves, Breakdown voltage
    - Effects on transistors and digital electronics
    - DCR, afterpulsing, electrical and optical cross-talk,
    - QE and PDP/PDE (needs dedicated setup)
    - ~~Time resolution~~

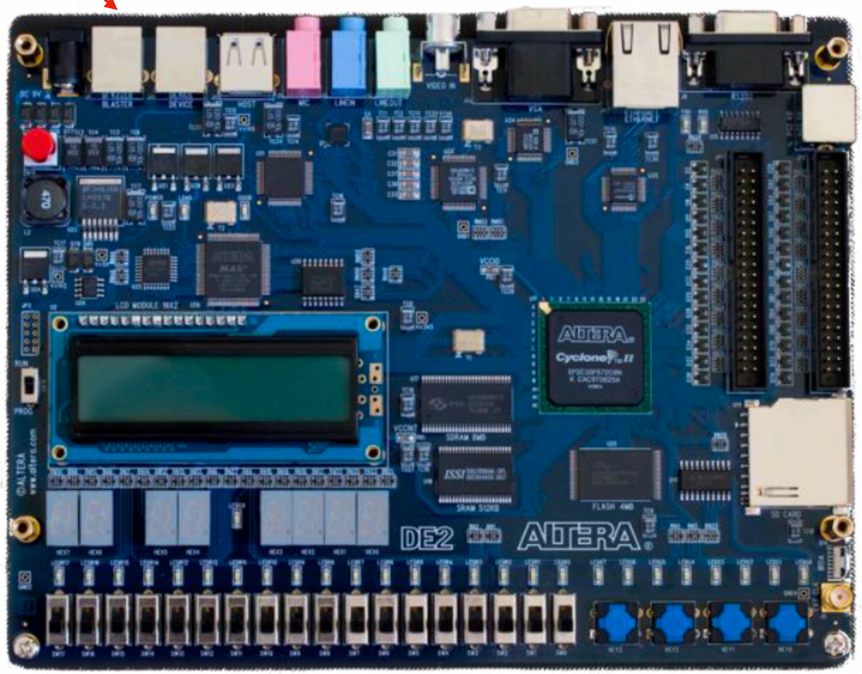
→ feedback to WP4

- Preliminary activities: design cryogenic (wet/dry) setups and interface boards for different measurements
- Timeline (proposed):
  - Define warm-cold **interfaces** by end of February, define **procedures** by March, **setups** ready by April
  - **Cryogenic tests** on same devices that will be irradiated → to be concluded by July, irradiation campaign in September

@room temperature

@cryo temperature





Connect to (warm)interface board → flat cable → feedthrough connector on flange

Connect to (cold)interface board → flat cable → feedthrough connector on flange

Radiation damage tests

Goals & Plans

- Goal:
  - Characterization of the test chip before and after irradiation
    - DCR (and I_{dark}) increase with the dose
      - Dedicated structures to evaluate the role of STI in DCR performance degradation
    - Effects on after pulsing
    - Random Telegraph Signals (RTS) occurrence
    - Damage mitigation/recovery with low temperature operations and thermal annealing

      → insights on the damage mechanism and feedback to WP4
    - Short- and mid-term annealing during irradiation (neutron and protons) using DCR as a damage probe
- Initial proposals for irradiation campaign:
    - protons (or neutrons), and electrons with integrated fluence in the range 10^{9} to $10^{11\text{-}12}$ n_{eq}
    - TIDs: 100 krad, 300 krad, 1 Mrad, 3 Mrad, 10 Mrad (may be reduced to three steps for the sake of time)
- Timeline (proposed):
  - **Define sources and fluence/dose steps** by end of February, **select irradiation facilities** by March, **define procedure**s by April, design&procurement of test boards in WP2 within May
  - **Pre-irradiation tests** concluded by July, **irradiation campaign** in September 2025

Summary and Outlook

- Cryogenic test preliminary steps:
  - design cryogenic setups and interface boards for different measurements
    - do we want a (dry) system to characterize the chip as a function of T?
    - system to characterize PDE at cryogenic temperature?
    - interface boards in WP2?
    - groups interested and available facilities (Padova? Torino? Others?)
- Radiation damage test preliminary steps:
  - define sources and fluence/dose steps → will ask Marcello to coordinate this task
    - select irradiation facilities
  - decide how many test chips to irradiate and/or cool down
    - cryogenic characterization before/after irradiation?
- Contact to WP2 → Romualdo
- Contact to WP4 → Luca/Lucio?

Input from the participants

L. Ratti

- Ionizing radiation damage
  - typically not the most alarming problem in CMOS SPADs (especially in comparison with bulk damage), but nevertheless interesting to see how the device performance evolves with the dose
  - Onset of secondary breakdown observed in SPADs fabricated in a 180 nm CMOS technology, likely related to charge accumulation in STI (see L. Ratti et al., “Dark Count Rate Degradation in CMOS SPADs Exposed to X-Rays and Neutrons”, IEEE Trans. Nucl. Sci., vol. 66, no. 2, Feb. 2019, pp. 567-574)
  - However, ionization damage, resulting from radiation induced charge accumulation in oxide layers, is strongly technology dependent (see A. Jouni et al., “Effects of X-Ray and γ-Ray Irradiations on 2-D-Planar and 3-D-Stacked CMOS SPADs”, IEEE Trans. Nucl. Sci., vol. 71, no. 8, Aug. 2024, pp. 1753-1765)
- Characterization of the test chip (also including dedicated structures to evaluate the role of STI in DCR performance degradation) at different TIDs: 100 krad, 300 krad, 1 Mrad, 3 Mrad, 10 Mrad (may be reduced to three steps for the sake of time)
- Possible facilities with irradiation systems can be found in Padova, Pisa, Torino, CERN

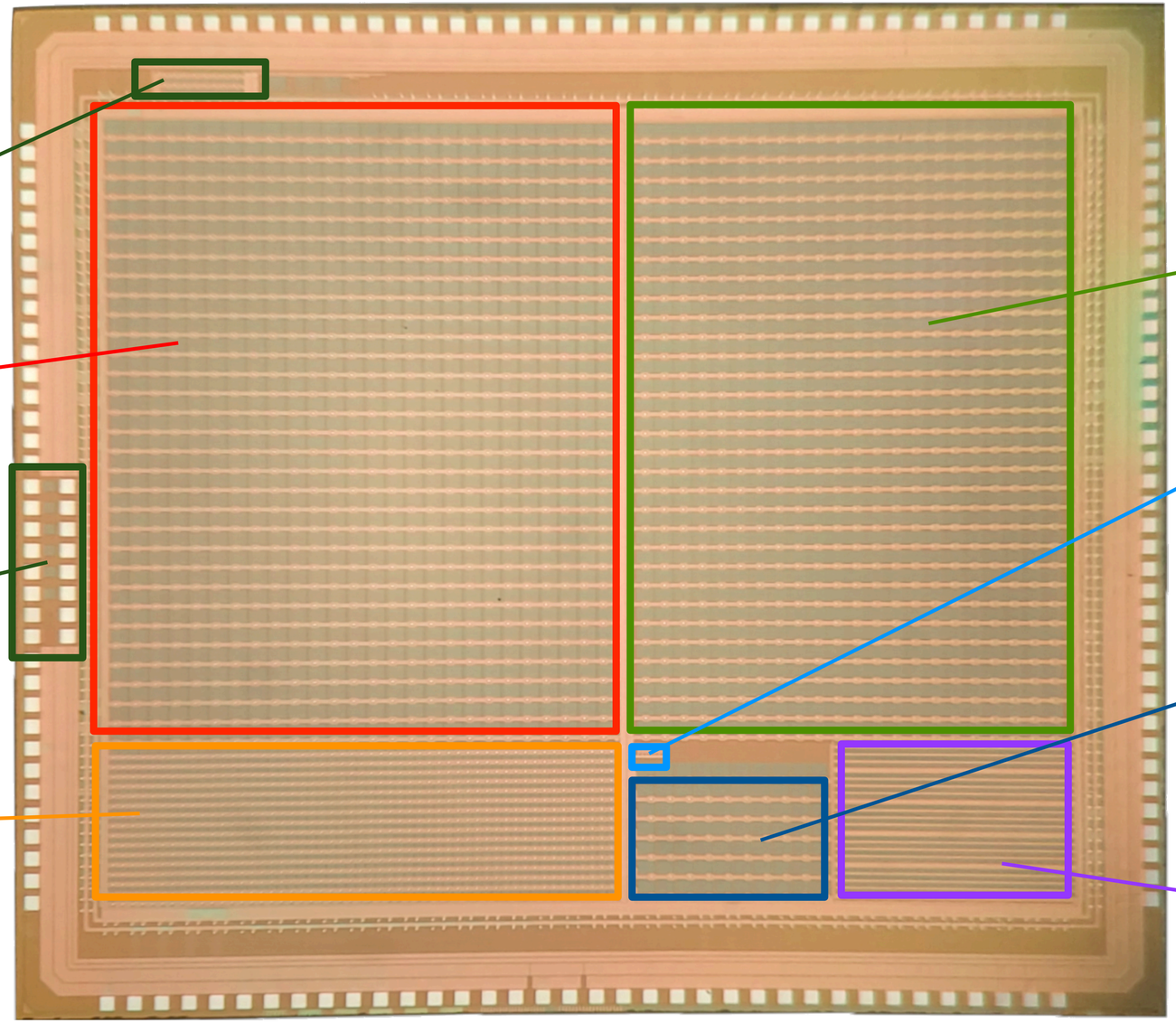
Test chip

structures for timing and ionizing radiation tolerance study

100 um pitch, passive quenching, 1 bit, FF=67% (32x26)

single SPADs

50 um pitch, passive quenching, 1 bit, FF=48% (16x52)



100 um pitch, passive quenching, 10 bit, FF=64% (32x22)

10b/20b TDC and ring oscillator

100 um pitch, active quenching, 1 bit, FF=67% (7x10)

Mini-SiPMs (4x4), 160 um pitch, FF=41% (5x12)

Input from the participants

M. Campajola

Radiation damage

Interest in the characterization of displacement damage effects:

- DCR (and I_{dark}) increase with the displacement damage dose
- Random Telegraph Signals occurrence
- Damage mitigation/recovery with low temperature operations and thermal annealing
  - insights on the damage mechanism

Plan to irradiate samples with:

- protons (or neutrons), and electrons:
  - span over a few orders of magnitude in the range 10^{9} to $10^{11\text{-}12}$ n_{eq} [1]
  - test NIEL scaling model (for particle species and energies)

Timeline:

- second half of 2025, after setup comprehension and devices characterization

Few possibilities to irradiate samples in Europe:

- **protons**: TIFPA, UCL (Belgio), CNA (Spagna), IRRAD (CERN)
- **neutrons**: ENEA Casaccia, INFN-LNL, JSI reactor (Slovenia)
- **electrons** (2MeV): INCT (Varsavia)

[1] Target maximum doses for calorimeters at e+e- colliders. e.g. FCC expected doses

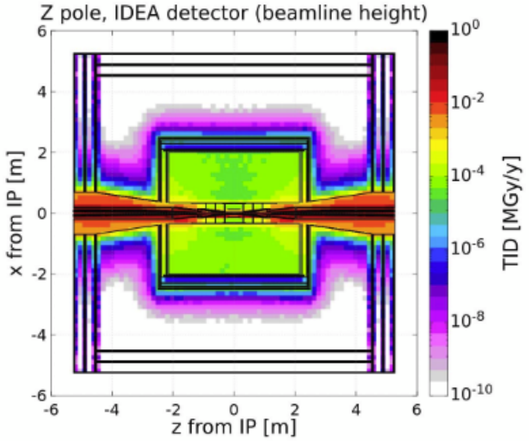
FCC doses

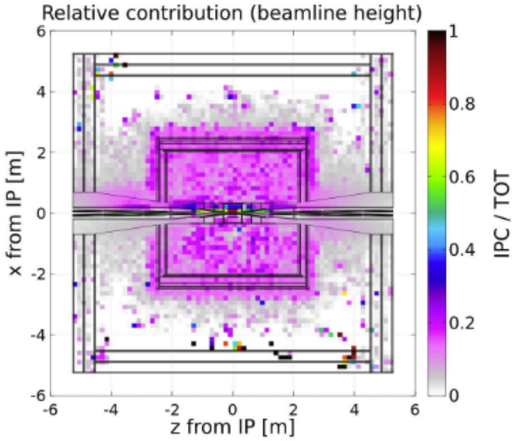
link

IDEA radiation levels (RB + IPC)

incomplete magnetic field map:
results will be altered, to be revisited
with the a map covering the full detector

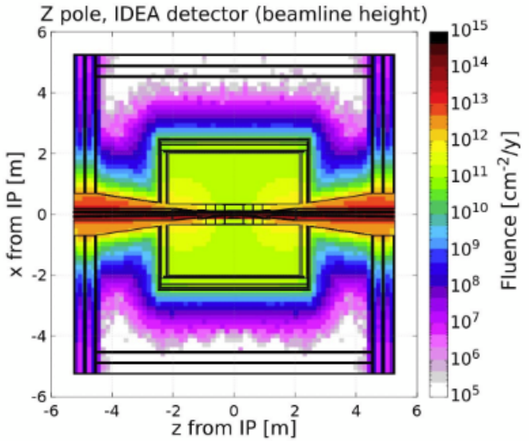
Dose

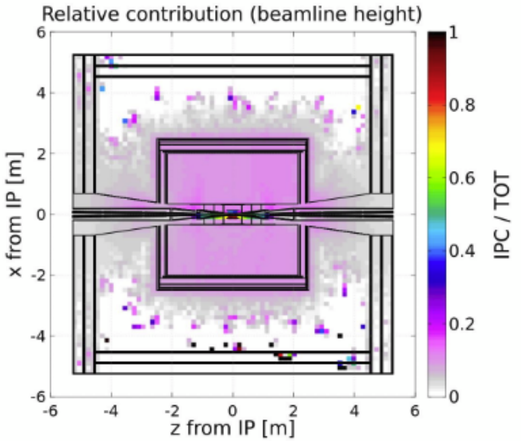




- Drift chamber: 100 Gy/year
- Calorimeter: <10 Gy/year
- RB dominates
- IPC contributes up to 20% in the drift chamber

Fluence





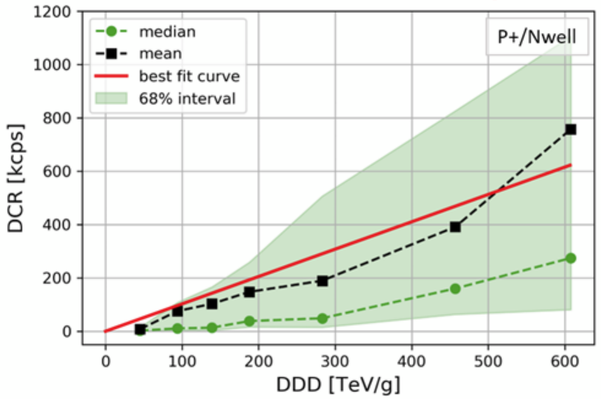
- Drift chamber: 10^{11} cm^{-2}/year
- Calorimeter: <10^{10} cm^{-2}/year
- RB dominates
- IPC contributes up to 10% in the drift chamber

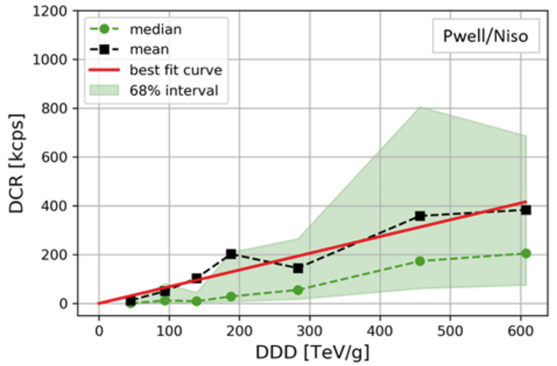
Radiation damage studies

Large degradation observed in previous studies [1]:

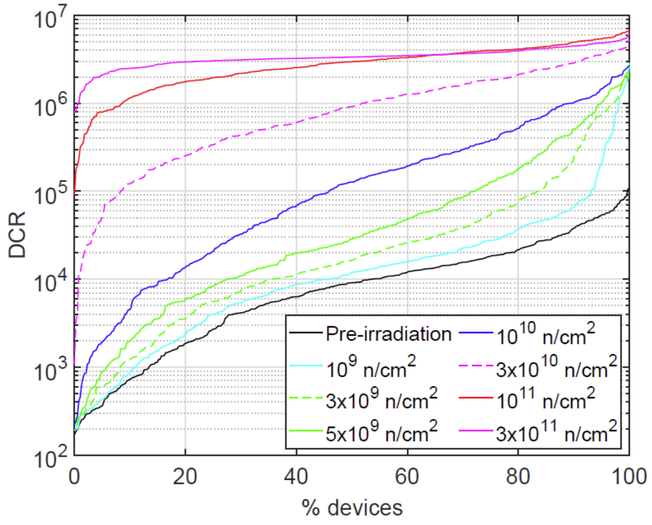
- First 150 nm devices -> few MHz/mm^2
  - ∽ GHz/mm^2 at 10^{10} p/cm^2
- APIX 180 nm devices: 1 MHz/mm^2 [2,3,4]
  - ∽ GHz/mm^2 at 10^{11} n_{eq}/cm^2
  - +30% DCR increase with 1 Mrad

proton irradiation

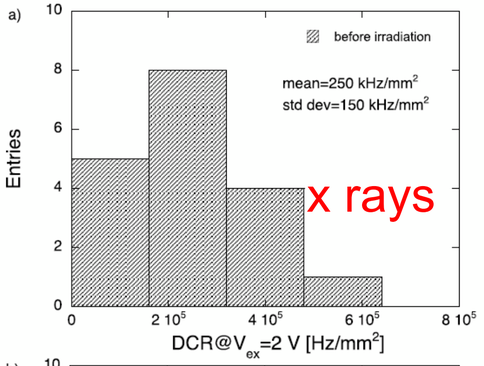


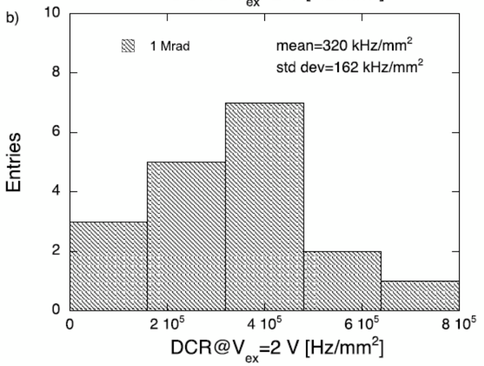


neutron irradiation



x rays





[1] M. Campajola, et al., Proton induced dark count rate degradation in 150-nm CMOS single-photon avalanche diodes, NIMA
[2] M. Musacci, et al. "Radiation tolerance characterization of Geiger-mode CMOS avalanche diodes for a dual-layer particle detector." NIMA
[3] L. Ratti, et al. “Dark Count Rate Degradation in CMOS SPADs Exposed to X-Rays and Neutrons” TNS
[4] A. Ficorella, APPLICATION OF AVALANCHE DETECTORS IN SCIENTIFIC AND INDUSTRIAL MEASUREMENT SYSTEMS, PhD thesis